## MEMORY SUPPORT

- Controls Operation of 8K/16K/32K/64K Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 256K Bytes of Memory Without External Drivers
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
  - Strap-Selected Refresh Rate
  - Synchronous, Predictable Refresh
  - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
  - Interfaces Easily to Popular Microprocessors
- Strap-Selected Wait State Generation for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)
- Three-State Outputs Allow Multiport Memory Configuration

## description

The TMS 4500A is a monolithic DRAM system controller designed to provide address multiplexing, timing, control refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

The controller contains a 16-bit multiplexer that generates the address lines for the memory device from the 16 system address bits and provides the strobe signals required by the memory to decode the address. An 8-bit refresh counter generates the 256-row addresses required for refresh.

A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure data retention

The TMS 4500A also contains refresh/access arbitration circuitry to resolve conflicts between memory access request and memory refresh cycles. The TMS 4500A is offered in a 40-pin, 600-mil dual-in-line plastic package and is guarantee for operation from 0°C to 70°C.

## PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS

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TMS 4500A 40-PIN 600-MIL PLASTIC DUAL-IN-LINE PACKAGE (TOP VIEW)

DYNAMIC RAM CONTRO

CLK	<u> </u>	U,	40	ים	/cc	
RDY	2	:	39	Di	REF	REQ
REN1	]3	:	38		rws	т
<u>č</u> s l	4	:	37		F S 0	
ALE	5	:	36		FS1	
RASO	6	:	35	ים	RA7	
RAS1	7	:	34		CA7	
ACR	8	:	33	]	M A 7	
ACW	9	:	32	]1	M A 6	
CAS	1	0 3	31	$\Box$	CA6	
RAO	11	1 3	30	]	RA6	
CAO	1:	2 3	29		RA5	
MAO	[] 1:	3 3	28		CA5	
MA1	<b>[</b> ] 1	4	27		MAS	i i
CA1	<b>[]</b> 1!	5	26		RA4	
R A 1	<b>[]</b> 1 (	6	25	Þ	CA4	
RA2	1:	7 3	24	],	/ A 4	
CA2	<b>[]</b> 1:	8 3	23		RA3	
MA2	[] 1 !	9 2	22	](	CA3	
GND	2	0 3	21	1	MA 3	
	-					

AGE

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TMS 4500

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