General Information



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Design Considerations



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Voltage Regulator Circuits



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Basic Regulator Theory

The function of every voltage regulator is to convert a dc input voltage into a specific, stable, dc output voltage and maintain that voltage over a wide range of load current and input voltage conditions. To accomplish this, the typical voltage regulator (Figure 1) consists of:

- 1. A reference element that provides a known stable voltage level, (VREF)
- 2. A sampling element to sample the output voltage level
- 3. An error-amplifier element for comparing the output voltage sample to the reference and creating an error signal.
- 4. A power control element to provide conversion of the input voltage to the desired output level over varying load conditions as indicated by the error signal.



Figure 1. Basic Regulator Block Diagram

Although actual circuits may vary, the three basic regulator types are series, shunt, and switching. The four basic functions listed above exist in all three regulator types.

Voltage Regulator Components

Reference Element

The reference element forms the foundation of all voltage regulators since output voltage is directly controlled by the reference voltage. Variations in the reference voltage

will be interpreted as output voltage errors by the error amplifier and cause the output voltage to change accordingly. To achieve the desired regulation, the reference must be stable for all variations in supply voltages and junction temperatures. There are several common techniques which can be used to solve design problems using integrated circuit regulators. Many of these techniques are discussed in the section of the text that outlines error contributions.

Sampling Element

The sampling element monitors the output voltage and converts it into a level equal to the reference voltage. A variation in the output voltage causes the feedback voltage to change to a value which is either greater or less than the reference voltage. This voltage difference is the error voltage which directs the regulator to make the appropriate response and thus correct the output voltage change.

Error Amplifier

The error amplifier of an integrated circuit voltage regulator monitors the feedback voltage for comparison with the reference. It also provides gain for the detected error level. The output of the error amplifier drives the control circuit to return the output to the preset level.

Control Element

All the previous elements discussed remain virtually unaltered regardless of the type regulator circuit. The control element, on the other hand, varies widely, depending upon the type of regulator being designed. It is the element that determines the classification of the voltage regulator; series, shunt, or switching. Figure 2 illustrates the three basic control element configurations, each of which is discussed in detail. These elements contribute an insignificant amount of error to the regulator's performance. This is because the sampling element monitors the output voltage beyond the control element and



Figure 2. Control Element Configurations

compensates for its error contributions. However, the control element directly affects parameters such as minimum input-to-output voltage differential, circuit efficiency, and power dissipation.

Regulator Classifications

Series Regulator

The series regulator derives its name from its control element. The output voltage, V_O , is regulated by modulating an active series element, usually a transistor, that functions as a variable resistor. Changes in the input voltage, V_I , will result in a change in the equivalent resistance of the series element identified as R_S . The product of the resistance, R_S , and the load current, I_L creates a changing input-to-output differential voltage, $V_I - V_O$, that compensates for the changing input voltage. The basic series regulator is illustrated in Figure 3, and the equations describing its performance are listed below.

$$\begin{array}{rcl} V_O &= V_I - (V_I - V_O) \\ (V_I - V_O) &= I_L R_S \\ V_O &= V_I - I_L R_S \end{array}$$

The change in RS for a changing input voltage is:

$$\Delta R_{\rm S} = \frac{\Delta V_{\rm I}}{I_{\rm L}}$$

The change in RS for a changing load current:

$$\Delta R_{S} = \frac{\Delta I_{L} R_{S}}{I_{L} + \Delta I_{L}}$$



Figure 3. Basic Series Regulator

Series regulators provide a simple, inexpensive way to obtain a source of regulated voltage. In high-current applications, however, the voltage drop which is maintained across the control element will result in substantial power loss and a much lower efficiency regulator.

Shunt Regulator

The shunt regulator employs a shunt control element in which the current is controlled to compensate for varying input voltage or changing load conditions. The basic shunt regulator is illustrated in Figure 4.



Figure 4. Basic Shunt Regulator

The output voltage, V_O as with the series regulator, is held constant by varying the voltage drop across the series resistor, R_S, by varying the current I_S. I_S may vary because of I_L changes or it may vary because of current, $I_{(shunt)}$, through the shunt control element. For example, as I_L increases, $I_{(shunt)}$ decreases to adjust the voltage drop across R_S. In this fashion V_O is held constant.

The change in shunt current for a changing load current is:

 $\Delta I_{(shunt)} = -\Delta I_L$

The change in shunt current for a changing input voltage is:

$$\Delta I_{(\text{shunt})} = \frac{\Delta V_{\text{I}}}{R_{\text{S}}}$$
$$I_{(\text{shunt})} = \frac{V_{\text{O}}}{R_{(\text{shunt})}}$$

Even though it is usually less efficient than series or switching regulators, a shunt regulator may be the best choice for some applications. The shunt regulator is less sensitive to input voltage transients; does not reflect load current transients back to the source, and is inherently short-circuit proof.

Switching Regulator

The switching regulator employs an active switch as its control element. This switch is used to chop the input voltage at a varying duty cycle based on the load requirements. A basic switching regulator is illustrated in Figure 5.



Figure 5. Basic Switching Regulator (Step-Down Configuration)

A filter, usually an LC filter, is then used to average the voltage present at its input and deliver that voltage to the output load. Because the pass transistor is either on (saturated) or off, the power dissipated in the control element is minimal. The switching regulator is therefore more efficient than the series or shunt type. For this reason, the switching regulator becomes particularly advantageous for applications involving large input-to-output differential voltages or high load-current requirements. In the past, switching voltage regulators were discrete designs. However, recent advancements in integrated circuit technology have resulted in several monolithic switching regulator circuits that contain all of the necessary elements to design step-up, step-down, or inverting voltage converters. The duty cycle may be varied by:

- 1. maintaining a constant on-time, varying the frequency
- 2. maintaining a constant off-time, varying the frequency
- 3. maintaining a constant frequency, varying the on/off times

Major Error Contributors

The ideal voltage regulator maintains constant output voltage despite varying input voltage, load current, and temperature conditions. Realistically, these influences affect the regulator's output voltage. In addition, the regulator's own internal inaccuracies affect the overall circuit performance. This section discusses the major error contributors, their effects, and suggests some possible solutions to the problems they create.

Regulator Reference Techniques

There are several reference techniques employed in integrated circuit voltage regulators. Each provides its particular level of performance and problems. The optimum reference depends on the regulator's requirements.

Zener Diode Reference

The zener diode reference, as illustrated in Figure 6, is the simplest technique. The zener voltage itself, V_Z , forms the reference voltage, V_{REF} .



Figure 6. Basic Zener Reference

This technique is satisfactory for relatively stable supply-voltage and load-current applications. The changing zener current results in a change in the zener diode's reference voltage, V_Z . This zener reference model is illustrated in Figure 7.

Constant-Current Zener Reference

The zener reference can be refined by the addition of a constant-current source as its supply. Driving the zener diode with a constant current minimizes the effect of zener



Figure 7. Zener Reference Model

impedance on the overall stability of the zener reference. An example of this technique is illustrated in Figure 8. The reference voltage of this configuration is relatively independent of changes in supply voltage and load current.

$$V_{\text{REF}} = V_{Z} + V_{\text{BE}(Q1)}$$
$$I_{Z} = \frac{V_{\text{BE}(Q1)}}{R_{\text{CS}}} + I_{\text{B}}(Q1)$$

In addition to superior supply voltage independence, the circuit illustrated in Figure 8 yields improved temperature stability. The reference voltage, V_{REF} , is the sum of the zener voltage (V_Z) and the base-emitter voltage of Q1[V_{BE(O1)}]. A low temperature



Figure 8. Constant-Current Zener Reference

coefficient can be achieved by balancing the positive temperature coefficient of the zener with the negative temperature coefficient of the base-emitter junction of Q1.

Band-Gap Reference

Another popular reference is the band-gap reference, which developed from the highly predictable emitter-base voltage of integrated transistors. Basically, the reference voltage is derived from the energy-band-gap voltage of the semiconductor material $[V_{go(silicon)} = 1.204 \text{ V}]$. The basic band-gap configuration is illustrated in Figure 9. The reference voltage, V_{REF} , in this case is:

 $V_{REF} = V_{BE(O3)} + I_2 R_2$



Figure 9. Band-Gap Reference

The resistor values of R1 and R2 are selected in such a way that the current through transistors Q1 and Q2 are significantly different ($I_1 = 10I_2$). The difference in current through transistors Q1 and Q2 also results in a difference in their respective base-emitter voltages. This voltage differential [VBE(Q1) - VBE(Q2)] will appear across R3. Application of transistors with sufficiently high gain results in current I₂ passing through R3. In this instance, I₂ is equal to:

$$\frac{\mathbf{V}_{\text{BE}(Q1)} - \mathbf{V}_{\text{BE}(Q2)}}{R3}$$

$$\therefore \mathbf{V}_{\text{REF}} = \mathbf{V}_{\text{BE}(Q3)} + \left[\left(\mathbf{V}_{\text{BE}(Q1)} - \mathbf{V}_{\text{BE}(Q2)} \right) \frac{R2}{R3} \right]$$

By analyzing the effect of temperature on V_{REF} it can be shown that the difference between two similar transistors' emitter-base voltages, when operated at different currents is:

$$V_{BE(Q1)} - V_{BE(Q2)} = \frac{kT}{q} \ln \frac{I_1}{I_2}$$

where

k = Boltzmann's constant T = absolute temperature - degrees K q = charge of an electronI = current

The base-emitter voltage of Q3 can also be expressed as:

$$V_{BE(Q3)} = V_{go} \left[1 - \frac{T}{TO} \right] + V_{BEO} \left[\frac{T}{TO} \right]$$

where

 V_{go} = band-gap potential V_{BEO} = emitter-base voltage at T_O

VREF can then be expressed as:

$$V_{\text{REF}} = V_{\text{go}} \left[1 - \frac{T}{T_{\text{O}}} \right] + V_{\text{BEO}} \left[\frac{T}{T_{\text{O}}} \right] + \frac{R2}{R3} - \frac{kT}{q} \ln \frac{I_1}{I_2}$$

Differentiating with respect to temperature yields

$$\frac{\mathrm{d}\mathbf{V}_{\mathrm{REF}}}{\mathrm{d}\mathrm{T}} = -\frac{\mathrm{V}_{\mathrm{go}}}{\mathrm{T}_{\mathrm{O}}} + \frac{\mathrm{V}_{\mathrm{BEO}}}{\mathrm{T}_{\mathrm{O}}} + \frac{\mathrm{R2}}{\mathrm{R3}} \frac{\mathrm{k}}{\mathrm{q}} \ln \frac{\mathrm{I}_{\mathrm{I}}}{\mathrm{I}_{\mathrm{I}}}$$

If R2, R3, and I1 are appropriately selected such that

$$\frac{R2}{R3} \ln \frac{I_1}{I_2} = [V_{go} - V_{BEO(Q3)}] C$$

where

$$C = \frac{q}{kTO}$$

and

$$V_{go} = 1.2 V$$

the resulting

$$\frac{\mathrm{dV}\mathbf{REF}}{\mathrm{dT}} = 0$$

The reference is temperature-compensated.

Band-gap reference voltage is particularly advantageous for low-voltage applications ($V_{REF} = 1.2 \text{ V}$) and it yields a reference level that is stable even with variations in supply and temperature.

Sampling Element

The sampling element used on most integrated circuit voltage regulators is an R1/R2 resistor divider network (Figure 10), which can be determined by the output-voltage-to-reference-voltage ratio.

$$\frac{V_O}{V_{REF}} = 1 + \frac{R1}{R2}$$

Since the feedback voltage is determined by ratio and not absolute value, proportional variations in R1 and R2 have no effect on the accuracy of the integrated circuit voltage regulator. When proper attention is given to the layout of these resistors in an integrated circuit, their contribution to the error of the voltage regulator will be minimal. The initial accuracy is the only parameter affected.



Figure 10. R1/R2 Ladder Network Sampling Element

If a stable reference and an accurate output sampling element exist, the error amplifier becomes the primary factor determining the performance of the voltage regulator. Typical amplifier performance parameters such as offset, common-mode and supply-rejection ratios, output impedance, and temperature coefficient affect the accuracy and regulation of the voltage regulator. These amplifier performance parameters will affect the accuracy of the regulator due to variations in supply, load, and ambient temperature conditions.

Offset Voltage

Offset voltage is viewed by the amplifier as an error signal, as illustrated in Figure 11, and will cause the output to respond accordingly.

$$V_{O} = A_{V}V_{I}$$

$$V_{I} = V_{REF} - V_{IO} - V_{FB}$$

$$V_{FB} = V_{O} \left[\frac{R2}{R1 + R2} \right]$$

$$V_{O} = \frac{V_{REF} - V_{IO}}{\frac{1}{A_{V}} + \left[\frac{R2}{R1 + R2} \right]}$$

If AV is sufficiently large

$$V_{O} = (V_{REF} - V_{IO}) \left[1 + \frac{R1}{R2} \right]$$

 V_{IO} represents an initial error in the output of the integraged circuit voltage regulator. The simplest method of compensating for this error is to adjust the output voltage sampling element R1/R2.

Offset Change with Temperature

The technique discussed above compensates for the amplifier's offset voltage and yields an accurate regulator, but only at a specific temperature. In most amplifiers, the offset voltage change with temperature is proportional to the initial offset level. Trimming the output voltage sampling element, does not reduce the offset voltage but merely counteracts it. At a different ambient tmperature, the offset voltage changes and, thus, error is again introduced into the voltage regulator. Monolithic integrated circuit regulators use technology that essentially eliminates offset in integrated circuit amplifiers. With minimal offset voltage, drift caused by temperature variations will have little consequence.





Supply Voltage Variations

The amplifier's power supply and common-mode rejection ratios are the primary contributors to regulator error which has been introduced by an unregulated input voltage. In an ideal amplifier, the output voltage is a function of the differential input voltage only. Realistically, the common-mode voltage of the input also influences the output voltage. The common-mode voltage is the average input voltage, referenced from the amplifier's virtual ground (see Figure 12 and the following equations).



Figure 12. Amplifier Model Showing Common-Mode Voltage

$$\begin{split} V_{I(av)} &= \frac{V_{S} + V_{O} \left[\frac{R2}{R1 + R2} \right]}{2} \\ V_{CM} &= \frac{1}{2} \left[V_{S} + V_{O} \left(\frac{R2}{R1 + R2} \right) - \left(V_{CC} + + V_{CC} - \right) \right] \\ \text{From this relation, it can be seen that unequal variations in either power supply bus rail will result in a change in the common-mode voltage. The common-mode voltage rejection ration (CMRR) is the ratio of the amplifier's differential voltage amplification to the common-mode voltage amplification. \end{split}$$

$$CMRR = \frac{AVD}{AVCM}$$
$$AVCM = \frac{AVD}{CMRR}$$

That portion of output which is voltage contributed by the equivalent common-mode input voltage is:

$$V_{O} = V_{CM}A_{VCM} = \frac{A_{VD}V_{CM}}{CMRR}$$

Virtual ground = $\frac{V_{CC+} + V_{CC-}}{2}$

The equivalent error introduced then is:

$$COMMON-MODE ERROR = \frac{VCM}{CMRR}$$

The common-mode error represents an offset voltage to the amplifier. Neglecting the actual offset voltage, the output voltage of the error amplifier then becomes:

$$V_{O} = \left(V_{REF} + \frac{V_{CM}}{CMRR}\right) \left(1 + \frac{R1}{R2}\right)$$

Using constant-current sources in most integrated circuit amplifiers, however, yields a high power-supply (common-mode) rejection ratio. This power-supply rejection ratio is of such a large magnitude that the common-mode voltage effect on V_O can usually be neglected.

Regulator Design Considerations

Various types of integrated circuit voltage regulators are available, each having its own particular characteristics, giving it advantages in various applications. The type of regulator used depends primarily upon the designer's needs and trade-offs in performance and cost.

Positive vs Negative Regulators

This classification of voltage regulators is easily understood; a positive regulator is used to regulate a positive voltage, and a negative regulator is used to regulate a negative voltage. However, what is positive and negative may vary, depending upon the ground reference.

Figure 13 illustrates conventional positive and negative voltage regulator applications employing a continuous and common ground. For systems operating on a single supply, the positive and negative regulators may be interchanged by floating the ground reference to the load or input. This approach to design is recommended only where ground isolation serves as an advantage to overall system performance.



Figure 13. Conventional Positive/Negative Regulator

Figures 14 and 15 illustrate a positive regulator in a negative configuration and a negative regulator in a positive configuration, respectively.



Figure 14. Positive Regulator in Negative Configuration



Figure 15. Negative Regulator in Positive Configuration

Fixed vs Adjustable Regulators

Many fixed three-terminal voltage regulators are available in various current ranges from most major integrated circuit manufacturers. These regulators offer the designer a simple, inexpensive method to establish a regulated voltage source. Their particular advantages are:

- 1. Ease of use
- 2. Few external components required
- 3. Reliable performance
- 4. Internal thermal protection
- 5. Short-circuit protection.

There are disadvantages. The fixed three-terminal voltage regulators cannot be precisely adjusted because their output voltage sampling elements are internal. The initial accuracy of these devices may vary as much as $\pm 5\%$ from the nominal value; also the output voltages available are limited.

Current limits are based on the voltage regulator's applicable current range and are not adjustable. Extended range operation (increasing I_{LOAD}) is cumbersome and requires complex external circuitry.

The adjustable regulator may be well suited for those applications requiring higher initial accuracy. This depends on the complexity of the adjustable voltage regulator. Additionally, all adjustable regulators use external feedback, which allows the designer a precise and infinite voltage selection.

The output sense may also be referred to a remote point. This allows the designer to not only extend the range of the regulator (with minimal external circuitry), but also to compensate for losses in a distributed load or external pass components. Additional features found on many adjustable voltage regulators are: adjustable short-circuit current limiting, access to the voltage reference element, and shutdown circuitry.

Dual-Tracking Regulator

The dual-tracking regulator (Figure 16) provides regulation for two power supply buses, usually one positive and one negative. The dual-tracking feature assures a balanced supply system by monitoring the voltage on both power supply buses. If either of the voltages sags or goes out of regulation, the tracking regulator will cause the other voltage to vary accordingly (A 10% sag in the positive voltage will result in a 10% sag in the negative voltage.). These regulators are, for the most part, restricted to applications such as linear systems where balanced supplies offer a definite performance improvement.



Figure 16. Dual-Tracking Regulator

Series Regulator

The series regulator is well suited for medium current applications with nominal voltage differential requirements. Modulation of a series pass control element to maintain a well-regulated, prescribed, output voltage is a straightforward design technique. Safe-operating-area protection circuits such as overvoltage, fold-back current limiting, and short-circuit protection are additional functions that series regulators can supply. The primary disadvantage of the series regulator is its power consumption. The amount of power a series regulator (Figure 17) will consume depends on the load current being drawn from the regulator and is proportional to the input-to-output voltage differential. The amount



Figure 17. Series Regulator

of power consumed becomes considerable with increasing load or differential voltage requirements. This power loss limits the amount of power that can be delivered to the load because the amount of power that can be dissipated by the series regulator is limited.

The equations that describe these conditions are listed below. P_{REG} is the power lost in the regulator, I_I is the input current, I_{REG} is the regulator current and I_L is the load current. The differential voltage across the regulator is $(V_I - V_O)$.

 $P_{\text{REG}} = V_{\text{I}}I_{\text{I}} - V_{\text{O}}I_{\text{L}}$ $I_{\text{I}} = I_{\text{REG}} + I_{\text{L}}$

Since IL is much greater than IREG

$$I_I = I_L$$

 $P_{REG} = I_L (V_I - V_O)$

Floating Regulator

The floating regulator (Figure 18) is a variation of the series regulator. The output voltage remains constant by changing the input-to-output voltage differential for varying input voltage. The floating regulator's differential voltage is modulated such that its output voltage when referenced to its common terminal $V_{O(reg)}$ is equal to its internal reference (V_{REF}). The voltage developed across the output-to-common terminal is equal to the voltage developed across R1(V_{R1}).



Figure 18. Floating Regulator

$$V_{O(reg)} = V_{REF} = V_{R1}$$
$$V_{R1} = V_O \left[\frac{R1}{R1 + R2} \right]$$
$$V_O = V_{REF} \left[1 + \frac{R2}{R1} \right]$$

The common-terminal voltage is:

 $V_{COM} = V_O - V_{R1} = V_O - V_{REF}$

The input voltage seen by the floating regulator is:

$$V_{I(reg)} = V_{I} - V_{COM}$$
$$V_{I(reg)} = V_{I} - V_{O} + V_{REF}$$
$$V_{I(reg)} = V_{DIFF} + V_{REF}$$

Since V_{REF} is fixed, the only limitation on the input voltage is the allowable differential voltage. This makes the floating regulator especially suited for high-voltage applications ($V_I > 40$ V). Practical values of output voltage are limited to practical ratios of output-to-reference voltages.

$$\frac{R2}{R1} = \frac{V_O}{V_{REF}} - 1$$

The floating regulator exhibits power consumption characteristics similar to that of the series regulator from which it is derived, but unlike the series regulator, it can also serve as a current regulator as shown in Figure 19.

$$V_{O} = V_{REF} \left[1 + \frac{R_{L}}{R_{S}} \right]$$
$$V_{O} = V_{L} + V_{O}(reg)$$
$$V_{O}(reg) = V_{REF}$$
$$V_{L} = V_{REF} \left[1 + \frac{R_{L}}{R_{S}} \right] - V_{REF}$$
$$V_{L} = V_{REF} \left[\frac{R_{L}}{R_{S}} \right]$$
$$I_{L} = \frac{V_{LOAD}}{R_{L}}$$
$$I_{LOAD} = \frac{V_{REF}}{R_{S}}$$



Figure 19. Floating Regulator as a Constant-Current Regulator

Shunt Regulator

The shunt regulator, illustrated in Figure 20, is the simplest of all regulators. It employs a fixed resistor as its series pass element. Changes in input voltage or load current requirements are compensated by modulating the current which is shunted to ground through the regulator.

For changes in $\dot{V_I}$: $\Delta I_Z = \frac{\Delta V_I}{R_S}$

For changes in IL: $\Delta I_Z = -\Delta I_L$



Figure 20. Shunt Regulator

The inherent short-circuit-proof feature of the shunt regulator makes it particularly attractive for some applications. The output voltage will be maintained until the load current required is equal to the current through the series element (see Figure 21). Since the shunt regulator cannot supply any current, additional current required by the load will result in reducing the output voltage to zero.



Figure 21. Output Voltage vs Shunt Current of a Shunt Regulator

 $V_O = V_I - I_L R_S$

The short-circuit current of the shunt regulator then becomes:

$$V_{O} = 0$$
$$I_{SC} = \frac{V_{I}}{R_{S}}$$

4 Design Considerations



The switching regulator lends itself primarily to the higher power applications or those applications where power supply and system efficiency are of the utmost concern. Unlike the series regulator, the switching regulator operates its control element in an onor off-mode. Switching regulator control element modes are illustrated in Figure 22.





In this manner, the control element is subjected to a high current at a very low voltage or a high differential voltage at a very low current. In either case, power dissipation in the control element is minimal. Changes in the load current or input voltage are compensated for by varying the on-off ratio (duty cycle) of the switch without increasing the internal power dissipated in the switching regulator. See Figure 23(a).

For the output voltage to remain constant, the net charge in the capacitor must remain constant. This means the charge delivered to the capacitor must be dissipated in the load.

$$I_{C} = I_{L'} - I_{L}$$

$$I_{C} = -I_{L} \text{ for } I_{L'} = 0$$

$$I_{C} = I_{L(pk)} - I_{L} \text{ for } I_{L'} = I_{L(pk)}$$

The capacitor current waveform then becomes that illustrated in Figure 23(b). The charge delivered to the capacitor and the charge dissipated by the load are equal to the areas under the capacitor current waveform.

$$\Delta Q + = \frac{1}{2} \frac{(I_{L}(pk) - I_{L})^{2}}{I_{L}(pk)} t \left(\frac{V_{I}}{V_{C}}\right)$$

$$\Delta Q - = I_{L} \left[t_{period} - \frac{1}{2} t \left(\frac{V_{I}}{V_{C}}\right) - \frac{1}{2} t \left(\frac{I_{L}(pk) - I_{L}}{I_{L}(pk)}\right) \left(\frac{V_{I}}{V_{C}}\right) \right]$$

By setting ΔQ + equal to ΔQ - , the relationship of I_L and I_{L(pk)} for ΔQ = 0 can be determined;

$$I_{L} = \frac{1}{2} I_{L}(pk) \left[\frac{V_{I}}{V_{C}} \frac{t}{t_{period}} \right]$$

As this demonstrates, the duty cycle t/t_{period} can be altered to compensate for input voltage changes or load variations.

The duty cycle t/tperiod can be altered a number of different ways.

 $t = t_{on}$ (inductor charge time)

 t_{period} = Total time $(t_{on} + t_{off} + t_I)$ where t_I is the time from t_{off} until the start of the next charge cycle.

Knowing tperiod then:

$$f = \frac{1}{t_{period}}$$



Fixed-On-Time, Variable Frequency

One technique of voltage regulation is to maintain a fixed or predetermined "on" time (t), the time the input voltage is being applied to the LC filter and vary the duty cycle by varying the frequency (f). This method makes voltage conversion applications design easier (step-up, step-down, invert) since the energy stored in the inductor of the LC filter during the on-time (which is fixed) determines the amount of power deliverable to the load. Thus calculation of the inductor is fairly straightforward.

Design Considerations

$$L = \frac{V}{I} t$$

where

L = value of inductance in microhenrys

V = differential voltage in volts

- I = required inductor current defined by the load in amps
- t = on-time in microseconds

The fixed-on-time approach is also advantageous from the standpoint that a consistent amount of energy is stored in the inductor during the fixed on-time period. This simplifies the design of the inductor by defining the operating parameters to which the inductor is subjected. The operating characteristic of a fixed-on-time switching voltage regulator is a varying frequency, which changes directly with changes in the load. This can be seen in Figure 24.



Figure 24. Frequency vs Load Current for Fixed On-Time SVR

Fixed-Off-Time, Variable Frequency

In the fixed-off-time switching voltage regulator, the average dc voltage is varied by changing the on time (t) of the switch while maintaining a fixed off-time (t_{off}). The fixed-off-time switching voltage regulator behaves in a manner opposite that of the fixed-on-time regulator.

As the load current increases, the on time is made to increase, thus decreasing the operating frequency; this is illustrated in Figure 25. This approach provides the capability to design a switching voltage regulator that will operate at a well-defined minimum frequency under full-load conditions.

The fixed-off-time approach also allows a dc current to be established in the inductor under increased load conditions, thus reducing the ripple current while maintaining the same average current. The maximum current experienced in the inductor under transient load conditions is not as well defined as that found in the fixed-on-time regulator. Thus, additional precautions should be taken to ensure that the inductor does not saturate.



Figure 25. Frequency vs Load Current for Fixed Off-Time SVR

Fixed-Frequency, Variable Duty Cycle

The fixed-frequency switching regulator varies the duty cycle of the pulse train in order to change the average power. The fixed-frequency concept is particularly advantageous for systems employing transformer-coupled output stages. The fixed frequency permits efficient design of the associated magnetics. Transformer coupling also has advantages in single and multiple voltage-conversion applications. The fixed-frequency regulator will establish a dc current through the inductor (for increased load conditions) to maintain the required load current with minimal ripple current. The single-ended and transformer-coupled configurations are illustrated in Figure 26.





These types of switching regulators can thus be operated with high efficiency to provide low-voltage, regulated outputs from a high-voltage, unregulated supply or vice versa. The switching frequency should be established at the optimum value for the switching components of the supply (transformer, switching transistor, inductor, and filter capacitor). High-frequency operation is distinctly advantageous because the cost, weight, and volume of both L and C filter elements are reduced. However, the frequency at which the effective series resistance of the filter capacitor equals its capacitive reactance is the maximum allowable frequency.

Operation above 20 kHz is desirable to eliminate the possibility of audible noise. Choosing an operating frequency that is too high will result in power switching transistor losses as well as "catch" diode losses. The higher cost of these high performance components must be balanced against the reduced cost, size, and weight of the L and C components when determining the optimum frequency for a specific application.

Regulator Safe Operating Area

The safe operating area (SOA) is a term used to define the input and output voltage range and load current range within which any device is designed to operate reliably. Exceeding these limits will result in a catastrophic failure or will render the device temporarily inoperative, depending upon the device and its performance characteristics. Integrated circuit voltage regulators with internal current limiting, thermal and short-circuit protection will merely shut down. External components, such as pass transistors on the other hand, may respond with catastrophic failure.

Regulator SOA Considerations

Although particular design equations depend upon the type of integrated circuit voltage regulator used and its application, there are several boundaries that apply to all regulator circuits for safe, reliable performance.

Input Voltage

The limits on the input voltage are derived from three considerations:

VImax

The absolute maximum rated input voltage as referenced to the regulator's ground. This is a safe operating area (SOA) destruct limit.

 $(V_I - V_O)min$

The input-to-output differential voltage also referred to as the dropout voltage, at which the regulator ceases to function properly. This is a functional limit.

 $(V_I - V_O)max$

The maximum input-to-output differential voltage. Usually, the regulator's power dissipation is exceeded prior to the $(V_I - V_O)_{max}$ limit. This is an SOA level that can be limited by the allowable power dissipation (P_{Dmax}).

Load Current

ILmax

The maximum load current deliverable from the integrated circuit regulator. If internal current limiting is not provided, external protection should be provided. This is a functional limit that may be further limited by PDmax.

Power Dissipation

PDmax

The maximum power that can be dissipated within the regulator. Power dissipation is the product of the input-to-output differential voltage and the load current, and is normally specified at or below a given case temperature. This rating is usually based on a 150 °C junction temperature limit. The power rating is an SOA limit unless the integrated circuit regulator provides an internal thermal protection.

Output Voltage of an Adjustable-Voltage Regulator

VOmin

The minimum output voltage a regulator is capable of regulating. This is usually a factor of the regulator's internal reference and is a functional limit.

VOmax

The maximum output voltage a regulator is capable of regulating. This is largely dependent on the input voltage and is a functional limit.

External Pass Transistor

For applications requiring additional load current, integrated circuit voltage regulator capabilities may be boosted with the addition of an external pass transistor. When employed, the external pass transistor, in addition to the voltage regulator, must be protected against operation outside its safe operating area. Operation outside the safe operating area is catastrophic to most discrete transistors.

ICmax

The maximum current the transistor is capable of sustaining. I_{Cmax} now becomes the maximum current the regulator circuit is capable of delivering to the load. Associated with I_{Cmax} is a collector-emitter voltage ($V_{CE} = V_I - V_O$). If the product ($V_I - V_{Omax}$) I_{Cmax} exceeds the SOA then I_{Cmax} will have to be derated. This will then become a functional limit instead of a catastrophic limit. I_{Cmax} is related to power dissipation and junction or case temperature. I_{Cmax} must again be derated if the thermal or power ratings at which it is specified are exceeded. The resulting derated I_{Cmax} should continue to be considered as a catastrophic limit. Actual I_{Cmax} limits and derating information will appear on the individual transistor specification.

VCEmax

The maximum collector-emitter voltage that can be applied to the transistor in the off-state. Exceeding this limit can be catastrophic.

PDmax

The maximum power that can be dissipated by the transistor. This is usually specified at a specific junction or case temperature. If the transistor is operated at higher temperatures, the maximum power must be derated in accordance with the operating rules specified in the transistor's applicable specification. Prolonged operation above the transistor's maximum power rating will result in degradation or destruction of the transistor.

Safe Operating Protection Circuits

Selection of the proper integrated circuit voltage regulators and external components will result in a reliable design in which all devices can operate well within their respective safe operating areas. Fault conditions (such as a short-circuit or excessive load) may cause components in the regulator circuit to exceed their safe operating area operation. Because of this situation, as well as protection for the load, certain protection circuits should be considered.

Reverse Bias Protection

A potentially dangerous condition may occur when a voltage regulator becomes reverse biased. For example, if the input supply were crowbarred to protect either the supply itself or additional circuitry, the filter capacitor at the output of the regulator circuit would maintain the regulator's output voltage and the regulator circuit would be reverse biased. If the regulated voltage is large enough (greater than 7 V), the regulator circuit may be damaged. To protect against this, a diode can be used as illustrated in Figure 27.



Figure 27. Reverse Bias Protection

Current Limiting Techniques

The type of current limiting used depends primarily on the safe operating area of the pass element used. The three basic current limiting techniques are series resistor, constant current, and fold-back current limiting.

Series Resistor

This is the simplest method for short-circuit protection. The short-circuit current is determined by the current-limiting resistor R_{CL} , illustrated in Figure 28.

$$V_O = V_{O(reg)} - I_L R_{CL}$$

A short-circuit condition occurs when $V_{O} = 0$, thus:

$$I_{SC} = I_L @ (V_O = 0) = \frac{V_O(reg)}{R_{CL}}$$



Figure 28. Series Resistance Current Limiter

The primary drawback of this technique is error introduced by the voltage dropped across R_{CL} under varying load conditions. The % error, as illustrated by the following equations, depends on the R_{CL} and R_L values.

$$I_{L} = \frac{V_{O}}{R_{L}}$$
$$V_{O} = \frac{V_{O}(reg)}{1 + \frac{R_{CL}}{R_{L}}}$$
$$ERROR = \frac{V_{O}(reg) - V_{O}}{V_{O}(reg)}$$

$$\% \text{ ERROR} = \frac{R_{CL}}{R_L + R_{CL}}$$

%
Maintaining R_{CL} at a level which is an order of magnitude less than the nominal load impedance minimizes this effect.

$$R_{CL} = \frac{1}{10} R_L$$
 % ERROR = 9.1%

This also yields a short-circuit current that is an order of magnitude greater than the normal operating load current.

$$I_{L(norm)} = \frac{V_{O(reg)}}{R_{CL} + R_{L(norm)}}$$
$$I_{SC} = \frac{V_{O(reg)}}{R_{CL}}$$
$$I_{SC} = 11 I_{L(norm)}$$

This technique is obviously inefficient since it requires using a regulator or pass element with current capabilities in excess (11X) of its normal operating capabilities. The performance characteristics of a series resistance current limited regulator are illustrated in Figure 29.



Figure 29. Performance Characteristics of a Series Resistance Current-Limited Regulator

Constant-Current Limiting

Constant-current limiting is the most popular current-limiting technique in low-power, low-current regulator circuits. The basic configuration is illustrated in Figure 30. Note that this method requires access to the control element and remote voltage sense capabilities. By sensing the output voltage beyond the current limiting resistor, the circuit allows the regulator to compensate for the voltage changes across R_{CL}.



Figure 30. Constant-Current Limit Configuration

If an external pass transistor is used, its base current may be starved to accomplish constant-current limiting, as illustrated in Figure 31. Current limiting takes effect as the voltage drop across R_{CL} approaches the potential required to turn on transistor Q1. As Q1 is biased on, the current supplying the base of Q2 is diverted, thus decreasing the drive current to Q3, the regulator's pass transistor. The performance characteristics of a constant-current limited regulator are illustrated in Figure 32.



Figure 31. Constant Current Limiting for External Pass Transistor Applications

It should be noted that short-circuit conditions are the worst conditions that can be imposed on the pass transistor since it has to survive not only the short-circuit current, but it has to withstand the full input voltage across its collector and emitter terminals.



Figure 32. Constant-Current Limiting

This normally requires the use of a pass transistor with power handling capabilities much greater than those required for normal operation i.e.:

 $V_{I} = 20 V$ $V_{O} = 12 V$ $I_{O} = 700 mA$ NOMINAL $P_{D} = (20 V - 12 V) \times 0.7 A = 5.6 W$ For $I_{SC} = 1 A(150\% I_{OUT})$: SHORT-CIRCUIT $P_{D} = 20 V \times 1 A = 20 W$

This requirement may be reduced by the application of fold-back current limiting.

Fold-Back Current Limiting

Fold-back current limiting is used primarily for high-current applications where the normal operating requirements of the regulator dictate the use of an external power transistor. The performance characteristics of a fold-back current limiting regulator are illustrated in Figure 33. The principle of fold-back current limiting provides limiting at a predetermined current (I_K). At this predetermined current, feedback reduces the load current as the load continues to increase (R_L decreasing) and causes the output voltage to decay.

The fold-back current-limiting circuit of Figure 34, behaves in a manner similar to the constant-current limit circuit illustrated in Figure 31. In Figure 34, the potential developed across the current limit sense resistor (R_{CL}) must not only develop the base-emitter voltage required to turn on Q1, but it must develop sufficient potential to overcome the voltage across resistor R1.

$$V_{BE(Q1)} = R_{CL}I_L - \frac{V_O + R_{CL}I_L}{R1 + R2} \times R1$$
$$\therefore I_K = \frac{V_{BE(Q1)} (R1 + R2) + V_O R1}{R_{CL}R2}$$



Figure 33. Fold-Back Current Limiting

As the load current requirement increases above I_K, the output voltage (V_O) decays. The decreasing output voltage results in a proportional decrease in voltage across R1. Thus, less current is required through R_{CL} to develop sufficient potential to maintain the forwardbiased condition of Q1. This can be seen in the above expression for I_K. As V_O decreases, I_K decreases. Under short-circuit conditions, (V_O = 0) I_K becomes:

$$I_{SC} = I_K @ (V_O = 0) = \frac{V_{BE(Q1)}}{R_{CL}} \left[1 + \frac{R1}{R2} \right]$$

The approach illustrated in Figure 34 allows a more efficient design because the collector current of the pass transistor is less during short-circuit conditions than it is during normal operation. This means that during short-circuit conditions, when the voltage across the pass transistor is maximum, the collector-emitter current is reduced. As illustrated in Figure 35, fold-back current limiting fits closer to the typical performance characteristics of the transistor, thus allowing a better design match of the pass transistor to the regulator.



Figure 34. Fold-Back Current Limit Configuration



Figure 35. Fold-Back Current Limit Safe Operating Area

Three-Terminal Regulators

Three-terminal IC regulators have been especially useful to the designer of small, regulated power supplies or on-card regulators. Three-terminal regulators are popular because they are small and require a minimum number of external components.

Stabilization

Mounting and using three-terminal regulators usually presents no problem, however, there are several precautions that should be observed. Positive regulators, in general, use n-p-n emitter follower output stages whereas negative regulators use n-p-n common-emitter stages with the load connected to the collector. The emitter follower output stage configuration is not used in negative regulators because monolithic p-n-p series-pass transistors are more difficult to make. Due to their output stage configuration, positive regulators are more stable than negative regulators. Therefore, the practice of bypassing positive regulators may be omitted in some applications. It is good practice, however, to use bypass capacitors at all times.

For a positive regulator, a $0.33-\mu F$ bypass capacitor should be used on the input terminals. While not necessary for stability, an output capacitor of $0.1 \ \mu F$ may be used to improve the transient response of the regulator. These capacitors should be on or as near as possible to the regulator terminals. See Figure 36.

When using a negative regulator, bypass capacitors are a must on both the input and output. Recommended values are 2 μ F on the input and 1 μ F on the output. It is considered good practice to include a 0.1- μ F capacitor on the output to improve the transient response (Figure 37). These capacitors may be mylar, ceramic, or tantalum, provided that they have good high frequency characteristics.



Figure 36. Positive Regulator



Figure 37. Negative Regulator

Fixed Dual Regulators

When building a dual power supply with both a positive and a negative regulator, extra precautions should be taken. If there is a common load between the two supplies, latch-up may occur. Latch-up occurs because a three-terminal regulator does not tolerate a reverse voltage of more than one-diode drop. To prevent this latch-up problem, it is good design practice to place reversed-biased diodes across each output of a dual supply. While the diodes should not be necessary if the dual regulator outputs are referenced to ground, latch-up may occur at the instant power is turned on, especially if the input voltage to one regulator rises faster than the other. This latch-up condition usually affects the positive regulator rather than the negative regulator. These diodes prevent reverse voltage to the regulator and prevent parasitic action from taking place when the power is turned on. The diodes should have a current rating of at least half the output current. A recommended circuit for a dual 15-V regulated supply is illustrated in Figure 38.

In Figure 38, 1N4001 diodes are placed directly across the regulators, input to output. When a capacitor is connected to the regulator output, if the input is shorted to ground, the only path for discharging the capacitor normally is back through the regulator. This could be (and usually is) destructive to the regulator. The diodes across the regulator divert any discharge current, thus protecting the regulator.



Figure 38. Regulated Dual Supply

Series Adjustable Regulator

Figure 39 illustrates a typical circuit for an LM317 adjustable positive regulator with the output adjustable from 1.2 V to 17 V and up to 1.5 A of current. (A typical input supply uses a 25.2-V transformer and a full-wave bridge rectifier.)

Stabilization, as described earlier for fixed three-terminal regulators, is usually not required. Although the LM317 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This effect occurs with values between 500 pF and 5000 pF. Using a $10-\mu$ F aluminum electrolytic on the output swamps this effect and ensures stability.



Figure 39. Positive Adjustable Series Regulator

C1 is the power supply filter capacitor following the rectifier section and should be connected close to the regulator input for maximum stability. If the input were to be shorted, D1 would divert the discharge current around the regulator, protecting it. Also, with both D1 and D2 in the circuit, when the input is shorted, C2 is discharged through both diodes. In general, a diode should be used in the position occupied by D1 on all positive regulators to prevent reverse biasing. This becomes more important at higher output voltages since the energy stored in the capacitors is larger. Bypassing the adjustment terminal (C2) improves ripple rejection. Output capacitor C3 is added to improve the transient response of the regulator.

In both the negative (LM337) and the positive (LM317) series adjustable regulators, there is an internal diode from the input to the output. If the total output capacitance is less than 25 μ F, D1 may be omitted.

Layout Guidelines

As implied in the previous sections, component layout and orientation plays an important, but often overlooked, role in the overall performance of the regulator. The importance of this role depends upon such things as power level, the type of regulator, the overall regulator circuit complexity, and the environment in which the regulator operates. The general layout rules, as well as remote voltage sensing, and component layout guidelines are discussed in the following text.

Layout Design Factors

Most integrated circuit regulators use wide-band transistors to optimize their response. These regulators must be compensated to ensure stable closed-loop operation. This compensation can be counteracted by a layout which has excess external stray capacitance and line inductance. For this reason, circuit lead lengths should be held to a minimum. Lead lengths associated with external compensation or pass transistor elements are of primary concern. These components, especially, should be located as close as possible to the regulator control circuit. In addition to affecting a regulator's susceptibility to spurious oscillation, the layout of the regulator also affects its accuracy and performance.

Input Ground Loop

Improper placement of the input capacitor can induce unwanted ripple on the output voltage. Care should be taken to ensure that currents in the input circuit do not flow in the ground line that is in common with the load return. This would cause an error voltage resulting from the peak currents of the filter capacitor flowing through the line resistance of the load return. See Figure 40 for an illustration of this effect.





Figure 40. Circuit Layout Showing Error Contributions

Output Ground Loop

Similar in nature to the problem discussed on the input, excessive lead length in the ground return line of the output results in additional error. Because the load current flows in the ground line, an error equivalent to the load current multiplied by the line resistance (R3') will be introduced in the output voltage.

Remote Voltage Sense

The voltage regulator should be located as close as possible to the load. This is true especially if the output voltage sense circuitry is internal to the regulator's control device. Excessive lead length will result in an error voltage developed across the line resistance (R4').

$$V_{O} = V_{O(reg)} - (R_{2'} + R_{3'} + R_{4'}) I_{L} + R_{2'} I_{reg}$$

 $ERROR = I_L(R_3' + R_4') - I_{reg}R_2'$

If the voltage sense is available externally, the effect of the line resistance can be minimized. By referencing the low current external voltage sense input to the load, losses in the output line are compensated. Since the current in the sense line is very small, error introduced by its line resistance is negligible (Figure 41).



Figure 41. Proper Regulator Layout

Input Supply Design

When the power source is an ac voltage, the transformer, rectifier, and input filter design are as important as the regulator design itself for optimum system performances. This section presents input supply and filter design information for designing a basic capacitor input supply.

Transformer/Rectifier Configuration

The input supply consists of three basic sections: (1) input transformer, (2) rectifier, and (3) filter as illustrated in Figure 42. The first two sections, the transformer and the rectifier, are partially dependent upon each other because the structure of one depends upon that of the other. The most common transformer configurations and their associated rectifier circuits are illustrated in Figure 43.



Figure 42. Input Supply





(b) SINGLE-PHASE CENTER-TAPPED FULL-WAVE



(c) SINGLE-PHASE FULL-WAVE BRIDGE

Figure 43. Input Supply Transformer/Rectifier Configurations

The particular configuration used depends upon the application. The half-wave circuit [Figure 43(a)] is used in low-current applications. This is because the single rectifier diode experiences the total load current and its conversion efficiency is less than 50%. The full-wave configurations [Figure 43(b) and 43(c)] are used for higher current application. The characteristic output voltage waveforms of these configurations are illustrated in Figure 44.



Figure 44. Rectifier Output-Voltage Waveforms

Before the input supply and its associated filter can be designed, the voltage, current, and ripple requirements of its load must be fully defined. The load, as far as the input supply is concerned, is the regulator circuit. Therefore, the input requirements of the regulator itself become the governing conditions. Because the input requirements of the regulator control circuit govern the input supply and filter design, it is easiest to work backwards from the load to the transformer primary.

Capacitor Input Filter Design

The most practical approach to a capacitor-input filter design remains the graphical approach presented by O.H. Schade¹ in 1943. The curves illustrated in Figures 45 through 48 contain all of the design information required for full-wave and half-wave rectifier circuits.

Figures 45 and 46 illustrate the ratio of the dc-output voltage developed (V_C) to the applied peak input voltage (V_(PK), as a function of ω CR_L for half-wave and fullwave rectified signals, respectively. For a full-wave rectified application, the voltage reduction is less than 10% for ω CR_L > 10 and R_S/R_L < 0.5%. As illustrated, the voltage reduction decreases as ω CR_L increases or the R_S/R_L ratio decreases. Minimizing the reduction rate, contrary to initial impressions, may prove to be detrimental to the optimum circuit design. Further reduction requires a reduction in the series to load resistance ratio (R_S/R_L) for any given ω CR_L. This will result in a higher peak-to-average current ratio

¹O.H. Schade, "Analysis of Rectifier Operation", Proc. IRE., VOL. 31, 343, 1943.



Figure 45. Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Half-Wave Capacitor-Input Circuits (From O.H. Schade, Proc. IRE, Vol. 31, p. 343, 1943)



Figure 46. Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Full-Wave Capacitor-Input Circuits (From O.H. Schade, Proc. IRE, Vol. 31, p. 344, 1943)

through the rectifier diodes (see Figure 47). In addition, and probably of more concern, this increases the surge current experienced by the rectifier diodes during turn-on of the supply. It is important to realize that the surge current is limited only by the series resistance R_S .

$$I_{SURGE} = \frac{V_{SEC(PK)}}{R_S}$$

Design Considerations



Figure 47. Relation of RMS and Peak-to-Average Diode Current in Capacitor-Input Circuits (From O.H. Schade, Proc. IRE, Vol. 31, p. 345, 1943)

In order to control the surge current, additional resistance is often required in series with each rectifier. It is evident that a compromise must be made between the voltage reduction and the rectifier current ratings. The maximum instantaneous surge current is $V_{(pk)}/R_S$. The time constant (τ) of capacitor C is $\tau \cong R_SC$. As a rule of thumb, the surge current will not damage the diode if: ISURGE < IF(SURGE)max and τ < 8.3 ms

Figure 48 illustrates the relationships between the ripple factor r_f , ωCR_L , and R_S/R_L . The ripple factor is the ratio of the rms value of the ripple component of the output voltage, expressed as a percent of the nominal dc output voltage.





Design Considerations

4

Low Drop-Out Voltage Regulator Design Considerations

Low drop-out (LDO) regulators have increased in popularity during the past five years. This design consideration discusses the special requirements that LDO applications users should consider to obtain optimum operations.

The LDO regulator design is characterized by a large geometry PNP output transistor that is used to conduct the power from input to output. This configuration places the collector at the output while reducing the overhead voltage required to drive the output transistor. Since the output impedance of the collector is several thousand ohms, a high open loop gain must be maintained to reach the necessary M Ω requirements of a voltage regulator. In addition, the high-impedance collector reactive-load elements can introduce lowfrequency-phase shifts and control-loop instability. The LDO control loop is designed to accept a minimum capacitive loading (approximately 10 μ F) for complete stablization for the low-power LDO (TL750LXX series) regulators. The medium-power regulators TL750MXX series introduced additional requirements because of the wide range of restistive loading (5 Ω to infinity) that have resulted in a broad frequency swing in loopphase shift and restrictions in the value of the load capacitor. Some assumptions have been made on the range of the Equivalent Series Resistance (ESR) the load capacitor should exhibit in certain applications. The ESR would cancel the phase shift at some of the higher frequencies and allow the regulator design to have internal fixed-stability compensation. This compensation allows the load capacitor value to vary from the minimum to a greater than value. The assumed ESR is approximately 0.5 Ω (polarized solid tantalum to be used in this range) derived from studies of the ESR of the standard available capacitors at the minimum value. Actual response curves for the TL750MXX series are shown in Figure 49. To justify these assumptions, the following conditions must be stated:

- 1. The ESR of the capacitor is directly related to the application (wiring resistance of regulator and load increases the ESR).
- 2. The loop will become unstable if the ESR is forced too low.
- 3. The stability will improve with an increase in load-capacitor value.

Caution must be exercised in some medium-power LDO applications that require stable regulation over a large load range because mV-level oscillations may be exhibited at the higher load-resistance ranges. To eliminate the oscillations, a larger capacitor value (approximately $100-\mu$ F maximum) should be selected or the ESR value should be increased (to approximately 2 Ω). The circuit bandwidth is decreased by the larger value capacitor and the loop bandwidth is increased with the higher ESR. This provides a faster transient load response and offsets some of the loss from the capacitor ESR.



Figure 49. Typical Response Curves for the TL750MXX Series

Thermal Considerations in Design of Power Supplies

Introduction

Power supply circuit designers place emphasis on suppressing transients, improving regulation, and increasing efficiency, yet concentrate minimum effort toward thermal considerations and packaging of the power supply. Serious efforts must be given to thermal design and packaging to minimize power supply failures in the field. If sufficient attention is given to the important parameters supplied by the semiconductor manufacturers (e.g., maximum junction temperature, junction-to-case, and junction-to-ambient thermal resistance), proper heat removal can be achieved. Thermal resistance is the temperature difference between two points divided by the power dissipation, normally stated in °C/W. The reference temperature can be the ambient temperature or the temperature of a heat sink that the integrated circuit (IC) package is attached to.

Heat can be transferred from the transistor or integrated circuit package by three methods; conduction, convection, and radiation.

Conduction is transmission of energy by a medium not involving movement of the medium itself. This method is predominate in junction to the case or from the case to a heat sink heat transfer from the semiconductor. Length, cross-section, and temperature differential of the medium are key parameters that determine conduction.

Convection is transmission of energy or mass by a medium involving movement of the medium itself. This method predominates in the transfer of heat from the case to ambient or a heat sink to ambient. Surface conditions, convecting fluids, velocity, and temperature difference are dominant factors in convection.

Radiation is the emission and propagation of waves transmitting energy through space or some medium. This method is important in heat transfer from the cooling-fin surface of a heat sink. Thermal emissivity, surface-area, and temperature difference between radiating and adjacent mediums are key factors that determine radiation.

Basic Thermal Circuit and Symbols

Figure 50 illustrates the various heat flow paths, temperatures, and thermal resistances of a steady-state thermal model using a KC package with formed leads. A popular concept is to display this thermal model as a network of series resistors as shown on Figure 51, comparing the thermal circuit analogy to an electric circuit. Extending this Ohm's-law concept of this thermal circuit, temperature is analogus to voltage and thermal resistance to ohmic resistance. Inspection of Figure 51 will provide an expression for:

 $T_{J} = T_{A} + P_{D}(R_{\theta JC} + R_{\theta CS} + R_{\theta SA})$

or $TJ = TA + PD(R\theta JA)$ for a regulator without external heat sink

(1)

where

- $T_J =$ junction temperature in °C
- T_A = ambient air temperature in °C
- $R_{\theta JC}$ = thermal resistance, junction-to-case in °C/W
- $R_{\theta CS}$ = thermal resistance, case-to-heat sink °C/W
- $R_{\theta SA}$ = thermal resistance, heat sink-to-ambient in °C/W
- $R_{\theta JA}$ = thermal reaistance, junction to ambient °C/W
 - P_D = power dissipated by semiconductor device in W



Figure 50. Semiconductor Thermal Model

The junction-to-ambient thermal resistance $R_{\theta JA}$ can be expressed as a sum of thermal resistances listed below:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA}$$
(2)

Equation 2 is applicable only when an external heat sink is used. If only a mounting (internal) heat sink is used, or the device does not have a heat sink, the $R_{\theta JA}$ is equal to the $R_{\theta JA}$ specified on the product data sheet. $R_{\theta JC}$ normally will be given on the data sheet also, and the junction-to-case thermal resistance is a function of the material, and size of the package, die area and thickness, and integrity of the die bond to the case, lead frame, or chip carrier. $R_{\theta CS}$ depends on the package, heat-sink-interface (mounting of the regulator to the heat sink) area, and integrity of the contact surface. Typical values for $R_{\theta CS}$ for different packages are shown in Table 1.





PACKAGE	METAL TO METAL	METAL-TO-METAL WITH THERMAL COMPOUND	CONTACT WITH MICA WASHER AND THERMAL COMPOUND [†]
TO-3	0.52°C/W	0.14°C/W	0.36 °C/W
KC (TO-220)	1.1 °C/W	1.0°C/W	1.7°C/W

Table 1. R_{\u03c0CS} for Different Types of Packages and Mounting Conditions

[†]Typical values extracted from heat-sink manufacturer's curves

The $R_{\theta SA}$ found on the heat sink data sheets depends on the attributes of the heat sink and the ambient conditions. Convection and radiation are heat flow methods affecting the heat sink to ambient thermal resistance.

Typically, the ambient temperature (T_A), maximum junction temperature (T_J), power dissipation (P_D), thermal resistance from junction-to-case (R θ JC), and thermal resistance from junction to ambient air (R θ JA) are known. To ensure safe operations of any semiconductor, the device junction temperature must be maintained below the maximum value given on the product data sheet. As with any semiconductor component, these devices have thermal and electrical limitations that must be adhered to if desired performance and service time are to be achieved. In addition, improved reliability can be obtained by selecting conservative operating procedures and thermal ranges. Normally, the electrical and thermal characteristics are interrelated with the actual operating ranges that are heavily dependent on the component application.

Thermal Design Examples

The following examples are given to illustrate the design procedure in:

- 1. Ascertaining the maximum allowable power dissipation of a semiconductor device
- 2. Determining the maximum junction-to-ambient air temperature (T_Amax) using a mounting (internal) heat sink, or regulator without internal heat sink
- 3. Selecting an external heat sink by calculating the heat sink-to-ambient thermal resistance ($R_{\theta SA}$).

To ascertain the maximum allowable power dissipation of a semiconductor device, use equation 3:

$$P_{D} = \frac{T_{Jmax} - T_{A}}{R_{\theta}J_{A}}$$
(3)
$$P_{D} = \frac{150 \,^{\circ}\text{C} - 75 \,^{\circ}\text{C}}{121.95 \,^{\circ}\text{C/W}} = 0.62 \text{ W}$$

where

 $T_{Jmax} = 150 \text{ °C} \text{ (design limit)}$ $T_{A} = 75 \text{ °C}$ $R_{\theta JA} = 1/\text{derating value} = 1/8.2 \text{ mW/ °C} \text{ (DW package)} = 121.95 \text{ °C/W}$ $T_{Jmax} = T_{A} + P_{D}(R_{\theta JC} + R_{\theta CS} + R_{\theta SA})$

To ascertain the maximum T_A for an uA78M12C regulator with an internal heat sink, use equation 4:

$$T_{J} = T_{A} + P_{D}(R_{\theta JA})$$

$$T_{A} = T_{J} - P_{D}(R_{\theta JA})$$

$$T_{A} = 125 - (0.8 \times 62.5)$$

$$T_{A} = 75 ^{\circ}C$$

$$(4)$$

where

 $P_D = 0.8~W$ $T_J = 125~^{o}C$ $R_{\theta JA} = 1/derating factor = 1/0.016 = 62.5~^{o}C/W$ Derating factor of KC (TO-220) package is 16 mW/ ^{o}C (from uA78M12C data sheet)

To ascertain the heat sink-to-ambient thermal resistance ($R_{\theta}SA$) for selection of external heat sink using the uA7915C regulator, the heat sink should be mounted metal-to-metal using thermal compound.

$$R_{\theta SA} = \frac{T_{J} - T_{A}}{P_{D}} - R_{\theta JC} - R_{\theta CS}$$
(5)
$$R_{\theta SA} = \frac{125 - 75}{3} - 4 - 1 = 11.7 \,^{\circ}C/W$$

where

$$P_{D} = 3 W$$

$$T_{J} = 125 °C$$

$$T_{A} = 75 °C$$

$$R_{\theta JC} = 4 °C/W \text{ (from the uA7915C data sheet)}$$

$$R_{\theta CS} = 1 °C/W \text{ from Table 1 (KC or TO-220 case)}$$

$$R_{\theta JA} = \frac{T_{J} - T_{A}}{P_{D}} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA}$$

A Thermalloy 7019 or Staver V3-5 heat sink will meet the desired requirements (see Table 3).

$R_{\theta SA} RANGE^{\dagger}$	MANUFACTURER [‡]	
°C/W	STAVER	THERMALLOY
3 to 5	V3-5-2	6004,6053,6054,6214,6216
5 to 8	V2.2.2	6002, 6003, 6015, 6016,
5 10 8	V3-3-2	6052, 6060, 6061, 6213
8 to 13	V1-3,V1-5,V3-3,V3-5,V3-7-96	6001, 6013, 6014, 6051

Table 2. Available Heat Sinks for TO-3 Packages

[†]All values are typical as determined from characteristic curves received from manufacturers. [‡]This table is a representative of two heat sink manufacturers, many others are available.

R _{0SA} RANGE [†] °C/W	M	MANUFACTURER [‡]	
	STAVER	THERMALLOY	
3 to 5	V3-5-2	6072/6071	
5 to 8	V3-3-2	6072, 7021, 7025	
8 to 13	V3-3, V3-5	6021, 6030, 6032, 7019, 7020	

Table 3. Available Heat Sinks for KC (TO-220) Packages

[†]All values are typical as determined from characteristic curves received from manufacturers. [‡]This table is a representative of two heat sink manufacturers, many others are available.

General Suggestions for Efficient Thermal Management

Suggestions are as follows:

- 1. Place regulator components away from heat-dissipating components and mount hardware in an area that provides a good heat-dissipation path for the regulator.
- 2. For applications requiring electrical insulation of the heat-sink from the regulator use a thin (0.003 inch) mica washer. A thermal lubricant must be placed on both sides of the washer.
- 3. If a heat sink with fins is used with the regulator, align the fins in a vertical plane for a more efficient transfer of heat.
- 4. Select heat sink with a mounting surface that has a finish and flatness comparable to the regulator package. Use thermal compounds to minimize voids, scratches, and imperfections between the mating surfaces. Use of thermal compounds with an insulating washer is more significant than with a metal-to-metal contact.
- 5. Attach regulator heat sink to the regulator before soldering and mounting on the PC board. Maximum lead temperatures are 260 °C for ten seconds with plastic packages or 300 °C for sixty seconds for cermanic packages at a distance of 1/16th inches from case.

Conclusion

Thermal considerations in the design of power supplies are straight-forward, and with emphasis on heat reduction and conservative operating techniques, more efficient and reliable designs will be realized. The design parameters are normally under the control of the circuit designer and, with compromises, the variables can be controlled to achieve a product that will experience fewer failures in the field. On the other hand, if the thermal design considerations are overlooked or minimized, many of the power supply failures in the field may result from an inadequate thermal design approach.

Switching Power Supply Design

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Introduction

Modern electronic equipment usually requires one or more dc power sources. The usual method of supplying dc power is a power supply which converts ac power to dc power. The two types of dc power supplies in common use are classified by the type of regulator employed; linear regulator and switching regulator.

Linear power supplies consist of a power transformer, rectifier and filter circuits, and a linear regulator. Switching power supplies do not require line transformers; the ac input is rectified and filtered, chopped by a high frequency transistor switch/transformer combination, then rectified and filtered again.

Switching power supplies have been used for some time in the military and space industry due to their smaller size and higher efficiency. In 1975, switching power supplies were more cost effective than linear power supplies from approximately the 500-W power level. Now the breakeven point is down to approximately 5 W.

Basic Operation of Switching Regulators

Figure 1 is a block diagram of a typical switching power supply which consists of four basic circuits:

- 1. Input rectifier and filter
- 2. High frequency inverter
- 3. Output rectifier and filter
- 4. Control circuit.

The ac line voltage is applied to an input rectifier and filter circuit. The dc voltage output from the rectifier and filter circuit is switched to a higher frequency (typically 25 kHz to 100 kHz) by the transistor switch in the high frequency inverter circuit. This circuit contains either a high frequency transformer or inductor, depending on the output voltage required.

Output from the high frequency inverter circuit is applied to the output rectifier and filter circuit. The circuit is monitored and controlled by the control circuit which attempts to keep the output at a constant level.



Figure 1. Basic Switching Regulator Block Diagram

The control circuit consists of an oscillator driving a pulse-width modulator, an error amplifier, and a precision voltage reference. The error amplifier compares the input reference voltage with a sample of the voltage from the output rectifier and filter circuit. As the load increases, the output voltage drops. The error amplifier senses this drop and causes the pulse-width modulator to remain on for a longer period of time, delivering wider control pulses to the transistor switch.

The width of the pulse determines how long the transistor switch allows current to flow through the high frequency transformer and, ultimately, how much voltage is available at the output. If the load decreases, narrower control pulses are delivered to the switching transistor until the output voltage remains at a constant value.

Advantages of a Switching Regulator

The primary advantages of switching regulators are higher efficiency and smaller size. Conventional linear series and shunt regulators operate in a continuous conduction mode, dissipating relatively large amounts of power. The efficiency of linear regulators is typically around 40% to 50%. When the input-to-output voltage differential is large, the resultant efficiency is much lower than 40%.

Switching regulators have typical efficiencies of 60% to 90%; much higher than either the linear series or shunt regulator. Switching regulators achieve their higher efficiency as a result of three factors:

- 1. The power-transistor switch is always turned completely on or off, except when it is switching between these two states, resulting in either low voltage or low current during most of its operation.
- 2. Good regulation can be achieved over a wide range of input voltage.
- 3. High efficiency can be maintained over wide ranges in load current.

Switching regulators use the on-off duty cycle of the transistor switch to regulate the output voltage and current. By using a frequency much higher than the line frequency (typically 20 kHz to 500 kHz), the transformers, chokes, capacitors, and other filter elements can be made smaller, lighter, and less costly. The smaller elements used in switching regulators result in smaller power losses than the larger components used in linear regulators. The highest cost elements of a switching power supply are the transistor switches. The remaining costs, in descending order, are due to the magnetic components, capacitors, and rectifiers.

Disadvantages of a Switching Regulator

Switching regulators can generate some electromagnetic and radio frequency interference (EMI/RFI) noise due to high switching currents and short rise and fall times. EMI/RFI noise, which is generated at higher frequencies (100 kHz to 500 kHz), is easily filtered. In those applications where a large series impedance appears between the supply and the regulator, the rapid changes in current also generate a certain amount of noise. These problems may be overcome or significantly reduced by one or more of the following steps:

- 1. Reducing the series impedance
- 2. Increasing the switching time
- 3. Filtering the input and output of the regulator.

Switching regulators with a fixed frequency are easier to filter than regulators with a variable frequency because the noise is at only one frequency. Variable frequency regulators with a fixed "on" time increase or decrease the switching frequency in proportion to load changes, presenting a more difficult filtering problem.

Basic Switching Regulator Architecture

There are three basic switching regulator configurations from which the majority of present day circuits are derived:

- 1. Step-down or "buck" regulator
- 2. Step-up or "boost" regulator
- 3. Inverting or "flyback" regulator (which is a variation of the "boost" regulator).

The Step-Down Regulator

Figure 2 illustrates the basic step-down or "buck" regulator. The output voltage of this configuration is always less than the input voltage. In the buck circuit, a semiconductor switch is placed in series with the dc input from the input rectifier/filter circuit. The switch interrupts the dc input voltage providing a variable-width pulse to a simple averaging LC filter. When the switch is closed, the dc input voltage is applied across the filter and current flows through the inductor to the load. When the switch is open, the energy stored in the field of the inductor maintains the current through the load. In the buck circuit, peak-switching current is proportional to the load current. The output voltage is equal to the input voltage times the duty cycle.

$$V_{O} = V_{I} \times Duty Cycle$$



Figure 2. Step-Down or "Buck" Switching Regulator Circuit

The Step-Up Regulator

Another basic switching regulator configuration is the step-up or "boost" regulator (Figure 3). In this type of circuit, the output voltage is always greater than the input voltage. The boost circuit first stores energy in the inductor and then delivers this stored energy along with the energy from the dc input voltage to the load. When the switch is closed, current flows through the inductor and the switch, charging the inductor but delivering no current to the load. When the switch is open, the voltage across the load equals the dc input voltage plus the charge stored in the inductor. The inductor discharges, delivering current to the load.


Figure 3. Step-Up or "Boost" Switching Regulator Circuit

The peak switching current in the boost circuit is not related to the load current. The power output of a boost regulator can be determined by the following equation:

$$P_{OUT} = \frac{LI^2f}{2}$$

where:

 P_{OUT} = power output L = inductance I = peak current f = operating frequency

The Inverting Regulator

The third switching regulator configuration is the inverting or "flyback" regulator. This circuit is a variation of the step-up or "boost" circuit discussed previously. The flyback circuit is illustrated in Figure 4. Flyback regulators, which evolved from "boost" regulators, deliver only the energy stored by the inductor to the load. This type of circuit can step the input voltage up or down. When the switch is closed, the inductor is charged, but no current is delivered to the load because the diode is reverse biased. When the switch is open, the blocking diode is forward biased and the energy stored in the inductor is transferred through it to the load.



Figure 4. Inverting or "Flyback" Switching Regulator Circuit

The flyback circuit delivers a fixed amount of power to the load regardless of load impedance. It is widely used in photo flash, capacitor-discharge ignition circuits, and battery chargers.

To determine the output voltage of an electronic equipment supply, the load (R_L) must be known. If the load is known, the output voltage may be calculated using the following equation:

$$V_{O} = \sqrt{P_{O}R_{L}} = I \sqrt{\frac{LfR_{L}}{2}}$$

where:

 V_O = voltage output P_O = power out R_L = load resistance I = inductor current f = operating frequency

The inductor current is proportional to the "on time" (duty cycle) of the switch and regulation is achieved by varying the duty cycle. However, the output also depends on the load resistance (which was not true with the step-down circuit).

Transient response to abrupt changes in the load is difficult to analyze. Practical solutions include limiting the minimum load and using the proper amount of filter capacitance to give the regulator time to respond to this change. Flyback type circuits are used at power levels of up to 100 W.

Forward Converters

The forward converter family, which includes the push-pull and half-bridge circuits, evolved from the step-down or "buck" type of regulator. A typical forward converter circuit is illustrated in Figure 5. When the transistor switch is turned on, the transformer delivers power to the load through diode D1 and the LC filter. When the switch is turned off, diode D2 is forward biased and maintains current to the load.

Without the third winding and diode D3, the converter would lose efficiency at higher frequencies. The function of this winding is to return energy stored in the transformer to the line and reset the transformer core after each cycle of operation. This is a popular low-power (up to about 200 W) converter and is almost immune to transformer saturation problems.





Push-Pull Converter

The push-pull converter is probably one of the oldest switching regulator type circuits. It was first used in the 1930s with mechanical vibrators functioning as the switch. When transistors became available, push-pull converters were used as free-running oscillators in the primary of many automobile communication converters. Some recreational vehicles still use this free-running type of oscillator converter in dc-to-dc converters as well as in dc-to-ac inverters. A typical push-pull converter circuit is shown in Figure 6.



Figure 6. Basic Push-Pull Converter Circuit

Half-Bridge Converter

The most popular type of high-power converter is the half-bridge circuit illustrated in Figure 7. The half-bridge converter has several advantages over the push-pull circuit. First, the midpoint between the capacitors (point A) can be charged to $V_I/2$. This allows the use of transistors with lower breakdown voltage. Second, because the primary is driven in both directions (push-pull), a full-wave rectifier and filter are used which allows the transformer core to be more effectively utilized.



Figure 7. Half-Bridge Converter Circuit

Full-Bridge Converter

In contrast to the half-bridge, the full-bridge (or H-Bridge) converter uses four transistors as shown in Figure 8. In a full-bridge circuit, the diagonally opposite transistors (Q1/Q2 or Q3/Q4) are turned on during alternate half cycles. The highest voltage any transistor is subjected to is V_I , rather than $2 \times V_I$ as is the case in the push-pull converter circuit. The full-bridge circuit offers increased reliability because less voltage and current stress is placed on the transistors. The disadvantage of this circuit is the space required by the four transistors and the cost of the two additional transistors.



Figure 8. Full-Bridge Converter Circuit

TL493 Floppy Disk Power Supply

The TL493 incorporates, on a single monolithic chip, all the functions required for a pulse-width modulation control circuit. The TL493 is similar to the TL594, from which it was derived, except that the TL493 includes a current-limit amplifier instead of a seconderror amplifier.

The current-limit amplifier of the TL493 has an offset voltage of approximately 80 mV in series with the inverting input (pin 15). This makes it easier to design the current-limit portion of the power supply and also requires fewer components. With 80 mV on the inverting input, it is only necessary to apply an 80-mV control voltage to the noninverting input (pin 16). This is easily accomplished by taking the voltage across a resistor in series with the load.

The floppy disk power supply schematic is shown in Figure 9. The power supply uses a pair of TIP34 p-n-p transistors in a push-pull configuration. The oscillation frequency is set at 25 kHz and -5 V at 500 mA by the .01- μ F capacitor on pin 5 and the 5-k Ω resistor on pin 6.



Figure 9. TL493 Floppy Disk Power Supply

The center connection of the two 5.6-k Ω resistors on pins 13 and 14 establishes a 2.5-V reference voltage on pin 2, which is the inverting input of the voltage control error amplifier. The voltage feedback to pin 1, the noninverting input, comes from the center connection of the two 5.6-k Ω resistors located on the 5-V/2.5-A power supply output terminal. Because this voltage supplies the logic circuits, it requires closer regulation.

The 24-V winding, on the other hand, is not critical as it furnishes voltage for the stepping motor. The -5-V supply is regulated separately with a uA7905 three-terminal regulator. In choosing components for this circuit, the same precautions taken in the construction of any switching power supply should be observed; be careful of layout, ground loops, and heatsinking of the power transistors. In the output section, where high-frequency rectifiers are needed, either Schottky or fast recovery diodes should be used. For output capacitors, low equivalent series resistance (ESR) types should be considered. The output ripple depends more on this resistance than on the capacitor value.

Transformer Construction

The transformer for this circuit was wound on a toroid core. The core used was 3C8 ferrite material (F-42908-TC). The winding layout is shown in Figure 10.

$$20 V$$

$$1 \xrightarrow{A}$$

$$20 V$$

$$2 \xrightarrow{B}$$

$$3 \xrightarrow{B}$$

$$\frac{C}{5} \xrightarrow{4}$$

$$5 \xrightarrow{6}$$

$$26 VDC @ 2.5 A$$

$$\frac{E}{F} \xrightarrow{7} \xrightarrow{9}$$

$$6 VDC @ 2.5 A$$

$$\frac{G}{H} \xrightarrow{11} \xrightarrow{9} VDC @ 0.5 A$$



Transformer Winding Data

Primary A + B = 20 turns bifilar #20 HNP Secondary C + D = 28 turns bifilar #20 HNP over A + B Secondary E + F = 6 turns bifilar #20 HNP over C+D Secondary G + H = 10 turns bifilar #26 HNP over E+F NOTE: All windings to be center tapped.

DC Resistance

Winding $1 - 3 = 0.11 \Omega$ Winding $4 - 6 = 0.11 \Omega$ Winding $7 - 9 = 0.025 \Omega$ Winding $10 - 12 = 0.15 \Omega$

TL594 12-V to 5-V Step-Down Regulator

The TL594 switching voltage regulator operates as a step-down converter in a discontinuous mode. When the output current falls below a specified minimum value, the inductor current becomes discontinuous. The advantages of a step-down converter in this mode of operation are:

- 1. The ripple voltage at the output can be kept low, even in high-current designs.
- 2. The ratio of peak current in the switching device to output current is determined by the inductor value and is typically low. For a specific output current requirement, the current rating for the switching transistor can be lower than for a transistor operating in a continuous mode.
- 3. Pulse-width modulation occurs with input voltage variations. Load variations are compensated for by modulation of the dc current level in the inductor, as well as by pulse-width modulation. This allows high efficiency to be maintained over the entire load range (from I_0 max to I_0 min).

The disadvantages of this type of converter are:

- 1. The size of the inductor used may result in a high-inductance value.
- 2. Transient response is impaired by high-inductance values.
- 3. Although peak current in the rectifier is reduced, losses due to reverse recovery current are increased.

The complete circuit for the TL594 step-down regulator is shown in Figure 11. For this application, the two switching transistors operate in phase with each other by grounding the output control, pin 13. The switching transistors supply input to the inductor, L for part of the oscillator cycle. For the remaining part of the oscillator cycle, the voltage across the inductor reverses and diode D1 starts conducting, maintaining current flow in the inductor while the transistors are off (see Figure 12).



Figure 12. 12-V to 5-V Series Switching Regulator Waveforms

The input supply through R1 to pin 12 is decoupled by capacitor C2. Capacitor C4 filters the output voltage. The timing components C3 and R6 set the oscillator frequency to 15 kHz. The 2.2-mH inductor can be made on an RM7 ferrite core with 94 turns of #28 transformer wire.

Output-current limiting of 500 mA is provided by sensing the overcurrent level with R11 and feeding the resultant error voltage to the positive input of the current error amplifier on pin 16. The negative input to this error amplifier is biased to 500 mV from reference divider R2, R3, and R4. This resistor network also furnishes about 2.3-V bias to the voltage control error amplifier. An output error voltage signal is taken from the junction of R7 and R8 and fed to the positive input of the voltage control error amplifier. The voltage control loop gain is set by feedback resistor R5.

Specifications

Input Voltage	12 V nominal (10 V to 15 V)
Output Voltage	$5 \text{ V} \pm 10\%$
Output Ripple	50 mV _{pp}
Output Current	400 mA
Output Power	2 W at 5-V output
Short Circuit Protection	500-mA constant current
Efficiency	typically 70%

The TL594 Control Circuit

The TL594 is a fixed frequency pulse-width-modulation control for switching power supplies and voltage converters. The TL594 includes an adjustable oscillator, a pulse-width modulator, and an error amplifier. Additional functions include over-current detection, independent dead-time control, a precision 5-V reference regulator, and output control logic which allows single-ended or push-pull operation of the two switching transistors. Figure 13 shows a block diagram of the TL594.

Modulation of the output pulses is accomplished by comparing the sawtooth waveform created by the internal oscillator on timing capacitor C_T to either of two control signals. The output stage is enabled when the sawtooth voltage is greater than the voltage of the control signal. See Figure 14. As the control signals increase, the output pulse width decreases. The control signals are derived from two sources: the dead-time control and the error amplifiers. The dead-time comparator has a fixed offset of 10 mV which provides a preset dead time of about 5%. This is the minimum dead time that can be programmed with pin 4 grounded.



PIN ASSIGNMENT

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1.	ERROR AMP. 1, NONINVERTING INPUT	9.	DRIVE TRANSISTOR 1, EMITTER
2.	ERROR AMP. 1, INVERTING INPUT	10.	DRIVE TRANSISTOR 2, EMITTER
3.	COMPENSATION INPUT	11.	DRIVE TRANSISTOR 2, COLLECTOR
4.	DEAD TIME CONTROL INPUT	12.	INPUT SUPPLY
5.	OSCILLATOR TIMING CAPACITOR	13.	OUTPUT MODE CONTROL
6.	OSCILLATOR TIMING RESISTOR	14.	STABILIZED REFERENCE VOLTAGE
7.	GROUND	15.	ERROR AMP 2, INVERTING INPUT
8.	DRIVE TRANSISTOR 1, COLLECTOR	16.	ERROR AMP 2, NONINVERTING INPUT

Figure 13. TL594 Block Diagram



PWM CONTROL RANGE, PIN 3

RESULTANT OUTPUT PULSE WITH PIN 3 VOLTAGE AS ABOVE PIN 13 WIRED FOR SINGLE ENDED OPERATION

Figure 14. Output Pulses vs Sawtooth Control Voltage

Design Considerations

The pulse-width-modulation (PWM) comparator generates the control difference signal created by the input from either of the error amplifiers. One error amplifier is used to monitor the output voltage and provide a change in control signal voltage. The other error amplifier monitors the output current and its change in control voltage provides current limiting.

Reference Regulator

The internal 5-V reference at pin 14 provides a stable reference for the control logic, pulse-steering flip-flop, oscillator, dead-time-control comparator and pulse-width-modulation circuitry. It is a band-gap circuit with short circuit protection and is internally programmed to an accuracy of $\pm 5\%$.

Oscillator

The internal oscillator provides a positive sawtooth waveform to the dead-time and PWM comparators for comparison with the various control signals. The oscillator frequency is set by an external timing capacitor and resistor on pins 5 and 6. The oscillator frequency is determined by the equation:

$$f_{OSC} = \frac{1}{R_T C_T}$$
 (single-ended applications)

The oscillator frequency is equal to the output frequency only for single-ended applications. The output frequency for push-pull applications is one-half the oscillator frequency as shown by the equation:

$$f_{OSC} = \frac{1}{2 R_T C_T}$$
 (push-pull applications)

There is a frequency variation of $\pm 5\%$ between devices due to internal component tolerances. The oscillator charges the external timing capacitor, C_T , with a constant current which is determined by the external timing resistor, R_T . This circuit produces a linear ramp voltage waveform. When the voltage across the timing capacitor reaches 3 V, the circuit discharges and the charging cycle is initiated again.

Dead-Time and PWM Comparators

Both the dead-time and PWM comparator functions use a single logic comparator with parallel input stages. The comparator output is a pulse-width-modulated signal, whose width is determined by comparison with the oscillator ramp waveform. The comparator outputs drive the output control logic. A fixed 100-mV offset voltage input to the dead-time comparator allows a minimum dead time between output pulses to be maintained when the dead-time control input (pin 4) is grounded (Figure 15).



OSCILLATOR RAMP, PIN 5

MAXIMUM OUTPUT PULSE WIDTH SINGLE ENDED OPERATION, PIN 4 = 0 V

Figure 15. Deadtime Comparator Operation

The full range of pulse-width control (0% - 90%) is available when the dead-time control voltage (pin 4) is between 3.3 V and 0 V. The relationship between control voltage and maximum output pulse width is essentially linear. A typical application for this may be in a push-pull converter circuit where overlap of the conduction times of power transistors must be avoided.

The PWM comparator input is coupled internally to the outputs of the two error amplifiers. This input is accessible on pin 3 for control loop compensation. The output pulse width varies from 90% of the period to zero as the voltage present at pin 3 varies from 0.5 V to 4.5 V (Figure 14).

Error Amplifiers

Both error amplifiers are high-gain amplifiers which operate as single-ended, single-supply amplifiers, in that each output is active high only. This allows each amplifier to pull up independently for a decreasing output pulse-width demand. With the outputs ORed together, the amplifier with the higher output level dominates. The open-loop gain of these amplifiers is 60 dB. Both error amplifiers exhibit a response time of about 400 ns from their inputs to their outputs on pin 3. Figure 16 shows the amplifier transfer characteristics and a Bode plot of the gain curves.

Output Logic Control

The output control logic interfaces the pulse-width modulator to the output stages. In the single-ended mode (both outputs conducting simultaneously), the pulse-width-modulated signal is gated through to both output stages when the output control (pin 13) is connected to ground.



AMPLIFIER TRANSFER CHARACTERISTICS



Figure 16. Amplifier Performance Curves

For push-pull operation (each output stage conducting alternately), the output control (pin 13) is connected to the internal reference voltage (pin 14) enabling the pulse steering flip-flop. The flip-flop is toggled on the trailing edge of the pulse-width-modulated signal gating it to each of the outputs alternately; therefore, the switching frequency of each output is one-half the oscillator frequency. The output control (pin 13) must never be left open. It may be connected to the internal voltage reference (pin 14) or ground (pin 7).

The Output Driver Stages

The two identical Darlington output drivers may be operated in parallel or push-pull mode. Both the collector and emitter terminals are available for various drive configurations. $V_{CE(sat)}$ of each output at 200 mA is typically 1.1 V in common-emitter configuration and 1.5 V in common-collector configuration. These drivers are protected against overload but do not have sufficient current limiting to be operated as current source outputs.

Soft Start

Use of a soft-start protection circuit is recommended. This circuit prevents current surges during power-up and protects against false signals which might be created by the control circuit when power is applied. Implementing a soft-start circuit is relatively simple using the dead-time control input (pin 4). Figure 17 shows an example.

Initially, capacitor C_S forces the dead-time control input to follow the internal 5-V reference which disables both outputs (100% dead time). As the capacitor charges through R_S , the output pulse width increases until the control loop takes command.



Figure 17. Soft-Start Circuit

Overvoltage Protection

The dead-time control input (pin 4) also provides a convenient input for over-voltage protection, which may be sensed as an output voltage condition, or input voltage protection as shown in Figure 18.



Figure 18. Overvoltage Protection Circuit

A TL431 is used as the sensing element. When the monitored supply rail voltage increases to the point that 2.5 V is developed across R2, the TL431 conducts, Q1 becomes forward biased, and the dead-time control is pulled up to the reference voltage which disables the output transistors.

Designing a Power Supply 5-V/10-A Output

Design Objective

This design uses the TL594 integrated circuit based on the following parameters:

Input Power Source

The 32-V dc-power source for this supply uses a 120-V input, 24-V output transformer rated at 75 VA. The 24-V secondary winding feeds a full-wave bridge rectifier followed by a $0.3-\Omega$ current limit resistor and two filter capacitors, as shown in Figure 19.



Figure 19. Input Power Source

The output current and voltage are determined by the following equations.

V rectifier = V secondary $\times \sqrt{2}$ = 24 V $\times \sqrt{2}$ = 34 V

I rectifier(avg)
$$\approx \left(\frac{V_{O}}{V_{I}}\right) \times I_{O} \approx \frac{5 \text{ V}}{32 \text{ V}} \times 10 \text{ A} \approx 1.6 \text{ A}$$

The 3-A/50-V full-wave bridge rectifier meets these calculated conditions. Figure 20 illustrates the switching and control section.

TL494 50 WATT POWER SUPPLY[5 V @ 10A OUTPUT]



Figure 20. Switching and Control Section

Control Circuits

Oscillator

The TL594 oscillator frequency is controlled by connecting an external timing circuit consisting of a capacitor and resistor to pins 5 and 6. The oscillator is set to operate at 20 kHz using the component values calculated by the following equations.

$$f = \frac{1}{R_T C_T}$$

Design Considerations

where:

 $\begin{array}{rcl} R_T &= & \text{Value of timing resistor} \\ C_T &= & \text{Value of timing capacitor} \\ \text{Choose } C_T &= & 0.001 \ \mu\text{F} \ \text{and calculate } R_T. \\ R_T &= & \frac{1}{f \ \times \ C_T} \ = \ \frac{1}{20 \ \times \ 10^3 \ \times \ 0.001 \ \times \ 10^{-6}} \ = \ 50 \ \text{k}\Omega \end{array}$

Error Amplifier

The error amplifier compares a sample of the 5-V output to a reference and adjusts the pulse-width modulator to maintain a constant output as shown in Figure 21. The TL594's internal 5-V reference (pin 14) is divided to 2.5 V by R3 and R4. The output voltage error signal is also divided to 2.5 V by R8 and R9. If the output must be regulated to exactly 5 V, a 10-k Ω potentiometer may be used in place of R8 to provide an adjustment control. To increase the stability of the error amplifier circuit, the output of the error amplifier is fed back to the inverting input through R7, reducing the gain to 100.



Figure 21. Error Amplifier Section

Current Limit Amplifier

The power supply was designed for a 10-A load current and an I_L swing of 1.5 A; therefore, the short circuit current should be

$$I_{SC} = I_O + \frac{I_L}{2} = 10.75 \text{ A}$$

The current limit portion of the circuit is shown in Figure 22. Resistors R1 and R2 set a reference of about 1 V on the inverting input of the current limit amplifier. Resistor R11, in series with the load, applies 1 V to the noninverting terminal of the current limit

amplifier when the load current reaches 10 A. The output-pulse width will be reduced accordingly. The value of R11 is calculated as follows:



Figure 22. Current Limit Circuit

Soft Start and Dead Time

To reduce stress on the switching transistors at startup, the startup surge which occurs as the output filter capacitor charges must be reduced. The availability of the dead-time control makes implementation of a soft-start circuit, as shown in Figure 23, relatively simple.

The "soft-start" circuit allows the pulse width at the output to increase slowly, as shown in Figure 23, by applying a negative slope waveform to the dead-time control input (pin 4). Initially, capacitor C2 forces the dead-time control input to follow the 5-V reference regulator, which disables the outputs (100% dead time). As the capacitor charges through R6, the output-pulse width slowly increases until the control loop takes command. With a resistor ratio of 1:10 for R6 and R7, the voltage at pin 4 after startup will be 0.1×5 V or 0.5 V.

The soft-start time is generally in the range of 25 to 100 clock cycles. If we select 50 clock cycles at a 20-kHz switching rate, the soft-start time is calculated as follows:

$$T = \frac{1}{f} = \frac{1}{20 \text{ kHz}} = 50 \text{ }\mu\text{s} \text{ per clock cycle}$$

The value of the capacitor is then determined by

C2 =
$$\frac{\text{soft start time}}{\text{R6}} = \frac{50 \ \mu\text{s} \times 50 \ \text{cycles}}{1 \ \text{k}\Omega} = 2.5 \ \mu\text{F}$$

This helps to eliminate any false signals which might be created by the control circuit as power is applied.



Figure 23. Soft-Start Circuit

Inductor Calculations

The switching circuit used is shown in Figure 24. The size of the inductor (L) required is calculated as follows:

d = Duty Cycle =
$$\frac{V_O}{V_I} = \frac{5 V}{32 V} = 0.156$$

f = 20 kHz (Design Objective)

Design Considerations

$$t_{on} = \text{time on } (S1 \text{ closed}) = \frac{1}{f} \times d = 7.8 \text{ } \mu\text{s}$$

$$t_{off} = \text{time off } (S1 \text{ open}) = \frac{1}{f} - t_{on} = 42.2 \text{ } \mu\text{s}$$

$$L \approx \frac{(V_I - V_O) \times t_{on}}{\Delta IL} \approx \frac{(32 \text{ } V - 5 \text{ } V) \times 7.8 \text{ } \mu\text{s}}{1.5 \text{ } A} \approx 140.4 \text{ } \mu\text{H}$$

$$L \approx 140 \text{ } \mu\text{H}$$



Figure 24. Switching Circuit

Output Capacitance Calculations

Once the filter inductance has been calculated, the value of the output filter capacitor is calculated to meet the output ripple requirements. An electrolytic capacitor can be modeled as a series connection of an inductance, a resistance, and a capacitance. To provide good filtering, the ripple frequency must be far below the frequencies at which the series inductance becomes important; so, the two components of interest are the capacitance and the effective series resistance (ESR). The maximum ESR is calculated according to the relation between the specified peak-to-peak ripple voltage and peak-topeak ripple current.

$$\text{ESR(max)} = \frac{\Delta V_{O} \text{ (ripple)}}{\Delta I_{L}} = \frac{0.1 \text{ V}}{1.5 \text{ A}} = 0.067 \Omega$$

The minimum capacitance of C3 necessary to maintain the V_0 ripple voltage at less than the 100-mV design objective was calculated according to the following equation.

C3 =
$$\frac{\Delta I_L}{8 f \Delta V_O} = \frac{1.5 \text{ A}}{8 \times 20 \times 10^3 \times 0.1 \text{ V}} = 94 \mu \text{F}$$

A 220- μ F, 60-V capacitor is selected because it has a maximum ESR of 0.074 Ω and a maximum ripple current of 2.8 A.

Transistor Power Switch Calculations

The transistor power switch was constructed with a TIP30 p-n-p drive transistor and a TIP73 n-p-n output transistor. These two power devices were connected in a p-n-p hybrid Darlington circuit configuration as shown in Figure 25. The hybrid Darlington must be saturated at a maximum output current of I_O + Δ I_L/2 or 10.8 A. The Darlington h_{FE} at 10.8 A must be high enough not to exceed the 250-mA maximum output collector current of the TL594. Based on published TIP30 and TIP73 h_{FE} specifications, the required power switch minimum drive was calculated by the following equations to be 108 mA.

 $h_{FE}(Q1)$ at I_C of 1.2 A = 10

 $h_{FE}(Q2)$ at I_C of 12.0 A = 10

$$i_{B} \ge \frac{I_{O} + \frac{\Delta I_{L}}{2}}{h_{FE}(Q2) \times h_{FE}(Q1)} \ge 108 \text{ mA}$$

The value of R10 was calculated by the following equation.

 $R10 \leq \frac{V_{I} - (V_{BE}(Q1) + V_{CE}(TL594))}{i_{B}} = \frac{32 - (1.3 + 0.7)}{0.108}$

R10 \leq 277 Ω



Figure 25. Power Switch Section

Used on these calculations, the nearest standard resistor value of 270 Ω was selected for R10. Resistors R11 and R12 permit the discharge of carriers in the switching transistors when they are turned off. The power supply described demonstrates the flexibility of the TL594 pulse-width-modulation control circuit. This power supply design demonstrates many of the power supply control methods provided by the TL594 as well as the versatility of the control circuit.

TL497A Switching Voltage Regulator

The TL497A is a fixed-on-time, variable-frequency voltage regulator controller. The block diagram of the TL497A is shown in Figure 26. The on-time is controlled by an external capacitor connected between the frequency control pin (pin 3) and ground. This capacitor, C_T , is charged by an internal constant-current generator to a predetermined threshold. The charging current and threshold vary proportionately with V_{CC} ; thus, the on-time remains constant over the allowable input voltage range.



[†]The Base pin (#11) and Base Drive pin (#12) are used for device testing only. They are not normally used in circuit applications of the device.

Figure 26. TL497A Block Diagram

The output voltage is controlled by two series resistors in parallel with the supply output. The resistance ratios are calculated to supply 1.2 V to the comparator input (pin 1) at the desired output voltage. This feedback voltage is compared to the 1.2-V bandgap reference by the high-gain error amplifier. When the output voltage falls below the desired voltage, the error amplifier enables the oscillator circuit, which charges and discharges C_T .

The n-p-n output transistor is driven "on" during the charging cycle of C_T . The internal transistor can switch currents up to 500 mA. It is current driven to allow operation

from either the positive supply voltage or ground. An internal diode matched to the current characteristics of the output transistor is included on the chip and may be used for blocking or commutating purposes.

The TL497A also contains current-limiting circuitry which senses the peak currents in the switching regulator and protects the inductor against saturation and the output transistor against overstress. The current limit is adjustable and is set by a single-sense resistor between pins 13 and 14. The current-limit circuitry is activated when 0.5 V is developed across current-limit resistor R_{CL} .



Figure 27. Basic Power Supply Configurations

Design Considerations

The TL497A contains all the active elements required for constructing a singleended dc-to-dc converter. The output transistor and the rectifier are uncommitted allowing maximum flexibility in the choice of circuit configuration. The TL497A's primary feature is design simplicity. Using six external components; three resistors, two capacitors, and one inductor, the step-up, step-down, and inverting power supplies shown in Figure 27 may be constructed.

STEP-DOWN	STEP-UP	INVERTING
$POS \rightarrow POS$	$POS \rightarrow POS$	$POS \rightarrow NEG$
$+ V_{I} > + V_{O}$	$+V_{\rm O}>+V_{\rm I}$	$+V_{I} > -V_{O}$

Step-Down Switching Regulator

The circuit in Figure 28(a) illustrates the basic configuration for a step-down switching regulator. When switch S1 is closed, the current in the inductor and the voltage across the capacitor start to build up. The current increases while switch S1 is closed as shown by the inductor waveform in Figure 28(b). The peak current in the inductor is dependent on the time S1 is closed (t_{on}) .

When S1 opens, the current through the inductor is I_{pk} . Since the current cannot change instantaneously, the voltage across the inductor inverts, and the blocking diode (D1) is forward biased providing a current path for the discharge of the inductor into the load and filter capacitor. The inductor current discharges linearly as illustrated in Figure 28(b).



Figure 28. Step-Down Switching Regulator

For the output voltage to remain constant, the net charge delivered to the filter capacitor must be zero. The charge delivered to the capacitor from the inductor must be dissipated in the load. Since the charge developed in the inductor is fixed (constant on-time), the time required for the load to dissipate that charge will vary with the load requirements. It is important to use a filter capacitor with minimal ESR. Note, however, some ripple voltage is required for proper operation of the regulator. Figure 29 shows a positive, step-down configuration both with and without an external pass transistor. Design equations for calculating the external components are included.





Step-Up Switching Regulator

In the step-up regulator, the formulas change slightly. During the charging cycle (S1 closed), the inductor (L) is charged directly by the input potential. The peak current is not related to the load current as it was in the step-down regulator because, during the inductor charge cycle, the blocking diode D1 is reverse biased and no charge is delivered to the load.

The circuit in Figure 30(a) delivers power to the load only during the discharge cycle of the inductor (S1 open). The diode (D1) is forward biased and the inductor discharges into the load capacitor. Figure 31 shows a positive, step-down configuration both with and without an external pass transistor. Design equations are included.



Figure 30. Step-Up Switching Regulator

Inverting Configuration

The inverting regulator is similar to the step-up regulator. During the charging cycle of the inductor, the load is isolated from the input. The only difference is in the potential across the inductor during its discharge. This can best be demonstrated by a review of the basic inverting regulator circuit (Figure 32).

During the charging cycle (S1 closed), the inductor (L) is charged only by the input potential, similar to the step-up configuration. In the inverting configuration, the input provides no contribution to the load current during the charging cycle. The maximum load current for discontinuous operation will be limited by the peak current, as observed in the step-up configuration. The inductor current waveform looks identical to the waveform demonstrated in the step-up configuration [see Figure 30(b)].

Figure 33 shows the inverting applications both with and without an external pass transistor. Design equations are also included. Note that in the inverting configuration, the internal diode is not used. An external diode must be used because pin 4 (substrate) must be the most negative point on the chip. The cathode of the internal diode is also the cathode of a diode connected to the substrate. When the cathodes are at the most negative voltage in the circuit, there will be conduction to the substrate resulting in unstable operation.



Figure 31. Positive Regulator, Step-Up Configurations



Figure 32. Basic Inverting Regulator Circuit

Design Considerations

An oscilloscope is required when building a switching regulator. When checking the oscillator ramp on pin 3, the oscilloscope may be difficult to synchronize. This is a normal operating characteristic of this regulator and is caused by the asynchronous operation of the error amplifier to that of the oscillator. The oscilloscope may be synchronized by varying the input voltage or load current slightly from design nominals.

High frequency circuit layout techniques are imperative. Keep leads as short as possible and use a single ground point. Resistors R1 and R2 should be as close as possible to pin 1 to eliminate noise pick-up in the feedback loop. The TL497A type of circuits do not need "hi-Q" inductors. They are, in fact, not desirable due to the broad frequency range of operation. If the "Q" is too high, ringing will occur. If this happens, a shunt resistor (about 1-k Ω) may be placed across the coil to damp the oscillation.

While not necessary, it is highly desirable to use a toroidal inductor as opposed to a cylindrically wound coil. The toroidal type of winding helps to contain the flux closer to the core and in turn minimize radiation from the supply. All high current loops should be kept to a minimum length using copper connections that are as large as possible.



 $\frac{1}{\sqrt{0}}$

Figure 33. Inverting Applications

Design Considerations

A Step-Down Switching Regulator Design Exercise with TL497A

The schematic of a basic step-down regulator is shown in Figure 34. This regulator will have the following design goals:

$$V_{I} = 15 V$$

 $V_{O} = 5 V$
 $I_{O} = 200 mA$
 $V_{ripple} = < 1.0\% \text{ or } 50 mV (1.0\% \times 5 V)$

Calculations:

 $I_{PK} = 2 I_L max = 400 mA$





For design margin, I_{PK} will be designed for 500 mA which is also the limit of the internal pass transistor and diode.

• $I_{PK} = 500 \text{ mA}$

The next step will be to select t_{on} . You may select a timing capacitor to match an inductor you may already have. You may also assume an on-time and calculate the inductor value. We will assume an on-time of 20 μ s.

To set the TL497A for 5-V output:

R2 =
$$1.2 \text{ k}\Omega$$
 (fixed)
R1 = $(5 - 1.2) \text{ k}\Omega$ = $3.8 \text{ k}\Omega$

To set current limiting:

$$R_{CL} = \frac{0.5}{I_L} = \frac{0.5}{500 \times 10^{-3}} = 1 \Omega$$
$$R_{CL} = 1 \Omega$$

For the on-time chosen, C_T can be approximated:

$$C_{T}(pF) = 12 t_{on} \mu s$$
$$C_{T} = 240 pF$$

or it may be selected from a table in the data sheet.

To determine filter capacitor (CF) for desired ripple voltage:

$$C_{\rm F} = \frac{(I_{\rm PK} - I_{\rm L})^2}{(V_{\rm ripple}) \ 2 \ I_{\rm PK}} \times \frac{t_{\rm on} \ V_{\rm I}}{V_{\rm O}}$$
$$C_{\rm F} = \frac{(0.5 - 0.2)^2}{(0.05) \ 2 \times 0.5} \times \frac{20 \times 10^{-6} \times 15}{5} = 108 \ \mu {\rm F}$$

We selected C_F to be 120 μ F, the next higher standard value. Figure 35 illustrates the regulator with the calculated values applied to it.

A 150- μ F filter capacitor may be used as a prefilter as well as a 0.01- μ F disc capacitor to take care of any transients on the incoming V_I rail. For peak currents greater than 500 mA, it is necessary to use an external pass transistor and diode. Such a technique is illustrated in Figure 36, which is an automotive power supply. With a 12-V battery, this step-down regulator supplies 5 V at 2 A.

Figure 37 illustrates a basic step-up regulator. This design steps up the output voltage from 5 V to 15 V. The equations for determining the values of the external components are provided in Figure 31.











Figure 37. 5-V to 15-V Switching Regulator

Design and Operation of an Inverting Regulator Configuration

Figure 38 illustrates a basic inverting regulator designed to have -5-V output with +5-V input using the design equations in Figure 33.

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Conditions:

$$V_{I} = 5 V$$

 $V_{O} = -5 V$
 $I_{O} = 100 \text{ mA}$
 $V_{ripple} = 1.0\% \text{ or } 50 \text{ mV} (1\% \times 5 \text{ V})$

Calculations:

$$I_{PK} = 2 I_L(max) \left(1 + \frac{|V_O|}{V_I}\right)$$

$$I_{PK} = 400 \text{ mA (for design margin use 500 mA)}$$
Assume $t_{on} = 20 \ \mu\text{s}$

$$C_{T(pF)} = 12 \ t_{on} \ \mu\text{s}$$

$$C_T = 240 \ pF$$

$$L = \frac{V_I}{I_{PK}} t_{on} = \frac{5}{0.5} \times 20 = 200 \ \mu\text{H}$$

To set the output voltage:

$$R2 = 1.2 \text{ k}\Omega$$

R1 = (5 - 1.2) k\Omega = 3.8 k\Omega

To set the current limiting:

$$\begin{aligned} \mathsf{R}_{\mathrm{CL}} &= \ \frac{0.5}{\mathrm{I}_{\mathrm{PK}}} = \frac{0.5}{0.5} = 1 \ \Omega \\ \mathsf{R}_{\mathrm{CL}} &= \ 1 \ \Omega \\ \mathsf{C}_{\mathrm{F}} &= \ \frac{(\mathrm{I}_{\mathrm{PK}} - \mathrm{I}_{\mathrm{L}})^2}{(\mathrm{V}_{\mathrm{ripple}}) \ 2 \ \mathrm{I}_{\mathrm{PK}}} \times \frac{\mathsf{t}_{\mathrm{on}} \ \mathrm{V}_{\mathrm{I}}}{\mathrm{V}_{\mathrm{O}}} \end{aligned}$$

To determine C_{filter} for desired ripple voltage:

$$C_{\rm F} = \frac{(I_{\rm PK} - I_{\rm L})^2}{(V_{\rm ripple}) \ 2 \ I_{\rm PK}} \times \frac{t_{\rm on} \ V_{\rm I}}{| \ V_{\rm O} |}$$
$$= \frac{(0.5 - 0.1)^2}{(0.05)2 \times 0.5} \times \frac{20 \times 10^{-6} \times 5}{| \ -5 |}$$

 $C_F = 64 \ \mu F$ (nearest standard value = 68 μF)





Figure 38. +5-V to -5-V Switching Regulator

Adjustable Shunt Regulator TL430 - TL431

The TL430 and TL431 are three-terminal "programmable" shunt regulators. The devices are basically the same except the TL431 contains a diode connected between the emitter and collector of the output transistor. The standard symbol and block diagram are shown in Figure 39.

The circuit consists of a bipolar operational amplifier driving an n-p-n transistor. The reference on the TL430 is a band-gap reference (not temperature compensated). The TL431 has a true-temperature compensated band-gap reference and is more stable and accurate than other shunt regulators. The TL431 also has a diode across the emitter-collector of the n-p-n output transistor. If the cathode goes negative, the diode conducts around the transistor, emulating the performance characteristics of a normal zener diode. The basic operating characteristics are shown in Figure 40.



(b) BLOCK DIAGRAM



TL430, TL431 PROGRAMMABLE ZENERS



Figure 40. Basic Operating Characteristics

Their excellent thermal stability make these devices extremely attractive as a replacement for high-cost, temperature-compensated zeners. As seen in Figure 41, the TL431 offers improved characteristics, even at low voltages. Since the TL431 operates as a shunt regulator, it can be used as either a positive or negative voltage reference. The TL431 has an equivalent full-range temperature coefficient of 50 ppm/°C (typical) and has low output noise voltage. Note in the graph (Figure 41) that for a nominal 2.495-V reference the curve is essentially flat from 0°C to 70°C. Depending upon the zener voltage, the TL431 also has an extremely low dynamic impedance of about 0.2 Ω , compared to a standard zener diode's dynamic impedance of about 30 to 60 Ω .

A 2.5-V reference voltage is developed across R2 as shown in Figure 42. I_{ref} , the current input at the reference terminal, is about 10 μ A. To maintain a steady reference, it is advisable to allow 1 mA of current flow through series resistors R1 and R2. This will assure a stable reference voltage independent of I_{ref} variations. The TL431 is available in either the commercial temperature range of 0° - 70°C or the military temperature range of -55° to +125°C.

$$R = \frac{V_{I} - (V_{be} + V_{O})}{I_{R}}$$

$$R = \frac{32 - (2 + 24)}{10 \text{ mA}} = 600 \Omega$$

$$V_{O} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$R1 = 21.4 \text{ k}\Omega$$

$$R2 = 2.5 \text{ k}\Omega$$

The circuit in Figure 43 uses a TL431 as a regulator to control the base drive to a TIP660 series pass transistor. For good reference stability, a current flow of about 1 mA (I₂) though the resistor divider is recommended. A 2.5-V reference voltage is developed across R2, and R1 will develop a voltage drop of 21.5 V. The Darlington power transistor is used because of the reduced base drive requirement of the TIP660 which has a V_{be} (max) of about 2 V. The h_{FE} at 2.5-A I_C is about 1000, so it would only require about 2.5 mA of base drive to produce 2.5 A of output current. In calculating the value of the current limit resistor, R3, we assume about 7.5 mA of current through the TL431. The value of R3, therefore, would be 600 Ω and the current about 10 mA, so a 1/2-W resistor will suffice. This is a simple method of designing a medium output current power supply using only four components plus the series pass transistor.

Design Considerations


Figure 41. Reference Input Voltage vs Ambient Temperature



Figure 42. Basic Operational Circuit



Figure 43. Series Regulator Circuit

Shunt Regulator Applications (Crowbar)

To protect solid-state electronic equipment from overvoltage due to a power-supply component failure, it is sometimes desirable to use a "crowbar" circuit. When a preset voltage is exceeded, the TRIAC turns on, shorting the output and blowing the fuse on the input side of the crowbar circuit. The circuit in Figure 44 is set to trip when V_{O} reaches 27 V. When that occurs, the reference voltage should be 2.5 V which turns on the TL431, thus biasing the SCR low. This turns the SCR on and immediately blows the safety fuse on the circuit input, thus protecting the equipment using this power supply.

> 24 Vo

TRIAC TIC226A (8A-100 V)

MT2

$$= \left(1 + \frac{KI}{R2}\right) V_{ref}$$

$$= \left(1 + \frac{KI}{R2}\right) V_{ref}$$

$$= \frac{4 \text{ AMP}}{\text{FUSE}}$$

$$= 24.5 \text{ k}\Omega$$

$$= 100 \Omega$$

$$= 24.5 \text{ k}\Omega$$

$$= 100 \Omega$$

Figure 44. Shunt Regulator in Crowbar Circuit

 $V_{\text{LIMIT}} = \left(1 + \frac{R1}{R2}\right) V_{\text{ref}}$

V_L

Controlling Vo of a Fixed Output Voltage Regulator

Sometimes, it is necessary to have a regulated output voltage different from that for which the regulator is designed. This may be accomplished with any three-terminal regulator, although it should be noted that the lowest obtainable voltage will be 2.5 V for the TL431 plus the voltage of the three-terminal regulator. In the circuit in Figure 45, the lowest possible regulated voltage would be 7.5 V (2.5 V for the TL431 + 5 V for the 7805). This particular circuit provides 9-V output using a uA7805 three-terminal regulator.

Note: Minimum $V_O = V_{ref} + 5 V$





Figure 45. Fixed Output Shunt Regulator

Current Limiter

Figure 46 is an example of a current limiter designed to limit the current from a 12-V supply to 1.5 A using a TIP31 n-p-n transistor as the pass element. The value of R1 is calculated from the equation in Figure 46. The current through R1 is split almost equally in this circuit, with about 30 mA going to the TL431, and 30 mA for base drive to the TIP31. With a current load of 6 mA and an R1 value of 128 Ω , a 1/2-W resistor is sufficient. When the voltage across the current limit resistor (R_{CL}) reaches 2.5 V (TL431 reference voltage), the base drive to the TIP31 is reduced and the output current is limited to 1.5 A.

$$R1 = \frac{V_{I} - (V_{be} + V_{RCL})}{I_{1}} = \frac{12 - (1.8 + 2.5)}{0.06} = 128 \Omega$$
$$R_{CL} = \frac{V_{ref}}{I_{L}} = \frac{2.5 V}{1.5 A} = 1.7 \Omega$$



Figure 46. Current Limiter

Voltmeter Scaler

The circuit in Figure 47 is a voltmeter scaler (or multiplier) to extend the range of a 0- to 10-V voltmeter to 40 V. Most multiplier circuits extend the range with 0 V being the low reading on any given scale. This circuit actually divides the 40-V total range into 4 separate 10-V scales.

With the selector switch in position #1, the reference input of the TL431 is bypassed and the TL431 does not influence circuit operation. The meter is effectively connected directly to the voltage being measured. This scale would be the normal meter range of 0 to 10 V.



Figure 47. Voltmeter Scaler

When in position #2, a 75-k Ω and a 25-k Ω resistor are added in series across the anode and cathode of the TL431. The voltmeter will remain near zero until the input reaches 10 V. At this time, there is 2.5 V between the reference terminal and anode which causes the voltmeter to start reading at 10 V. It will continue reading on this scale until it reaches full scale, which is 20 V.

This sequence is repeated in 10-V steps until position #4 is reached. This circuit is very useful when expanded-scale voltmeter multiplication is required. The precision of the scaler depends upon the accuracy of the resistors.

Voltage-Regulated, Current-Limited Battery Charger for Lead-Acid Batteries

There are a number of approaches to recharging lead-acid batteries. Many will return the battery to service, but fail to fully rejuvenate the battery. To keep a battery fully charged, and attain maximum battery life, proper charging techniques must be observed.

The status of a cell is determined by the specific gravity of the electrolyte solution. A specific gravity of 1.280 (obtained by hydrometer reading) indicates a fully-charged cell. A reading of 1.250 or better is considered good. A fully-discharged cell exhibits a specific gravity of 1.150 or less.

Battery Charger Design

The battery charger design shown in Figure 48 is based on a charging voltage of 2.4 V per cell, in accordance with most manufacturers' recommendations. The battery charger circuit pulses the battery under charge with 14.4 V (6 cells \times 2.4 V per cell) at a rate of 120 Hz.

The design provides current limiting to protect the charger's internal components while limiting the charging rate to prevent damaging severely discharged lead-acid batteries. The maximum recommended charging current is normally about one-fourth the ampere-hour rating of the battery. For example, the maximum charging current for an average 44 ampere-hour battery is 11 A.

If the impedance of the load requires a charging current greater than the 11-A current limit, the circuit will go into current limiting. The amplitude of the charging pulses is controlled to maintain a maximum peak charging current of 11 A (8 A average).

The charger circuit is composed of four basic sections:

- 1. Rectifier
- 2. Voltage Regulator
- 3. Current Limiting
- 4. Series-Pass Element



Figure 48. Current-Limited and Voltage-Regulated Battery Charger

Rectifier Section

A full-wave rectifier configuration with a center-tapped transformer (Figure 49) achieves maximum performance with minimum component count. The breakdown voltage requirement for the diode is:

 $VR > Vsecondary(pk) - V_F(rectifier drop)$ $VR > 20 \times 2.8 - 1 = 55 V$

This design is set to current limit at 11 A, therefore, a rectifier rating of 25 A is recommended to handle the maximum current drain plus any current surges. A pair of 1N1184 diodes was chosen (35-A/50-V rectifiers).



Figure 49. Full-Wave Rectifier Section of Circuit

Voltage Regulator Section

The components which make up the voltage regulator portion of the circuit are: Z1, Q1, R1, R2 and R_B as shown in Figure 50. Z1 is a TL431 programmable shunt regulator which serves as the control element, Q1 is the pass transistor, and R1 - R2 sense the output voltage providing feedback to Z1. R1 and R2 are chosen so that their node voltage is 2.5 V at the desired output voltage. This node voltage is applied to the TL431's error amplifier which compares it to the internal 2.5-V reference.



Figure 50. Voltage Regulator Section of Circuit

When the feedback voltage is less than the internal 2.5-V reference, the series impedance (anode-to-cathode) of the TL431 increases, decreasing the shunt current through the TL431. This increases the current available to the base of pass transistor Q1, increasing the output voltage. When the feedback voltage is greater than the internal 2.5-V reference, the series impedance of the TL431 decreases, increasing the shunt current through the TL431. This decreases the current available to the base of Q1, decreasing the output voltage. Because the feedback voltage is sensed at the output, the TL431 will compensate for any changes in the base-emitter drop of Q1 or the voltage dropped across R_{CL} for various currents.

Current Limiter Section

The components which make up the current-limit portion of this circuit are: Z2, Q1, and R_{CL} as shown in Figure 51. The value of the current-limit setting resistor, R_{CL} , is chosen so that 2.5 V will be developed across it at the desired limit current. The voltage across R_{CL} is sensed by a TL431 programmable shunt regulator (Z2). When the output current is less than the current limit, V_{ref} is less than 2.5 V and Z2 is a high impedance which does not affect the operation of Q1.

When the output current reaches maximum, V_{ref} is 2.5 V and the impedance of Z2 decreases, decreasing the current available at the base of Q1 and controlling the maximum output current. Under this condition, shunt regulator Z2 takes control of pass transistor Q1 and maintains a constant current, even into a short circuit.



Figure 51. Current Limiter Section of Circuit

Series Pass Element

The series pass element used in this configuration is a conventional Darlington power transistor, whose control is derived from either Z1 or Z2 depending on the state of the battery being charged. See Figure 52.

The performance characteristics of Q1 are important in determining the circuit design and in the choice of the transformer to be used. This relationship is shown in the following section on the design of the battery charger.



Figure 52. Series Pass Element

Design Calculations

The values of R1 and R2 set the output voltage level at 2.4 V per cell or 14.4 V for 6 cells. For optimum performance of Z1, 1 mA should flow through the R1 and R2 combination.

$$R1 + R2 = \frac{14.4 \text{ V}}{1 \text{ mA}} = 14.4 \text{ k}\Omega$$
$$R2 = \frac{2.5 \text{ V}}{1 \text{ mA}} = 2.5 \text{ k}\Omega$$
$$R1 = 14.4 \text{ k}\Omega - 2.5 \text{ k}\Omega = 11.9 \text{ k}\Omega$$

For ease of final adjustment, a 20-k Ω potentiometer may be used for R1.

Current limiting starts when 2.5 V is developed across R_{CL} at the desired current limit. For a 44-A hour battery, the maximum charge rate is 11 A.

$$R_{CL} = \frac{2.5 \text{ V}}{11 \text{ A}} = 0.227 \Omega$$

The average current = $0.707 \times 11 \text{ A} = 7.777 \text{ A} \text{ or} \approx 8 \text{ A}$

The average power dissipation = $I^2R = 8^2 \times 0.227 = 14.5$ W

After the pass transistor has been selected, its base drive resistor, R_B , may be calculated. A TIP642 meets the requirements. From the data sheet:

To calculate R_B, assume a worst case or short-circuit condition where:

$$R_{B} \approx \frac{V_{I} - V_{ref} - V_{BE(Q1)}}{I_{B}(Q1) + I_{SHUNT}(Z_{2})}$$
$$R_{B} \approx \frac{27.28 - 2.5 - 1.6}{0.022 + 0.12} = 163 \,\Omega$$

 R_B must be small enough so that it does not limit the base current of Q1 at the desired I_{CHG} of 8 A, but large enough to limit the current during short circuit conditions. This value should be less than the sum of the base drive current required by Q1 and $I_{SHUNT(max)}$ Z2.

$$R_{B} \approx \frac{(V_{I} - 14.4 V - 2.5 V - V_{BE}(QI))}{I_{CHG}/h_{FE}(QI)}$$
$$= \frac{27.28 - 14.4 - 2.5 - 1.6}{8/500}$$
$$R_{B} \approx \frac{8.78}{0.016} = 548.7 \Omega$$

A value of R_B within this range assures sufficient drive to Q1 for a charging rate of 8 A, yet allows total control of Q1 by Z2 during short-circuit conditions. R_B was selected to be 200 Ω .

Power Dissipation and Heat Sinking

To determine the power dissipation in the 1N1183 rectifier and the TIP642 Darlington, the RMS currents and voltages must be calculated. The voltage and current paths are shown in Figure 53.



Figure 53. Voltage and Current Path

 $V_{CE(Q1)} = V_I - V_{BATT} - V_{RCL} = 27.78 - 14.4 - 2.5 = 10.88 V$ $V_{CE(Q1)} = 10.9 V$

The transistor power dissipation is:

$$P_{Q1} = I_{(RMS)} \times V_{CE(RMS)} = (11 \text{ A} \times 0.707)(10.9 \text{ V} \times 0.707)$$

 $P_{Q1} = (7.78 \text{ A}) (7.7 \text{ V})$
 $P_{O1} = 59.9 \text{ W}$

The rectifier power dissipation is:

 $P_{(RECT)} = I_{(RMS)} \times V_F = (7.78 \text{ A}) (1.3 \text{ V})$ $P_{(RECT)} = 10.1 \text{ W total}$

If the pass transistor and rectifiers are mounted on separate heat sinks, the sinks must be capable of dissipating the heat transferred by each device and maintain a surface temperature which satisfies the temperature requirement for each device. Mounted separately, the respective heat sink requirements are as follows:

PASS TRANSISTOR	RECTIFIERS		
$R_{\Theta CA} \leq \frac{150^{\circ}C - 25^{\circ}C}{59.9 \text{ W}}$	$R_{\Theta CA} < \frac{140^{\circ}C - 25^{\circ}C}{10.1 W}$		
$R_{\Theta CA} \leq 2.08^{\circ}C/W$	$R_{\Theta CA} < 11.4^{\circ}C/W$		

Depending on the mass of the heat sink and the type of cabinet, forced air cooling may be required.

Voltage Supply Supervisor Devices

Voltage supply supervisor devices deliver a digital output signal (high or low) if supply voltage (V_{CC}) falls below a predefined value. The digital output signal remains in its high or low state for a certain period of time (t delay) after V_{CC} returns to normal. These devices are used to sequentially initialize digital systems for proper operation at power-on or following a V_{CC} interruption.

The versatility, few external components, and accurate threshold voltage of the TL7700 series make these devices easy to use in digital systems requiring V_{CC} line supervision.

General Operation

At power-on, digital systems must normally be forced into a definite initial state. In simple microcomputer and microprocessor applications, an RC network connected to the RESET input pin will generally suffice. However, in more complex systems, a discrete component design as illustrated in Figure 54 may be used.

In this circuit, after V_{CC} reaches a specific value, defined by Z_D , the input voltage divider, and V_{BE} , the collector of Q2 becomes high and coupling capacitor C1 provides enough power to the RESET input pin of the digital system to execute the reset function.

The major deficiency with this type of circuit is that after power-on and the system is operating, low V_{CC} conditions and short drops in V_{CC} may not be recognized. A small decrease of V_{CC} below the recommended supply voltage can destroy the content of the memory and registers without activating the reset circuit. This may have catastrophic

consequences. Moreover, the circuit in Figure 54 contains an excessive number of components, one being Z_D , which has to be specially selected and is therefore relatively expensive.



Figure 54. Discrete Solution of a Voltage Supply Supervisor

Several features are provided in larger computers to prevent some of the problems just mentioned. In some cases, the content of the memory is protected by a battery back-up. However, for most applications and in small microcomputer systems, these solutions are too expensive and generally not required. After any serious voltage drop, it is usually sufficient to force the microcomputer into a defined initial condition. To implement this function, while preventing the problems previously mentioned, a chip with the following features is required:

- 1. Accurate detection of a serious voltage drop
- 2. Generation of a continuous reset signal while the supply voltage is not in the operational range to prevent undefined operations.
- 3. Maintenance of the reset signal for a certain time after the supply voltage has returned to its nominal value to ensure a proper reset.

TL77XXA Series Supervisor Chips

A functional block diagram of the chip is illustrated in Figure 55. The most critical element of this chip is the reference voltage source, which consists of a very stable, temperature-compensated bandgap reference. An external capacitor (typically 0.1 μ F) must be connected to the Reference (REF) voltage output to reduce the influence of fast transients in the supply voltage. The voltage at the SENSE INPUT pin is divided by resistors R1 and R2 and compared with the reference voltage. The divider is adjusted to achieve high accuracy at the probing operation during manufacture of the chip.



Figure 55. TL77XXA Series Function Block Diagram

When the sensed input voltage is lower than the threshold voltage, the thyristor is triggered discharging the timing capacitor C_T . It is also possible to fire the thyristor with a TTL logic level (active low) at the <u>RESIN</u> input. The thyristor is turned off again when the voltage at the SENSE INPUT (or <u>RESIN</u> input) increases beyond the threshold, or during short supply voltage drops when the discharge current of the capacitor becomes lower than the hold current of the thyristor. Capacitor C_T is recharged by a 100-µA current source; the charge time is calculated as follows:

 t_d (internal time delay) = $C_T (1.3 \times 10^4)$

A second comparator forces the output into the active state as long as the voltage at the capacitor is lower than the reference voltage. Figure 56 is a graph plotting C_T versus t_d . The SENSE INPUT pin is connected to V_{CC} in typical applications. Figure 57 shows the timing of the supply voltage and **RESET** signals.

The minimum supply voltage for which operation is guaranteed is 3 V. Between POWER-ON (0 V) and 3 V, the state of the outputs is not defined. In practical applications, this is not a limitation because the function of the reset inputs of the other devices is not guaranteed at such supply voltages.

Above 3 V, capacitor C_T is discharged and the outputs stay in the active state. When the input voltage exceeds the threshold voltage, V_S , the thyristor is turned off and capacitor C_T is charged. After a delay of t_d , the voltage passes the trigger level of the output comparator and the outputs become inactive. The microcomputer is then set to a defined initial state and starts operation.



Figure 56. Graph for Calculation of C_T



Figure 57. Timing Diagram

Operation During a Voltage Drop

The thyristor is triggered when the supply voltage drops below the minimum recommended value. After the supply returns to its required value, the output stays in the active state for the duration of t_d .

The delay time, t_d , is determined by the requirements of the computer system to be controlled. Typically, in TTL systems, a reset time of 20 to 50 ns is sufficient.

Microcomputers usually require a reset signal which lasts several machine cycles. The duration of the reset signal is dependent on the type of microcomputer, but is typically 10 to 200 μ s. In most practical applications, t_d is determined by the characteristics of the power supply.

During and shortly after power-on make sure voltage fluctuations do not repetitively reset the system. Delay times of 10 to 20 ns will usually prevent this problem. Four versions of this device are available:

	Threshold Voltage	Vcc
TL7702A	2.53 V	3.0 — 18.0 V
TL7705A	4.55 V	5.0 V
TL7712A	10.8 V	12.0 V
TL7715A	13.5 V	15.0 V

The TL7702A may be used in applications where V_{CC} voltages up to 18 V are used. The required trigger level (2.5 V) may be set with a resistor divider network at the SENSE INPUT pin. The TL7705A, TL7712A, and TL7715A have an internal resistor divider network and operate on 5 V, 12 V, and 15 V, respectively.

TL77XXA Series Applications

Since, for most applications, the devices are already adjusted to the appropriate voltage levels, these chips are easy to use. Figure 58 illustrates an undervoltage protection circuit for a TMS370 microcomputer system with a 5-V power supply. External components are the 0.1- μ F bypass capacitor at the REF terminal, which reduces transients from the supply voltage, and the C_T capacitor, which sets the time delay (t_d). The TL7705A devices do not have internal pull-up (or pull-down) resistors. An external 10-k Ω pull-up resistor is connected from the RESET pin to the 5-V V_{CC} to produce a high level. A similar application is illustrated in Figure 59.

This circuit utilizes a TL7715A as a protection device for a TMS1000 microcomputer system. The C_T and reference bypass capacitors are also used in this application. Note, however, the absence of the pull-up resistor used in Figure 58. This circuit has a required internal pull-down resistor at the INIT INPUT pin on the TMS1000 microcomputer chip.

In large systems, where several supply voltages are required (e.g., TMS8080, TMS9900), it is necessary to supervise all supply voltages that may cause dangerous conditions if a power failure or transient occurs. The circuit illustrated in Figure 60 uses two TL7712A devices to check the positive and negative 12-V supplies. A TL7705A is used to check a 5-V supply.



Figure 58. TL7705A in 5-V Microcomputer Application



Figure 59. TL7715A in TMS1XXXNLP Application

The outputs of the two TL7712As are fed to the RESIN input of the TL7705A. The output of this device, a system-reset signal, becomes active when any one of the three supply voltages fail. The supply voltage supervisor devices were designed to detect very short voltage drops of 150 ns. In applications where this sensitivity is not required, the circuit may be delayed by adding an RC network ahead of the SENSE INPUT pin (Figure 61). To avoid influence on the threshold voltage of this input, the resistor should be less than 22 Ω . The capacitor C_d is then calculated to the required delay time (C_d = t/R).

Another application for the TL7705A is in battery-buffered memory systems. After a line-voltage failure, the content of the memory has to be protected against spikes on the write line. It is usually sufficient to switch the chip-select line into the inactive state; however, some memories also require that the write line be disabled. See Figure 62. A switch, formed by transistor Q1 and diode D1, is inserted into the chip-select line of the memory. Under normal operation (line voltage present), the RESET output of the TL7705A is turned off (high), transistor Q2 is turned on, and transistor Q1 draws its base current through transistor Q2 and resistor R1. When the chip-select line is switched from high to low, transistor Q1 conducts and the CS input of the memory goes low. Because of the small dc load of resistor R2, the saturation voltage of the transistor is very small (typically 40 mV). When the chip-select line is switched high again, transistor Q1 is turned off and diode D1 conducts, charging the circuit capacitance.

In case of a power failure, the TL7705A is triggered and its RESET output becomes low, turning off transistor Q2 and the base current to transistor Q1. In this way, the CS input of the memory is separated from the chip-select line. In some cases, it is also recommended that memory be disabled during the system reset with the \overline{RI} SIN input. This protects the memory content against spikes on the write line during this time.





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Design Considerations



Figure 61. Delayed Triggering



Figure 62. Circuit Diagram for Memory Protection

uA723 Precision Voltage Regulator

The uA723 monolithic integrated circuit voltage regulator is used extensively in power supply designs. The device consists of a temperature-compensated reference amplifier, an error amplifier, a 150-mA series-pass transistor, and current-limiting circuitry. See Figures 63 and 64 for the functional diagram and schematic.

Additional external n-p-n or p-n-p pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition, the device features low standby current drain, low-temperature drift and high-ripple rejection. The uA723 may be used with positive or negative supplies as a series, shunt, or floating regulator.







Figure 64. uA723 Schematic

When using an external series pass device, the 3-dB bandwidth of the uA723 must also be taken into consideration. Adequate uA723 compensation may be provided by connecting a 100- to 500-pF capacitor from the compensation terminal to the inverting input. Extra capacitance may be required at both the input and output of any power supply due to the inductive effects of long lines. Adding output capacitance provides the additional benefit of reducing the output impedance at high frequencies.

Typical Applications

The required output voltage and current limits for the applications shown in Figure 65 can be calculated from the equations given in Table 1. In all cases, the resulting resistor values are assumed to include a potentiometer as part of the total resistance. Table 2 affords a quick reference for many standard output voltage requirements.

Table 1. Formulas for Output Voltages

Outputs from 2 to 7 V [Figures 65(a), (e), (f)]

vo	_	V _(ref)	×	R2		
	_			R1	+	R2

Outputs from 7 to 37 V [Figures 65(b), (d), (e), (f)]

$$V_{O} = V_{(ref)} \times \frac{R1 + R2}{R2}$$

Outputs from -6 to -250 V [Figure 65(c)]

$$v_{\rm O} = -\frac{V_{\rm (ref)}}{2} \times \frac{R1 + R2}{R1}$$

$$R3 = R4$$

Current Limiting

$$I_{(\text{limit})} \approx \frac{0.65 \text{ V}}{\text{R}_{\text{SC}}}$$

Foldback Current Limiting [Figure 65(f)]

$$I_{(\text{knee})} \approx \frac{V_{\text{O}}R3 + (R3 + R4)0.65 \text{ V}}{R_{\text{SC}} \text{ R4}}$$
$$I_{\text{OS}} \approx \frac{0.65 \text{ V}}{R_{\text{SC}}} \times \frac{R3 + R4}{R4}$$



Figure 65. Typical Applications

OUTPUT APPLICABLE VOLTAGE FIGURE (65)		FIXED OUTPUT ± 5% kΩ		ADJUSTABLE ΟUTPUT ± 10% kΩ		
(V)	SEE NOTE 1	R1	R2	R1	P1	R2
+ 5.0	a, e, f	2.15	4.99	0.75	0.5	2.2
+ 6.0	a, e, f	1.15	6.04	0.5	0.5	2.7
+9.0	b, d, e, f	1.87	7.15	0.75	1.0	2.7
+ 12.0	b, d, e, f	4.87	7.15	2.0	1.0	3.0
+ 15.0	b, d, e, f	7.87	7.15	3.3	1.0	3.0
-9.0	c see	3.48	5.36	1.2	0.5	2.0
- 12.0	c > note 2	3.57	8.45	1.2	0.5	3.3
- 15.0	c	3.57	11.5	1.2	0.5	4.3

Table 2. Resistor Values for Standard Output Voltages

NOTES:1. To make the voltage adjustable, the R1/R2 divider shown in the figures must be replaced by the divider shown here.



2. For negative output voltages less than 9 V, V_{CC} + and V_C must be connected to a level large enough to allow the voltage between V_{CC} + and V_{CC} - to be greater than 9 V.

General-Purpose Power Supply

The general-purpose power supply shown in Figure 66 may be used for supply output voltages from 1 to 35 V. The line transformer should be selected to give about 1.4 times the desired output voltage from the positive side of the filter capacitor, C1, to ground. R1 discharges the carriers in the base-emitter junction of the TIP31 when the drive is reduced. Its value is determined as follows:

$$R1 = \frac{TIP31 \text{ voltage (at point of conduction)}}{\text{leakage current of TIP31 and uA723 output}}$$

where:

TIP31 voltage at point of conduction is 0.35 V, leakage current (collector-base) of the TIP31 plus the collector-emitter leakage of the uA723 output transistor (worst case = 200μ A).

therefore:

$$R1 = \frac{0.35 \text{ V}}{0.0002 \text{ A}} = 1750 \Omega \text{ max}$$

 $R1 = 1.5 k\Omega$ (standard value)

Potentiometer R2 sets the output voltage to the desired value by adjusting the reference input voltage. It is connected between pin 6 (7.15-V reference) and ground. The center arm of R2, connected to pin 5, will select any point between zero and the 7.15-V reference.

Resistors R3 and R4 are connected in series across the supply output. The junction of these two resistors is connected to the inverting input (pin 4) of the error amplifier establishing an output voltage reference. This voltage reference is compared to the selected voltage at the noninverting input to the error amplifier (pin 5) to set the level of output voltage regulation. The values for R3 and R4 are listed in Note 1 of Figure 66. R_{SC} is the current limit set resistor. Its value is calculated as:

$$R_{SC} = \frac{0.65 \text{ V}}{I_L}$$

For example, if the maximum current output is to be 1 A, $R_{SC} = 0.65/1.0 = 0.65 \Omega$.



Figure 66. General-Purpose Power Supply

The 1-k Ω resistor, R_S, on the output is a light-load resistor designed to improve the no-load stability of the supply. The 100- μ F electrolytic capacitor improves the overall output ripple voltage. A 100-pF capacitor from the compensation terminal (pin 13) to the inverting input (pin 4) allows for gain variations in the uA723 error amplifiers and for parasitic capacitances.

The output voltage and current of this supply must be restricted to the specifications of the TIP31 series pass transistor. Since it is rated at 2 W in free air at 25°C, sufficient heat sinking is necessary.

8-A Regulated Power Supply for Operating Mobile Equipment

It is often necessary to operate or test equipment used in automotive applications. This supply, as shown in Figure 67, provides up to 8 A at 13.8 V. The uA723 is used as the control element, furnishing drive current to series-pass transistors which are connected in a Darlington configuration. Two 2N3055 n-p-n transistors are used as the pass transistors, so proper heat sinking is necessary to dissipate the power.

This supply is powered by a transformer operating from 120 VAC on the primary and providing approximately 20 VAC on the secondary. Four 10-A diodes with a 100-PIV rating are used in a full-wave bridge rectifier. A $10,000-\mu$ F/36-VDC capacitor completes the filtering, providing 28 VDC.

The dc voltage is fed to the collectors of Darlington-connected 2N3055s. Base drive for the pass transistors is from pin 10 of the uA723 through a 200- Ω current limiting resistor, R1. The reference terminal (pin 6) is tied directly to the noninverting input of the error amplifier (pin 5), providing 7.15 V for comparison. The inverting input to the error amplifier (pin 4) is fed from the center arm of a 10-k Ω potentiometer connected across the output of the supply. This control is set for the desired output voltage of 13.8 V. Compensation of the error amplifier is accomplished with a 500-pF capacitor connected from pin 13 to pin 4.

The 1-k Ω resistor on the output is a light load to provide stability when the supply has a no load condition. The 100- μ F/16-VDC electrolytic capacitor completes the filter action and reduces the ripple voltage. The current output of the supply is sampled through resistor R_{SC} between the output transistor and the output terminal. The resistor value for a 10-A maximum current is calculated from the formula:

$$R_{SC} = \frac{0.65 \text{ V}}{I \text{ (load max)}} = \frac{0.65}{10} = 0.065 \Omega$$

If the power supply should exceed 8 A or develop a short circuit, the uA723 regulator will bias the transistors to cutoff and the output voltage will drop to near zero until the short circuit condition is corrected. This circuit features a no-load-to-full-load (8 A) voltage regulation of no more than 0.2-VDC variation (better than 2% regulation).



Figure 67. 8-A Regulated Power Supply

± 15 V at 1 A Regulated Power Supplies

When working with operational amplifiers, a common requirement is plus and minus supplies in the 15-V range. A positive 15-V supply is shown in Figure 68 and a negative 15-V supply is shown in Figure 69.

Positive Supply

The positive supply, shown in Figure 68, receives +20 VDC from the rectifier/filter section. This is applied to pins 11 and 12 of the uA723 as well as to the collector of the 2N3055 series-pass transistor. The output voltage is sampled through R1 and R2 providing about 7 V with respect to ground at pin 4.



Figure 68. +15-V at 1-A Regulated Power Supply

The reference terminal (pin 6) is tied directly to pin 5, the noninverting input of the error amplifier. For fine trimming of the output voltage, a potentiometer may be installed between R1 and R2. A 100-pF capacitor from pin 13 to pin 4 furnishes gain compensation for the amplifier.

Base drive to the 2N3055 pass transistor is furnished by pin 10 of the uA723. Since the desired output of the supply is 1 A, maximum current limit is set to 1.5 A by resistor R_{SC} whose value is calculated as:

$$R_{SC} = \frac{0.65 \text{ V}}{I_{(\text{max limit})}} = \frac{0.65}{1.5} = 0.433 \Omega$$

A 100- μ F electrolytic capacitor is used for ripple voltage reduction at the output. A 1-k Ω output resistor provides stability for the power supply under no-load conditions. The 2N3055 pass transistor must be mounted on an adequate heat sink since the 3.5-W, 25°C rating of the device would be exceeded at 1-A load current.

Negative Supply

The negative 15-V version of this power supply is shown in Figure 69. The supply receives -20 V from the rectifier/filter which is fed to the collector of the Darlington p-n-p pass transistor, a TIP105. A different uA723 configuration is required when designing a negative regulator.



Figure 69. -15-V at 1-A Regulated Power Supply

The base drive to the TIP105 is supplied through resistor R5. The base of the TIP105 is driven from pin 9 (V_Z terminal), which is the anode of a 6.2-V zener diode that connects to the emitter of the uA723 output control transistor.

The method for providing the positive feedback required for foldback action is shown in Figure 69. This technique introduces positive feedback by increasing current flow through resistors R1 and R2 under short-circuit conditions. This forward biases the base-emitter junction of the 2N2907 sensing transistor, which reduces base drive to the TIP105.

The final percentage of foldback depends on the relative contributions of the voltage drop across R2 and R_{SC} to the base current of the 2N2907 sensing transistor. From the start of base-emitter conduction of the sense transistor to the full shut-off of the TIP105 pass transistor requires a 2- μ A base current.

The latch condition, or 100% positive feedback, is generated by any change in the input voltage which increases the voltage drop across R2 turning on the sense transistor (2N2907). It can only be reset by breaking the positive feedback path with switch S1. This allows the series pass device to once more be driven in a normal fashion.

R3 and R4 are equal in value and divide the 7.15-V reference in half. The resulting 3.6-V reference is tied to the inverting input of the error amplifier. R6 and R7 are connected in series across the output of the power supply. The junction of R6 and R7 furnishes 3.6 V to the noninverting input of the error amplifier. At this point, the output is regulated at -15 V with respect to ground.

Resistors R1 and R2 are calculated as follows:

 $R1(k\Omega) = V_{I} - *V_{SENSE(V)}$ = 20 - 0.5 $= 19.5 k\Omega$ $R1 = 20 k\Omega \text{ (standard value)}$ $R2(k\Omega) = *V_{SENSE(V)} = 0.5 \text{ k or } 510 \Omega \text{ (standard value)}$ $Resistor R5 = (V_{I} - V_{O} - V_{BEQ2} - VR_{SC}) \times \frac{(\text{min beta } Q2)}{I_{M} \text{ (max load current)}}$ $R5 = (20 - 15 - 2.8 - 0.4) \times \frac{1000}{1} = 1800 \Omega$ $R5 = 1.8 k\Omega$

*V_{SENSE} is defined as the base to emitter voltage needed to start turn-on of the 2N2907. From the data sheet this is about 0.5 V.

The current sense resistor RSC is calculated as follows:

$$R_{SC} = \frac{V_O}{I_M} \left(\frac{V_{SENSE}}{V_I - V_{SENSE}} \right) = \frac{15}{1} \left(\frac{0.5}{20 - 0.5} \right) = 0.384 \ \Omega$$
$$R_{SC} = 0.39 \ \Omega$$

Foldback limiting, as used in this circuit, is advantageous where excessive pass transistor power dissipation is a problem. The TIP105 can tolerate only 2-W dissipation in free air at 25°C ambient, so adequate heat sinking is necessary.

Overvoltage Sensing Circuits

The use of SCR crowbar overvoltage protection (OVP) circuits is a popular method for providing protection from accidental overvoltage stress for a power supply load. The sensing function for this type of OVP circuit can be provided by a single IC, the MC3424, as shown in Figure 70.



Figure 70. MC3423 Overvoltage Crowbar Sensing Circuit Block Diagram

The Crowbar Technique

One of the simplest and most effective methods of obtaining overvoltage protection is to use a crowbar SCR placed across the equipment's dc power supply bus. As the name implies, the SCR is used much like a crowbar would be, to short the input of the dc supply when an overvoltage condition is detected. A typical circuit configuration is shown in Figure 71.



Figure 71. Typical Crowbar Circuit

The MC3423 operates from a V_{CC} minimum of 4.5 V to a maximum of 40 V. The input error amplifier has a 2.6-V reference between the noninverting input and V_{EE}. The inverting input is V_{sense1} (Pin 2) and is the point to which the output sense voltage is applied. This is usually done through a resistor voltage divider which sets the trip point (V_{ref}) at 2.6 V. The output of the device, pin 8, then triggers the gate drive terminal of the SCR. A basic OVP circuit is shown in Figure 72.

When V_{CC} rises above the trip point set by R1 and R2, an internal current source (pin 4) begins charging capacitor C1 which is also connected to Pin 3. When triggered, pin 8 supplies gate drive through the current-limit resistor (RG) to the gate of the SCR. The minimum value of RG is given in Figure 73.



Figure 72. Overvoltage Protection Circuit



The value of capacitor C determines the minimum duration of the overvoltage condition necessary to trip the OVP. The value of C can be determined from Figure 74. If the overvoltage condition disappears before C is charged, C discharges at a rate which is 10 times faster than the charging rate, and resets the timing feature until the next overvoltage condition occurs.



Figure 74. Capacitance vs Minimum Overvoltage Duration

Activation Indication Output

An additional output for use as an OV indicator is provided on the MC3423. This is an open-collector transistor which saturates when the OVP circuit is activated. It will remain in a saturated state until the SCR crowbar pulls the supply voltage, V_{CC} , below 4.5 V.

This output may also be used to clock an edge-triggered flip-flop whose output inhibits or shuts down the power supply when the OVP trips. This method of protection reduces or eliminates the heat-sinking requirements for the crowbar SCR.

Remote Activation Input

Another feature of the MC3423 is its remote activation input, pin 5, which has an internal pull-up current source. This input is CMOS/TTL compatible and, when held below 0.8 V, the MC3423 operates normally. However, if it is raised above 2 V, the OVP is activated regardless of whether an overvoltage condition is present. This feature may be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition.

TL77XXA Series Supply Voltage Supervisors

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Design Considerations



Introduction

The TL77XXA supply voltage supervisors are a series of monolithic integrated circuits that monitor the power supply status in digital and computer equipment and supply a reset signal when the supply voltage falls below the operational range. Each TL77XXA device performs all the functions required to monitor a voltage supply and generate complementary reset outputs whenever the voltage level being monitored falls below a defined operational range.

The reset outputs are maintained for a certain time delay after the supply voltage has returned to its nominal value. This allows the supply voltage to stabilize and prevents undefined operations. The amount of delay, t_d , is determined by an external timing capacitor C_T in accordance with the following formula:

 $t_d \approx 1.3 \text{ X } 10^4 \text{ X } \text{CT}$

where:

td is in seconds CT is in farads

Theory of Operation

This section explains why a reset function is necessary in computer applications and how this function has been typically performed. It also explains why the TL77XXA supply voltage supervisors are a superior alternative to typical solutions, and provides a detailed description of TL77XXA performance.

Typical Reset Generators

A reset generator is required in most digital or computer applications where vital data is stored in volatile memory. Most digital or computer equipment uses discrete circuits that force the system into a defined state after power-on and when a supply voltage drop is detected.

Discrete Reset Generator 1

In a typical application (see Figure 1) for a digital or computer system, the reset input is connected to an RC (resistor-capacitor) reset network.

During power-up, the RC reset network maintains the reset signal until the charge on the capacitor reaches the threshold value. However, this network does not work well



Figure 1. Discrete Reset Generator 1 in Typical System Application



Figure 2. Discrete Reset Generator 2 in Typical System Application

during short voltage drops because the capacitor does not have enough time to discharge through the diode. This circuit is also characterized by a slow rise time and an uncertain reset time.

Discrete Reset Generator 2

Discrete reset generator 2 solves the problem of slow rise time (see Figure 2).

This circuit uses a zener diode to determine the threshold of the voltage being monitored, (V_{CC}) . A reset signal is generated when V_{CC} drops to a level that causes the voltage at the junction of resistors RA and RB to fall below the zener diode breakdown voltage.

Either a high-active RESET or a low-active $\overrightarrow{\text{RESET}}$ output can be produced, depending on the connections to the inverting and noninverting inputs of the operational amplifier (op-amp).

For proper operation, V_{CC} for this circuit should never drop below the zener diode breakdown voltage or an undefined threshold point results.

Discrete Reset Generator 3

The circuit shown in Figure 3 provides a reset signal during power-up and detects short drops in the power supply.



Figure 3. Discrete Reset Generator 3 in Typical System Application

This circuit generates a low-active pulse when one or both comparator outputs go low. This occurs when V_{CC} drops below the predefined threshold.

However, this circuit has two major disadvantages:

- 1. It does not generate accurate reset pulse durations.
- 2. It requires an excessive amount of components. The extra components add to the cost of the system and occupy more board space.

TL77XXA Performance

The TL77XXA series of supply voltage supervisors, with few external components, solves the problems associated with typical discrete reset generators. The TL77XXA supply voltage supervisors immediately detect low voltage conditions that

can cause a computer system to lose valuable data. Most discrete reset generators require a severe glitch before a fault is detected. However, the TL77XXA supervisors are sensitive to power drops of very small magnitude and duration.

In addition, fast rise and fall times are provided on the reset signal, which can be adjusted to ensure stable operating conditions.

To eliminate the need for an external inverter, two outputs, RESET and RESET, are provided. These outputs remain active down to supply levels of 2 V during powerdown, which would not be possible with an external inverter. Hysteresis is provided on the SENSE IN pin to improve the device performance by preventing oscillations around the threshold point.

Each TL77XXA circuit includes a very stable, temperature-compensated bandgap reference (see Figure 4), trimmed to 2.53 V (typically). In all but the TL7702A, a precision resistor-divider network (R1 and R2) reduces the voltage at SENSE IN for comparison with the internal reference voltage.



Figure 4. TL77XXA with Very Stable **Temperature-Compensated Bandgap Reference**

The typical resistance values of resistors R1 and R2 differ for the various supply voltage supervisors in the TL77XXA series. The nominal values of R1 and R2 for each are listed below.

	R1	R2
TL7702A	Short	Open
TL7705A	7.8 kΩ	10 kΩ
TL7709A	19.7 kΩ	10 kΩ
TL7712A	32.7 kΩ	10 kΩ
TL7715A	43.4 kΩ	10 kΩ

When the voltage being monitored at SENSE IN is within the operating range, SENSE IN voltage is greater than or equal to the threshold, the reset input (\overline{RLSIN}) is high, the internal silicon-controlled rectifier (SCR) is off, and the external timing capacitor (CT) is charged to a value above the reference voltage. Both RESET and RESET outputs are inactive (low and high, respectively). Because both outputs are only active in one direction. RESET must be connected to a pull-down resistor and RESET to a pull-up resistor.

The TL77XXA outputs become active to generate a reset under various conditions.

When the SENSE IN voltage falls 10% below its operating value, the SCR is fired, the timing capacitor is discharged, and the outputs are forced into their active states.

With a low at the $\overline{\text{RESIN}}$ input, the SCR fires independently of the state of SENSE IN, so that an external system can generate a reset.

The SCR is turned off again after the voltages at SENSE IN and $\overline{\text{RESIN}}$ inputs increase above the respective thresholds.

In the TL7702A supply voltage supervisor, SENSE IN is tied directly to the input comparator, so that the threshold voltage can be programmed through an external voltage divider connected to SENSE IN.

For proper operation, the recommended voltage at SENSE IN should not exceed $V_{CC} - 1 V$. Voltage in excess of 6 V at this input will damage the internal circuit. With the exception of this feature, the performance of the TL7702A supply voltage supervisor is identical to that of the other circuits in the TL77XXA series.

During power-up, the outputs are undefined until the supply voltage (V_{CC}) to the TL77XXA reaches 3.6 V (see Figure 5). During power-down, with the voltage at SENSE IN below the threshold, the outputs remain active until the supply voltage to the TL77XXA falls below 2 V.

For proper operation in all TL77XXA applications, an external capacitor (0.1 μ F minimum) must be connected from the REF pin to ground. The reference capacitor should be connected as close as possible to the TL77XXA. Using the reference output as a source for other circuits may result in erroneous operations.



Figure 5. Circuit for Power-Up and Detection of Short Drops

TL77XXA Circuit Operation (see Figure 6)

Initialization

During power up, before the TL77XXA attains the minimum operating supply voltage value of 3.6 V, the bandgap reference circuit is inoperative, and both the RESET and $\overline{RI} \cdot N \overline{T}$ outputs are undefined. When V_{CC} exceeds 3.6 V, the reference circuit is ensured to be on by transistor Q32 and the 150-k Ω resistor, which form the start-up circuit. At this point, the reference voltage (pin 1) remains fixed at 2.53 V (typical) and is applied to the base of Q8, which is the inverting input of the comparator Q7-Q8. The noninverting input (the base of Q7) is the divided-down SENSE IN voltage from pin 7.

Low RESIN

When $\overline{\text{RESIN}}$ (pin 2) is tied low, transistor Q19 is turned on and Q18 is turned off. With Q18 off, the base of Q17 is biased to the reference voltage, turning Q17 on. This activates the current mirror Q5-Q6, regardless of the state of Q8. Also with Q17 on, Q16 turns on causing Q12 to be shunted. This causes current mirror Q11-Q12 to be

inactive. Even though Q5 is on, there is no collector current flowing into Q11. Therefore, all the collector current of Q5 flows into the base of Q10 (SCR gate). This current flow allows both Q10 and Q9 to turn on and remain on even if the gate drive is removed.

With Q10-Q9 on, the timing capacitor CT (pin 3) and the base of Q21 (inverting input of comparator Q21-Q22) are shorted to ground. This turns on transistor Q22, which activates current mirror Q23, Q24, Q25, Q26, and Q27. With collector current flowing from Q26 and Q27, transistors Q28 and Q turn on, which causes the outputs (RESET and RESET, respectively) to become active.

High RENN

When $\overline{\text{RESIN}}$ (pin 2) is tied high, transistor Q17 draws very little current, and Q16 is off. The state of the SCR (Q10-Q9) now depends only on the output of comparator Q7-Q8, which is determined by the SENSE IN voltage.

If the SENSE IN voltage is lower than the threshold, Q7 is off, disabling current mirror Q1, Q2, Q3, and Q4. In addition, Q8 is on, causing current mirror Q5-Q6 to be active. With Q4 off, no current flows into Q12 and mirror Q11-Q12 is disabled. Collector current from Q5 again flows into the SCR gate (Q10 base) to turn it on. CT discharges. This turns on Q22 allowing base current to flow into Q28 and Q29 and turning the outputs on (active).

Outputs Inactive

If the voltage at SENSE IN is greater than the threshold (with $\overline{\text{RESIN}}$ still tied high), Q7 turns on and Q8 is shut off. This activates mirror Q1, Q2, Q3, and Q4 and disables mirror Q5-Q6. With collector current flowing from Q4 into Q12, current mirror Q11-Q12 is on. Since Q5 is off, Q11 pulls current from the gate of the SCR and forces the SCR to turn off (gate turn off).

With Q9 off, collector current from Q3 charges CT to a value above the base voltage of Q22, after the time delay t_d . At this point, Q22 turns off, disabling mirror Q23, Q24, Q25, Q26, and Q27. This removes the base drive from Q28 and Q29 and places the outputs at their inactive (off) state.







Design Considerations

TL77XXA ELECTRICAL SPECIFICATIONS

The TL77XXA supply voltage supervisors offer accurate, reliable performance over a wide range of operating conditions. The TL77XXA maximum allowable ratings, recommended operating conditions, and electrical characteristics are presented in the following tables.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, VCC (see Note 1) 20 V
Input voltage range at RE_10.3 V to 20 V
Input voltage at SENSE: TL7702A (see Note 2)0.6 V to 6 V
TL7705A
TL7709A
TL7712A
TL7715A
High-level output current at RESET30 mA
Low-level output current at RESET 30 mA
Operating free-air temperature range: TL77XXAI25°C to 85°C
TL77XXAC 0°C to 70°C
Storage temperature range65°C to 150°C

NOTES: 1. All voltage values are with respect to the network ground terminal.

2. For the TL7702A, the voltage applied to the SENSE terminal must never exceed V_{CC}.

recommended operating conditions

		MIN	MAX	TINU
Supply voltage, V _{CC}		3.6	18	V
High-level input voltage at F.E, VIH		2		V
Low-level input voltage at F = , VIL			0.8	۷
	TL7702A	0	†	
	TL7705A	0	10	
Input voltage at SENSE, VI	TL7709A	0	15	V
	TL7712A	0	20	
	TL7715A	0	20	
High-level output current at ···· - · , IOH			-16	mA
Low-level output current at - = :: ; IOL			16	mA
	TL77XXAI	-25	85	00
Operating ree-air temperature range, 1A	TL77XXAC	0	70	

[†] For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed $V_{CC} - 1$ V or 6 V, whichever is less.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYPT	MAX	UNIT	
Vон	High-level output voltage	RESET		IOH = -16 mA	V _{CC} -1.5			v
VOL	Low-level output voltage			I _{OL} = 16 mA			0.4	v
V _{ref}	Reference v	oltage		$T_A = 25^{\circ}C$	2.48	2.53	2.58	V
			TL7702A		2.48	2.53	2.58	V 4 V 3 V 3 7 V 1 3 7 V 1 3 7 V 1 3 7 V 1 4 7 V 1 4 7 V 1 5 7 V 1 5 7 V 1 5
			TL7705A		4.5	4.55	4.6	
٧ _T	Threshold	SENSE	TL7709A	$V_{CC} = 3.6 V \text{ to } 18 V,$	7.5	7.6	7.7	
	voltage		TL7712A	$1A = 25^{\circ}C$	10.6	10.8	11	
			TL7715A		13.2	13.5	13.8	
			TL7702A	+	1	10		mV
		1 1	TL7705A			15		
$V_{T+} - V_{T-}$	Hysteresis [‡]	SENSE	TL7709A	$V_{CC} = 3.6 V \text{ to } 18 V,$		20		
			TL7712A	$1A = 25^{\circ}C$		35		
			TL7715A			45		
		DECINI		$V_{I} = 2.4 V$ to V_{CC}			20	
h	Input	RESIN		$V_{I} = 0.4 V$			-100	μA
	content	·	TL7702A	VI = Vref to VCC - 1.5 V		0.5	2	
юн	High-level output current	RESET		V _O = 18 V			50	μА
IOL	Low-level output current	RESET		$V_{O} = 0$			-50	μA
lcc	Supply current			All inputs and outputs open		1.8	3	mA

[†] All typical values are at $T_A = 25^{\circ}C$. [‡] Hysteresis is the difference between the positive-going input threshold voltage, V_{T+} , and the negative-going input threshold voltage, VT-.

Design Considerations

4

switching characteristics

	PARAMETER	TEST CO	NDITIONS	MIN	TYP [†]	MAX	UNIT
^t w1	Pulse duration, SENSE	$V_{IH}^{\ddagger} = V_{Tmax} + 300 \text{ mV},$ $V_{IL}^{\ddagger} = V_{Tmin} - 300 \text{ mV}$			0.5		μs
tw2	Pulse duration at RESET and	$C_T = 0.1 \ \mu F$			1.3		ms
^t pd	Propagation delay from RESIN to RESET	V [‡] = 5 V,	C1 = 100 pF		5		μs
t _r	Rise time, RESET and RESET	$V_{l}^{\ddagger} = 5 V,$ R1 = 4.7 k Ω	C1 = 100 pF,		1		μs
t _f	Fall time, RESET and RESET	$V_l^{\ddagger} = 5 V_l$ R1 = 4.7 k Ω	C1 = 100 pF,		1		μs

[†] All typical values are at $T_A = 25^{\circ}C$. [‡] Voltages listed are at the SENSE input.

Application Examples

This section describes several sample applications for the TL77XXA series of supply voltage supervisors. The sample applications are as follows:

- 1. Generating a Reset
- 2. Generating Dual Reset Signals
- 3. TL77XXA Supply Voltage Supervisors in Multiple Supplies
- 4. Speeding Up TL77XXA Output
- 5. Slowing the SENSE IN Glitch Response
- 6. Connecting a TL77XXA as an Oscillator
- 7. Building a Watchdog Circuit
- 8. The TL77XXA as a Retriggerable One-Shot Circuit
- 9. Connecting VCC of the TL77XXA to a High Voltage Line
- 10. Monitoring AC and Unregulated DC Voltages
- 11. TL7705A in a Battery-Buffered Memory System
- 12. Eliminating Undefined States of TL77XXA Outputs
- 13. Sensing Different Voltage Thresholds
- 14. Preventing Voltage Above V_{CC} -1 at SENSE IN of the TL77XXA

Generating a Reset

The simplest application of a TL77XXA supply voltage supervisor is its use as a reset generator. A reset signal must be generated in microcomputer or microprocessor systems to properly initialize the system to a known state during power-on and protect the system memory when the system power supply is below the operational range.

The TL77XXA supply voltage supervisor can be used in microcomputer or microprocessor equipment to generate a reset. By connecting the RESET output of the TL77XXA to the RESET input of the microcomputer or microprocessor system, an accurate reset pulse is generated when fault conditions occur in the power supply being monitored.

Microprocessor Applications

The microprocessors with which the TL77XXA can interface fall into two categories according to whether they interface directly or indirectly with the TL77XXA. The following table lists examples of microprocessors in each category.

Direct InterfacingIndirect InterfacingMC6800MC68000R6502Intel 8088TMS7040Intel 80286Intel 8085TMS320Intel 801887-80

Interfacing the TL77XXA supply voltage supervisor directly with a microprocessor is a relatively straightforward process. Interfacing it indirectly with a microprocessor is similar, but requires an additional consideration.

Direct Interfacing

Microprocessors in the first category, such as the MC6800, can be directly interfaced with the TL77XXA supply voltage supervisors as shown in Figure 7. Both the V_{CC} and SENSE IN inputs are tied to the microprocessor system supply line, so that the voltage being monitored at SENSE IN is the system supply voltage. The $\overline{RI} \ N\overline{N}$ input is also tied to the supply line.



Figure 7. Microprocessor to TL77XXA Direct Interface

A small capacitor connected from the REF output to ground is required to minimize the effects of system noise, and provide a stable reference. Another capacitor $C_{\rm T}$ determines the delay between the end of the fault condition and the return of the RESET output to its inactive state.

The system is forced into a defined state when a high-to-low transition is detected on the RESET input of the microprocessor.

Indirect Interfacing

The microprocessors in the second category, such as the 68000, the 8088, etc., cannot be interfaced directly with the TL77XXA supply voltage supervisor because a clock generator precedes the microprocessor as shown in Figure 8.

The clock generator must generate the proper logic-reset signal (with a low external pulse) during power-fault conditions. The high-to-low transition of the clock

generator $\overrightarrow{RI} \times \overrightarrow{T}$ output must be synchronized to the system clock. When the clock generator $\overrightarrow{RI} \times \overrightarrow{T}$ input is low, the RESET output goes high after a one to two clock cycle delay, due to the synchronization of RESET to the system clock.





Generating Dual Reset Signals

A TL77XXA supply voltage supervisor can be used in a system that requires both low-active and high-active reset signals. Figure 9 shows a circuit that uses a TL7705A to send interrupt signals to a microcomputer and to read-only-memory (ROM). When a



Figure 9. TL7705A Interrupt to Microprocessor and ROM

power failure occurs, RESET goes high and \overrightarrow{RESET} goes low. $\overrightarrow{R1} \lor \overrightarrow{I}$ resets the microcomputer; RESET sets the ROM to a standby mode. The microcomputer output is also used to generate a signal during a reset. This signal is sent to the ROM.

TL77XXA Supply Voltage Supervisors in Multiple Supplies

Several TL77XXA supply voltage supervisors can be used in systems that have various supplies and that require monitoring of the supplies for proper operation. Figure 10 shows a circuit that uses two TL7712A supply voltage supervisors and one TL7705A to monitor 12 V, -12 V, and 5 V supplies.

The $\overline{\text{RESET}}$ outputs of both TL7712A supervisors are sent to the $\overline{\text{RESIN}}$ input of the TL7705A, which is high during normal operation. SENSE IN of the TL7705A is tied to the 5-V line. The $\overline{\text{RESET}}$ output of the TL7705A serves as the system interrupt signal. When one of the three supervisors detects a fault, an interrupt signal is generated.



Figure 10. TL7705A Supply Voltage Monitor Circuit

Speeding Up the TL77XXA Output

The rise and fall time of the TL77XXA output can be shortened with only a minor modification to the circuit.

The circuit shown in Figure 11 can be used in applications where the normal \overrightarrow{RESET} output pulse transition time is too slow. Connecting a transistor-inverter circuit to the RESET output provides a \overrightarrow{RESET} at its collector. This circuit results in a faster response because the saturation region of Q1 is avoided by clamping its base-collector junction. Under normal operating voltage levels RESET is inactive, Q1 is ensured to be off by RB, and $\overrightarrow{R1}$. \overrightarrow{IT} is high. When a voltage drop occurs at SENSE IN, RESET goes high. This turns on Q1 which pulls \overrightarrow{RESET} low.





Slowing the SENSE IN Glitch Response

An RC reset network can be connected to the TL77XXA supply voltage supervisor to slow the supervisor response to voltage drops. The TL77XXA supply voltage supervisors are designed to detect voltage drops of less than 1 μ s in duration. The circuit shown in Figure 12 can be used in applications where this fast response is not desired, such as very noisy environments.

With an external RC reset network connected to the SENSE IN pin, the device normal response is delayed by an amount t_A , such that

 $t_A = C_A X RA$

where: t_A is in seconds C_A is in farads RA is in ohms

The value of RA should be small (less than 22 Ω) so that RA will not affect the SENSE IN threshold voltage.



Figure 12. Circuit to Slow SENSE IN Glitch Response

Connecting a TL77XXA as an Oscillator

The TL77XXA can be connected so that it will perform as an oscillator. Figure 13 shows a TL77XXA p:: $\bar{\Gamma}$ ming an oscillator function. When power is turned on, both outputs are active (RLSL $\bar{\Gamma}$ low, RESET high) and capacitor <u>C</u> is charging. When the voltage on C reaches the SENSE IN threshold, RESET and RESET change states. At this time, the capacitor begins to discharge until SENSE IN voltage falls below the threshold and the outputs become active again. The cycle is then repeated.

A sawtooth waveform is generated at the junction of RA and RB. Because the SENSE IN voltage crosses the threshold regularly, RESET alternates between high and low. In this configuration, \overrightarrow{RESET} provides a square wave suitable for main clock output. The duty cycle of the square wave depends upon the time that the sawtooth wave is above and below the threshold.

The rise and fall time of the sawtooth output, as well as its general shape, is determined by the values of capacitor C, the two resistors RA and RB, and the timing capacitor C_{T} .



Figure 13. TL77XXA Oscillator Circuit

Building a Watchdog Circuit

A TL7702A and a TL7705A can be used in building a watchdog circuit that monitors incoming pulses and generates a reset whenever an input pulse is absent. Figure 14 shows a TL7702A and a TL7705A in a watchdog circuit. If the microcomputer is operating, the watchdog input is continuously strobed by input pulses that, through C1 and D1, charge C2. To allow C2 to receive an equal charge from each input pulse, C1 is discharged through RA between pulses.

In the absence of input pulses, C2 discharges through RB; when this occurs, the voltage at the TL7702A SENSE IN drops below its threshold and a reset signal is generated. This reset signal causes RESIN of the TL7705A to go low, in turn causing its RESET to go low, which provides a reset signal to the microprocessor or computer.

When the supply voltage (V_{CC}) drops below its operational range, the TL7705A also generates a \overrightarrow{RESET} to the microcomputer.

When the string of <u>input pulses</u> is resumed, C2 again charges to a value above the TL7702A threshold and RESET of the TL7705A becomes inactive.

Diode D2 is connected from the TL7702A RESET output to SENSE IN to allow C2 to be charged during power-up. For proper operation, the value for C_{T1} must be less than that of C_{T2} .





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The TL77XXA as a Retriggerable One-Shot Circuit

Figure 15 shows the TL77XXA used as a retriggerable one-shot circuit. In this application, complementary active outputs (from RESET and RESET) are obtained every time the RESIN input is triggered, the trigger pulse duration plus t_d equals the one shot pulse duration, and SENSE IN is tied to V_{CC}.

The outputs become active when $\overline{\text{RESIN}}$ passes from a high to a low state. Outputs remain active if the input has a period less than the delay time, t_d.

In this configuration, the **RESIN** input can be used as a panic button to provide an interrupt signal regardless of system condition.



Figure 15. TL77XXA Retriggerable One-Shot Circuit

Connecting VCC of the TL77XXA to a High-Voltage Line

The TL77XXA supply voltage supervisors can be used to monitor the output of a regulator and to generate a reset even if the sensed voltage line drops to zero. Figure 16 shows such a circuit.

The V_{CC} input is fed from the input side of the regulator so that it is not affected by failures in the regulator. Because the regulator input voltage cannot be 35 V, a TL431 programmable reference is used to drop the voltage to a level that is compatible with the TL77XXA. Therefore, the RESET output remains active with 0 V at SENSE IN, provided that there is enough voltage at the regulator input.



Figure 16. V_{CC} of the TL7715A Connected to a High-Voltage Line

Monitoring AC and Unregulated DC Voltages

The TL77XXA can be used in a voltage regulator system to monitor either the ac input line to the power supply or the unregulated dc input. To avoid undefined operations, the point monitored must be one at which a power loss can be detected as quickly as possible.

When a TL77XXA supply voltage supervisor is used to supervise a voltage regulator system, the regulator output should not be used as a sensing point. The preferred points in a regulator system, because they respond more quickly to a system power loss, are the ac input line to the power supply and the unregulated dc input to the regulator.

When the ac voltage is being monitored, the output of the input transformer can be monitored by a TL7702A, see Figure 17. Resistors RA and RB are selected for the desired trip point above the regulator required minimum input voltage. Diode D1 acts as a half-wave rectifier. Capacitor C1 filters this half-wave signal so that a reset does not occur at every half cycle. Capacitor C1 also introduces a delay between the ac power loss and the reset signal. When a drop in the ac line voltage is detected, the dc value of the rectified signal drops. The values of RA and RB should be such that any change greater than the maximum allowable drop will be detected.



Figure 17. TL7702A Circuit for Monitoring Input-Transformer Output

Figure 18 shows a TL7702A used to monitor the unregulated dc voltage. The regulator remains within its specified output voltage rating as long as the input voltage remains within its minimum and maximum limits. During a power drop, the regulator input starts to drop before the output experiences any voltage change.

When the input voltage begins to drop, the ripple voltage also starts to drop. Resistors RA and RB should be selected so that the threshold of the TL7702A SENSE IN voltage is below the ripple voltage at the desired detection level (which should be above the regulator minimum input voltage). The TL7702A therefore warns of a power failure at the regulator input before the regulator output is significantly affected.



Figure 18. TL7702A Circuit for Monitoring Unregulated DC Voltage

The TL7705A in a Battery-Buffered Memory System

The TL7705A can be used in a circuit that protects the memory contents of a microprocessor against spikes on the "write" line after failure of the line voltage. Figure 19 shows the TL7705A in a battery-buffered memory system. A switch consisting of transistor Q1 and diode D1 is inserted on the memory chip select line. If SYSTEM RESET (tied to RESIN) is high, the $\overline{RI} \sim I \overline{T}$ output of the TL7705A is high, which turns on transistor Q1.

When a power failure occurs, SYSTEM RESET goes low (triggering the TL7705A) and $\overrightarrow{\text{RESET}}$ goes low (turning off Q1 and reverse-biasing diode D1). Therefore, the chip select input of the memory (CS) is isolated from the chip-select line.

Eliminating Undefined States of TL77XXA Outputs

An external circuit can be connected to the TL77XXA supply voltage supervisor in applications where the state of the TL77XXA outputs is to remain defined down to the point at which V_{CC} is 0 V. Figure 20 shows an external circuit that, when connected to the TL77XXA, eliminates undefined states of the TL77XXA outputs during power-up and power-down.



Figure 19. TL7705A in a Battery-Buffered Memory System

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The RESET output is used to switch transistor Q1 on or off. Switching Q1 on causes the collector (the RES output) to go high. Switching Q1 off causes the collector to go low. When V_{CC} is above minimum operational value, RESET is at a low voltage. This condition turns on Q1 and causes RES to go high. As V_{CC} drops, the RESET output keeps Q1 turned off. This causes the RES output to remain active down to the point at which V_{CC} is 0 V.



Figure 20. Elimination of Undefined States

Figure 21 shows a circuit application that eliminates the undefined state of the TL77XXA outputs by using a p-channel depletion JFET.

To ensure that the transistor is switched off when the supply voltage reaches a nominal value, the gate must be more positive than the source. The circuit in Figure 21 provides the advantage of less power dissipation than the circuit in Figure 20.

Sensing Different Voltage Thresholds

The TL77XXA supply voltage supervisors are capable of detecting voltage drops of 10%. The TL7702A can be used in a modified circuit to detect even smaller voltage drops.

The threshold voltage at SENSE IN of the TL77XXA is designed to detect a voltage drop of approximately 10% below the rated voltage. The TL7705A, for example, is for use in 5 V systems and the threshold voltage at its SENSE IN is typically 4.55 V. The TL7709A, the TL7712A, and the TL7715A have typical threshold voltages at SENSE IN of 7.6 V, 10.8 V, and 13.5 V, respectively.



Figure 21. Elimination of Undefined State Using P-Channel Depletion JFET

In applications where a 10% drop in voltage is harmful and therefore a drop of 5% must be detected, the programmable TL7702A with a precision voltage divider at SENSE IN can be used as shown in Figure 22. To calculate the exact threshold voltage for the TL7702A, the following equation is used:

$$V_{S} = \frac{R1 + R2}{R2} (V_{T-})$$

where:

$$V_{T} = 2.53 V$$

For a 5-V system with a -5% detection level: V_S = 4.75 V, V_T = 2.53 V and R2 is selected as 10 k Ω . R1, therefore, is 8.775 k Ω .

Preventing Voltage Above V_{CC} - 1 at SENSE IN of the TL7702A

The TL7702 must be used in a circuit that ensures that the voltage at SENSE IN never exceeds the recommended voltage. Figure 23 shows a circuit that clamps the voltage at SENSE IN to a value below V_{CC} .







Figure 23. Clamp Circuit for TL7702A SENSE IN

To select the resistor values, a minimum V_{CC} (V_{CCmin}) and a maximum SENSE IN voltage (V_{Tmax}) must be selected. Resistors RB and RC are chosen such that:

$$V_{\text{Tmax}} = \frac{\text{RC}}{\text{RB} + \text{RC}} V_{\text{CCmin}} + V_{\text{diode}}$$

With this accomplished, the value for RA is calculated for the desired trip point $\left(V_{S}\right)$ such that:

$$V_{\text{Tnom}} = \frac{\text{RC}}{\text{RA} + \text{RB} + \text{RC}} \quad (V_{\text{S}})$$

where:

 $V_{Tnom} = 2.53 V$

4 Design Considerations

500-W, 80-A, Off-the-Line, Half-Bridge Converter, Switching Power Supply



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Introduction

The power supply was designed and built for the purposes of demonstrating and evaluating switching power supply components under operating conditions. The primary consideration of the mechanical design was to facilitate instrumentation, not particularly to achieve a compact modular design.

The half-bridge circuit configuration was selected because it is one of the more common types of converter circuits in use today. The half-bridge power converter is very popular because of its many advantages which include: (1) voltage stress on the power switches is no greater than the rectified power mains voltage; (2) power transformer dc core flux can be eliminated by the use of a capacitor in series with the primary of the power transformer; (3) reverse energy created by the transformer leakage inductance can be commutated back to the dc bus and therefore need not be absorbed by the power switches; and (4) a simple power transformer primary is required.

Although the half-power bridge converter is very popular, it does require additional consideration for the base drive of the power switches. These considerations include switching speed and isolation requirements. This work details the construction of such a base driver section that very successfully interfaces between a TL494 control circuit and the bases of the TIPL755 power inverter transistors.

The discussion will begin with a power supply specification and then proceed with the detailed design considerations.

The selection of the operating frequency is a compromise between physical size of the magnetics and filters and loss of efficiency due to increased switching losses. The frequency of this design was set at 20 kHz.

Power Supply Definitions

Specifications

Regulated Output Power:

1) +5 volts \pm 0.5% at 80 A 2) +10 volts \pm 2% at 2.5 A 3) +26 volts \pm 2% at 2 A. Ripple: Shall be \leq 125 mV peak-to-peak on all outputs Input Power: 120 V or 240 V, 1 ϕ , 60 Hz Efficiency: 65% minimum at full load **Protection Circuits:**

1) All regulated outputs shall be current limited.

2) The 5 V/80 A output shall have overvoltage protection.

Input Voltage Range:

	120-V ac Input	240-V ac Input
Minimum	96	192
Nominal	120	240
Maximum	132	264

Holdup Time, th: 10 ms (time outputs remain in regulation following loss of input power)

Block Diagram

A block diagram of the half-bridge converter switching power supply is shown as Figure 1.

Half-Bridge Converter Description

The idealized waveforms of Figure 2 define the voltage and current characteristics of the Power Converter Section.



Figure 1. 500-W, 80-A Half-Bridge Converter Switching Power Supply



HALF-BRIDGE INVERTER IDEALIZED WAVEFORMS



HALF-BRIDGE POWER CONVERTER SECTION

Figure 2. Half-Bridge Inverter Waveforms and Power Converter Section

Design Considerations

Preliminary Calculations

Input Voltage Range

The input rectifiers and filter capacitors are designed to operate as a standard fullwave rectifier with 240-V ac input and as a doubler with 120-V ac input (Figure 3). Switch S2A is closed for the 120-V ac operation.



Figure 3. Input Filter Circuit

Based on the specification, the theoretical minimum converter voltage, V_{CC} , with 120-V ac input and switch S2A closed is:

$$V_{CC} = \sqrt{2} \times 96 \ V_{rms} \times 2 = 271 \ V \tag{Eq.1}$$

By allowing 10 V for EMI filter, surge limiting, thermistor, rectifier, and wiring losses, the value of V_{CC} is reduced to 261 V. This value represents V_{CC1} in Figure 3 and Equation 2. From the specification, the holdup time, t_h , is 10 ms. The value of minimum filter capacitance is calculated by allowing V_{CC2} to be 220 V.

$$C = \frac{2 P_{IN} t_{h}}{\left[(V_{CC1})^{2} - (V_{CC2})^{2} \right]}$$
(Eq.2)

The term P_{IN} is the input power supplied to the converter and based on a 65% efficiency, it is estimated to be:

$$P_{IN} = \frac{5 \text{ V} \times 80 \text{ A} + 10 \text{ V} \times 2.5 \text{ A} + 26 \text{ V} \times 2 \text{ A}}{0.65}$$

 $P_{IN} = 734 W$

Therefore:

$$C = \frac{2 \times 734 \text{ W} \times 10 \times 10^{-3} \text{s}}{\left[(261 \text{ V})^2 - (220 \text{ V})^2\right]} = 744 \ \mu\text{F}$$
(Eq.3)

The capacitors C1 and C2 are connected in series for 240 V_{rms} operation, so the minimum value required of each is $2 \times C$ or $\approx 1488 \ \mu F$.

Power Transformer Turns Ratio Estimate

Equation (4) is used to estimate the transformer turns ratio.

$$N = \frac{NP}{NS} = \frac{VP}{VS} = \frac{\delta\left[\frac{V_{CC}}{2}\right]}{V_{O} + V_{D} + V_{W} + V_{REG}}$$
(Eq.4)

where

Np = number of turns on primary

- N_S = number of turns on secondary
- V_{P} = transformer primary voltage [or (V_{CC})/(2)]
- δ = duty cycle (80% assumed)
- V_O = regulated output voltage

 V_S = transformer secondary voltage

- V_D = rectifier conduction voltage
- V_W = power supply wiring voltage
- VREG = linear regulator voltage

Turns Ratio Calculation for +5 V Output

Assume:

$$V_{O} = 5 V$$

$$V_{D} = 0.6 V$$

$$V_{W} = 0.1 V$$

$$V_{CC} = 220 V$$

$$\delta = 0.8$$

$$N = \frac{N1}{N2} = \frac{0.8 \left[\frac{220 V}{2}\right]}{5 V + 0.6 + 0.1 V} = 15.43 \text{ max}$$

Turns Ratio Calculation for +10 V Output

Assume:

$$V_O = 10 V$$

 $V_D = 0.7 V$
 $V_W = 0.1 V$
 $V_{REG} = 5 V$
 $V_{CC} = 220 V$
 $\delta = 0.8$
 $N = \frac{N1}{N3} = \frac{0.8 \left[\frac{220 V}{2}\right]}{10 V + 0.7 V + 0.1 V + 5 V} = 5.56 \text{ max}$

Turns Ratio Calculation for +26 V Output

Assume:

$$V_O = 26 V$$

 $V_D = 0.7 V$
 $V_W = 0.1 V$
 $V_{REG} = 5 V$
 $V_{CC} = 220 V$
 $\delta = 0.8$
 $N = \frac{N_1}{N_4} = \frac{0.8 \left[\frac{220 V}{2}\right]}{26 V + 0.7 V + 0.1 V + 5 V} = 2.76 \text{ max}$

Pulse Engineering Transformer PE63203 has turns ratio N1: N2: N3: N4 of 14: 1: 3: 6 and was selected for the application (see Figure 2).

Based on the PE63203 transformer turns ratio of (N1)/(N2) = (14)/(1) = 14, the converter duty cycle, δ , is calculated for various 120-V ac input voltages (assume 35-V filter loss):

Input (V)	δ
96	0.68
120	0.52
132	0.42

Power Transformer Current Calculations

The total power provided to the transformer secondaries is

 $P_{(sec)} \approx 80 \text{ A} (5 \text{ V} + 0.6 \text{ V} + 0.1 \text{ V})$ +2 A (26 V + 0.7 V + 0.1 V + 5 V)+2.5 A (10 V + 0.7 V + 0.1 V + 5 V)

 $P(sec) \approx 559.1 \text{ W}.$

Assuming the inverter transformer efficiency is 95%, the inverter input power is

$$P(INV) \approx \frac{P(sec)}{0.95} \approx \frac{559 W}{0.95} \approx 588 W.$$

d Design Considerations

Under low line conditions, the maximum duty cycle is 0.68 and the voltage applied to the transformer primary Vp is

$$\frac{V_{CC}}{2} = \frac{236}{2} = 118 V$$

The peak primary current is

$$Ip \approx \frac{P(INV)}{Vp} \approx \frac{588 \text{ W}}{0.68 \times 118 \text{ V}} \approx 7.3 \text{ A}.$$

The actual peak current is estimated to be about 10% higher or ≈ 8 A due to magnetizing current in the inverter transformer and current variations in the output filter choke.

Efficiency Estimate

Regulated Output Power =
$$P_O$$

 $P_O = 5 V \times 80 A + 10 V \times 2.5 A + 26 V \times 2 A$

 $P_{O} = 488 W$

Input Power for 65% efficiency = PIN.

$$P_{IN} = \frac{P_O}{0.65} = \frac{477 \text{ W}}{0.65} = 734 \text{ W}.$$

A power of 588 W has already been accounted for, so 146 W remains for power transistors, input rectifiers and wiring losses.

Output Filter Design

Choke Inductance Calculations

The output inductor is selected to limit the ripple current the output capacitors must filter. Equation (5) is used to calculate the required inductance, L, once the Δi_L is defined. A Δi_L is equal to 15% of the maximum output current, IQ, is used in this design.

$$L = \frac{(V_O + V_D + V_W + V_{REG}) (1 - \delta)t}{\Delta i L}$$
(Eq.5)

All Equation (5) symbols have been previously defined in Preliminary Calculations except t, which is the clock period of 25 μ s. δ is the converter duty cycle of 0.42, previously calculated, for 132-V ac input voltage.

Filter Inductance Calculations for +5 V Output

$$\Delta i_{L} = 0.15 \times 80 \text{ A} = 12 \text{ A}$$

$$L1 \ge \frac{(5 \text{ V} + 0.6 \text{ V} + 0.1 \text{ V})(1 - 0.42)25 \times 10^{-6}\text{s}}{12 \text{ A}}$$

$$L1 \ge 6.9 \ \mu\text{H}$$

Filter Inductance Calculations for +10 V Output

$$\Delta i_{L} = 0.15 \times 2.5 \text{ A} = 0.37 \text{ A}$$

$$L2 \ge \frac{(10 \text{ V} + 0.7 \text{ V} + 0.1 \text{ V} + 5 \text{ V})(1 - 0.42)25 \times 10^{-6}\text{s}}{0.37 \text{ A}}$$

$$L2 \ge 619 \ \mu\text{H}$$

Filter Inductance Calculations for +26 V Output

$$\Delta i_{L} = 0.15 \times 2 \text{ A} = 0.3 \text{ A}$$

$$L3 \ge \frac{(26 \text{ V} + 0.7 \text{ V} + 0.1 \text{ V} + 5 \text{ V})(1 - 0.42)25 \times 10^{-6} \text{ S}}{0.3 \text{ A}}$$

L3 \geq 1537 μ H

Pulse Engineering laminated output inductors PE50742 (8 μ H), PE50731 (590 μ H) and PE50732 (2350 μ H) were selected for L1, L2, and L3 respectively.

Output Capacitance Calculations

Since the filter inductances have been chosen, the output capacitors can be selected to meet the ripple requirements. An electrolytic capacitor can be modeled as a series connection of an inductance, a resistance, and a capacitance. If good filtering is to be provided, the ripple frequency must be far below those at which the series inductance becomes important, so the two components of interest are the capacitance and the series resistance, R_C. To estimate the ESR ripple voltage, $\Delta V_{O(ESR)}$, it is assumed that all the ripple current in the inductor, Δi_L , flows through the output capacitance.

$$\Delta V_{O(ESR)} = \Delta i L RS$$

(Eq.6)

where

 ΔV_{O} = peak-to-peak ripple voltage due to ESR Δi_{L} = peak-to-peak ripple current RS = capacitor ESR. The peak-to-peak ripple voltage due to the capacitance is

$$\Delta V_{O(C)} = \frac{\Delta i_{L} t}{8C}$$
(Eq.7)

where

t = clock period = 25×10^{-6} s.

Capacitance Calculation for +5 V Output

The peak-to-peak output ripple must, by specification, be less than 125 mV.

The $\Delta i_{\rm L}$ will be limited by the 8 μ H filter inductor to ≤ 10.3 A.

The maximum capacitor ESR is then

$$R_{\rm S} \le \frac{0.125 \text{ V}}{10.3 \text{ A}} \le 0.012 \Omega$$

The Sprague 674D159H7R5JT5A, 15,000- μ F/7.5-V capacitor was selected because it has a maximum ESR 0.01 Ω and a maximum ripple current 12.3 A. The ripple due to capacitance is

$$\Delta V_{O(C)} = \frac{10.3 \text{ A} \times 25 \times 10^{-6} \text{s}}{8 \times 15 \times 10^{-3} \text{F}} \approx 2 \text{ mV}$$

which is negligible.

Capacitance Calculation for +10 V Output

$$R_{S} \leq \frac{0.125 \text{ V}}{0.37 \text{ A}} \leq 0.337 \Omega$$
$$C \leq \frac{0.37 \text{ A} \times 25 \times 10^{-6}}{0.125 \text{ V}} \leq 74 \mu\text{F}$$

The Sprague 672D687H020ET5C, 680- μ F/20-V capacitor was selected because it has a maximum ESR 0.08 Ω and a maximum ripple current 2.5 A.

Capacitance Calculation for +26 V Output

$$R_{S} \leq \frac{0.125 \text{ V}}{0.3 \text{ A}} \leq 0.416 \Omega$$
$$C \leq \frac{0.3 \text{ A} \times 25 \times 10^{-6}}{0.125 \text{ V}} \leq 60 \ \mu\text{F}$$

The Sprague 672D337H040ET5C, 330- μ F/40-V capacitor was selected because it has a maximum ESR 0.2 Ω and a maximum ripple current 2 A.

Magnetic Design

20-kHz Power Transformer

A ferrite "E" core with a rectangular center leg is used for the power transformer. Dimensions are shown in Figure 4. This is generally the most economical shape and is easy to wind and insulate. The core has a throughput power rating of 620 W for a 40 °C temperature rise.



Figure 4. Core Dimensions

The coil is designed with 8-mm creepage/clearance and three layers of 0.1-mm thick insulation between the primary and secondaries to comply with the most common international safety requirements for construction. The 5-V winding is wound with copper foil for low ac winding resistance at 20 kHz. To further reduce ac resistance and to minimize leakage inductance of the 5-V output, windings are arranged as shown in Figure 5. Low leakage inductance is illustrated by the low voltage overshoot at the start of "dead-time" in Figure 26. Data for this application are tabulated in Table 1.

		1/2 Primary	5 V Secondary	10 V Secondary	26 V Secondary
Turns		28	2-0-2	6-0-6	12-0-12
Conductor Size		19 AWG	2X.01 Cu	22 AWG	22 AWG
Pk Term, Voltage		100	7.96	23.57	47.1
DC Term, Voltage	5	-	5.66	16.97	33.9
DC Current, A		-	80	2.5	2.0
RMS Wdg Current	5	5.72	52.5	1.64	1.31
Throughput Power,	w	562.2	452	42.4	67.8
DC Resistance,		0.079	0.0007	0.095	0.185
AC Resistance,		0.130	0.0007	0.100	0.194
Copper Loss, W	5	2.13(1)	1.93	0.27	0.33

Table 1. Power Transformer Data

Total Cu Loss: 4.66 Core Los

Core Loss: 1.04 Total Loss: 5.7 W

(4)

1) Primary halves parallel connected.

(2) Nominal primary leakage inductance: 3 µH (5-V Secondary shorted)

(3) Primary throughput power = Σ (dc Term Voltage) × (dc Current)

(4) Transformer efficiency = 99% at 562 W throughput power.

5 At 72% duty cycle.



Figure 5. Coil Construction

20-kHz Base-Drive Transformer

The design objectives for the base-drive transformers were to provide:

- 1) Base current of 1.0 A minimum
- 2) Fast base-current rise time
- 3) Simple means to clamp dead-time voltage
- 4) Balanced secondary waveforms
- 5) Insulation for off-line operation.

To meet the first objective, ferrite E cores sized to limit temperature rise to $40 \,^{\circ}$ C were selected. E cores are easier to insulate reliably for off-line operation than toroids or more complex shapes. Units are fully encapsulated for improved insulation and thermal characteristics. The transformers will withstand 1500 Vrms dielectric strength test between base windings. Temperature rise is under $40 \,^{\circ}$ C at 1.5 A base current.

To obtain fast base-current rise time, minimum turns limited by core saturation are used and the base windings are tightly coupled to the primary. The clamp winding is also 'tightly coupled to the primary to assure effective core shorting during the dead time using the circuitry described in the Preliminary Calculations Section.

The winding sequence of Figure 6 is used to obtain coupling requirements. Base windings are multifilar wound for balanced drive.



Figure 6. Winding Sequence

A simplified equivalent is shown in circuit Figure 7 and calculations are discussed.

From catalog data for Pulse Engineering PE62129, the internal secondary resistance (R_{si}) is 0.14 Ω , yielding a typical internal voltage drop of 0.14 V/A amp of load current. Since this is usually negligible, the following are reasonable approximations:

Secondary terminal voltage (V_s) :

$$V_S \cong V_{in}/n$$
 (Eq.8)

Peak secondary current (I_S) :

$$I_{\rm S} \simeq \frac{V_{\rm S} - V_{\rm BE}}{R_{\rm b}}$$
 (Eq.9)

Note: $I_s = I_{B1}$

Solving Eq. 9 for Rb:

$$R_b = \frac{V_s - V_{BE}}{I_s}$$
(Eq.10)



NOTE: R_{si} = SECONDARY INTERNAL RESISTANCE = $R_p/n^2 + R_s$ R_b = BASE CURRENT LIMITING RESISTOR R_p = PRIMARY WINDING RESISTANCE R_s = SECONDARY WINDING RESISTANCE n = PRIMARY TO SECONDARY TURNS RATIO

Figure 7. Simplified Transformer Equivalent Circuit and Calculations

Peak primary current (Ip):

$$I_{p} = \frac{K}{n} I_{s} + \frac{V_{in} t_{on}}{L_{p}}$$
(Eq.11)

Note: K is the number of secondaries conducting at any time (secondaries assumed identical). The second term is the peak value of the current ramp due to primary inductance.

Leakage inductance impacts the rate of current rise after the load semiconductor starts conducting. Rise time (t_r) is approximately:

$$t_{\rm r} = \frac{2.2 \ \rm L_L}{\rm R_e} \tag{Eq.12}$$

Note: R_e is the effective secondary load resistance and is nonlinear. To estimate rise time, take $R_e = V_S/I_S$

Calculations for this application (Figure 7):Conditions:Circuit: Half-bridge (K = 1)Input voltage: 14 VTurns ratio: n = 3Power-on time: $t_{on} = 18 \ \mu s$ maximumPrimary inductance: $L_p = 1.25 \ mH$ Leakage inductance: $L_L = 0.85 \ \mu H$ Base-emitter voltage: $V_{BE} = 1 \ V$

Determine IB1 to obtain $R_b = 5 \Omega$

 $V_{\rm S} = 14/3 = 4.67 \text{ V}$ from Eq.8

$$I_{B1} = \frac{4.67 - 1.0}{5} = 0.73 \text{ A}$$
 from Eq.9

since $I_{B1} = I_s$

Determine peak primary current:

$$I_{p} = \frac{1}{3} \times 0.73 + \frac{14 \times 18 \times 10^{-6}}{1.25 \times 10^{-3}} = 0.24 + 0.20$$

= 0.44 A from Eq.11

Estimate base current rise time:

$$t_{\rm r} = \frac{2.2 \times 0.85 \times 10^{-6}}{4.67} = 0.4 \ \mu {\rm s} \qquad \text{from Eq.12}$$

Note: This yields $\beta \approx 10$ which is satisfactory. IB1 could be increased to 1 A at the expense of increased losses by reducing R_b to 3.5 Ω .

Waveforms for a load as shown in the equivalent circuit with $R_b = 2.5 \Omega$ and $V_{BE} = 2 V$ are shown in Figure 8.

Current Sense Inductor

From Figure 9, it can be seen that magnetizing current is "robbed" from the input current. This results in a droop of the voltage waveforms with rectangular current pulses.

Primary voltage is:

$$V_{p} = \frac{(I_{in} - I_{m}) (R_{s} + R_{ser} + R_{t})}{n^{2}}$$

If $I_m < \langle I_{in} \rangle$:

$$V_p = \frac{I_{in}(R_s + R_{ser} + R_t)}{n^2}$$

And the output voltage is:

$$V_{O} = \frac{I_{in} R_{t}}{n}$$



Figure 8. 20-kHz Base-Drive Transformer Waveform



NOTE: PRIMES FOR SECONDARY VALUES REFERRED TO PRIMARY. Figure 9. Simplified Equivalent Circuit

If the primary is one turn and the terminating resistor ohmic value equals turns, output voltage is 1 V/A of output current (scale factor). The scale factor is proportional to the terminating resistor and independent of winding and other series resistances.

For minimum output voltage droop, magnetizing current must be low. For rectangular pulses, magnetizing current is approximately:

$$I_{m} \cong \frac{V_{p} t_{on}}{L_{p}} \cong \frac{I_{in} (R_{s} + R_{ser} + R_{t}) t_{on}}{n^{2} L_{p}}$$

This neglects voltage droop.

The PE51719 has 100 turns on each side of the center tap. Resistance of each side is 2 Ω . A one-turn primary has 2- μ H inductance and will support a 4 V- μ s unipolar, or an 8 V- μ s bipolar waveform.

For this application, peak input current is 8 A and maximum t_{on} is 18 μ s. A diode is in series with the 100- Ω terminating resistor R32. Assuming 0.6-V drop, effective diode resistance is approximately 0.6 n/I_{in} = 0.6(100)8 = 7.5 Ω . Shunting of R31, R30, and Q6 is negligible. Magnetizing current is approximately:

$$I_{\rm m} \cong \frac{8(2+7.5+100)(18\times10^{-6})}{1002(2\times10^{-6})} \cong 0.79 \text{ A}$$

This results in output voltage droop of about 10%. V_{pton} is 1.75 V- μ s which is well within the 8 V- μ s rating. Droop and scale factor could be reduced by using a smaller terminating resistor.

Local Power Supply

The function of the local (auxilliary) power supply is to provide the TL494 control circuit and the base drive section with a source of regulated power. The anticipated power requirement for the TL494 is 100 mA at 15 V and the anticipated base drive section power requirement is 500 mA at 15 V. The estimated total regulated power is therefore 600 mA at 15 V. A 60-Hz transformer, rectifier, linear regulator system was selected.

The secondary voltage rating, VS, of the transformer was then calculated based on (Eq.13).

$$V_{S} = \frac{V_{D} + \Delta V_{C} + V_{REG} + V_{O}}{\sqrt{2}}$$
(Eq.13)

where

 $V_{REG} = \text{linear regulator } \Delta \text{ Voltage} = 3 \text{ V}$ $V_D = \text{rectifier voltage} = 1 \text{ V}$ $\Delta V_C = \text{filter capacitor voltage swing} = 4 \text{ V}$ $V_O = \text{regulated output voltage} = 15 \text{ V}$

$$V_{\rm S} = \frac{1 \, V + 4 \, V + 3 \, V + 15 \, V}{\sqrt{2}} = 16.3 \, V {\rm rms}$$

The nearest commercial transformer secondary voltage value to 16.3 V is probably 24 V, therefore the wattage rating of the 60-Hz transformer should be 14.4 W, i.e.,

$$VA = (24 V) (0.6 A) = 14.4 W.$$

The input filter capacitor, C10, minimum value was determined to be 846 μ F based on (Eq.14). A 1000- μ F/50-V capacitor was selected.

$$C10 = \frac{2 \times P_{IN} \times t_{h}}{[(v_{CC1})^2 - (v_{CC2})^2]}$$
(Eq.14)

where

 $P_{IN} = 0.6 \text{ A} \times 18 \text{ V} = 10.8 \text{ W}$ th = hold-up time = 10×10⁻³s V_{CC1} = $\sqrt{2} \times 24 \text{ V} = 33.9 \text{ V}$ V_{CC2} = $\sqrt{2} \times 24 \text{ V} - 4 \text{ V} = 29.9 \text{ V}$

Control Circuit

Description

The TL494 integrated circuit (Figure 10) was selected for the control of the power supply over a discrete design to take advantage of the lower component count with the TL494.

In addition to the basic functions of oscillator, pulse-width modulator, and error amplifier, the circuit also provides independent dead-time control and overcurrent detection.

The TL494 supply voltage can be varied in the range 7 V – 40 V. The reference voltage developed on the integrated circuit is 5 V \pm 5% and is set by a bandgap reference giving excellent immunity to supply and temperature variation.

The TL494 also has an output control logic feature which allows single-ended (90% max duty cycle) or push-pull operation (45% max duty cycle at each output).

Oscillator

The TL494's oscillator frequency is programmed with an external capacitor and an external resistor, pins 5 and 6. The oscillator clock frequency, f_{op} , must be set at 40 kHz for the converter to operate at the specified 20 kHz.

$$f_{op} = \frac{1}{2 R_T C_T}$$
(Eq.15)

Choose $C_T = 0.001 \ \mu F$ and calculate R_T .

$$R_{T} = \frac{1}{2 \times 20 \times 10^{3} \times 0.001 \times 10^{-6}}$$

= 25 kΩ

Dead-Time Generator

The duty cycle must not be limited to less than 68% or the supply may not be able to output rated voltage at low input line voltage. It is also important to limit the maximum duty cycle to 86% or less to allow the TIPL755 power switches 3.5 μ s of storage time. An 80% duty cycle design was selected. By choosing R23 = 1 k Ω , R22 was calculated to be 9 k Ω .

$$\frac{t}{t_{d}} = \frac{3 V}{0.1 V + 5 V \left[\frac{R23}{R23 + R22}\right]}$$
(Eq.16)

where

t = 25 μ s = clock period t_d = 5 μ s = dead time R₂₃ = 1 k Ω

The dead-time generator circuit is shown in Figure 11.



Figure 10. TL494 Block Diagram and Pin Assignments

4-200

Design Considerations



Figure 11. Dead-Time Generator

Error Amplifier

The error amplifier (Figure 12) compares a sample of +5-V output to a voltage reference and adjusts the pulse-width modulator to maintain the proper output. It also contains the compensation input for the network which shapes the frequency response of the regulator so that it is stable over the range of the line and load variations.

Protection Networks

Soft-Start Circuitry

In order to reduce the stress on the TIPL755 power switches at power supply startup, it is necessary to reduce the startup surge which is otherwise seen as the output filter capacitors charge.

By applying a negative slope waveform to pin 4 of the TL494's dead-time comparator, this "soft-start" characteristic is achieved, allowing the pulse width at the output stage to increase slowly (Figure 13).

. The soft-start timing capacitor is selected to provide a time constant, t_{const} , which is approximately one-third the desired output rise time, t_r , of 50 ms.

(Eq.17)

$$t_{const} = 1/3 t_r = \frac{(C15) (R22 \times R23)}{[R22 + R23]}$$

or

$$C15 = \left[\frac{1}{3} t_r \right] \left[\frac{R22 + R23}{R22 \times R23} \right]$$

C15 is calculated to be 18 μ F

where

 $\begin{array}{rcl} t_r &= 50 \mbox{ ms} \\ R22 &= 9 \mbox{ } k\Omega \\ R23 &= 1 \mbox{ } k\Omega \end{array}$



WHERE VR = 5 V

R14 POTENTIOMETER SET MID VALUE





Figure 13. Soft-Start Circuit

Undervoltage Protection

In the low supply condition, (V_{CC} \leq 7 V), correct operation of the control logic cannot be guaranteed even when pin 13 is correctly wired to the regulated voltage source and the pulse-steering flip-flop is enabled. Under this low voltage condition, simultaneous conduction of both outputs may occur and, of course, TIPL755 immediate destruction is certain to follow.

The circuit shown in Figure 14 is designed to cause Q5 to be turned on when $V_{CC} \leq 9.4 \text{ V}$. This Q5 on condition causes the reference voltage to be applied to pin 4 of dead-time comparator which causes both outputs to be disabled. (The TL494A has a monolithic undervoltage protection network and its use eliminates the Figure 14 circuit.)



Figure 14. Undervoltage Protection Circuit



$$V_{CC(min)} \left[\frac{R12}{R11 + R12} \right] = V_R - V_{BE(Q5)}$$
(Eq.18)

where

 $V_{CC(min)} = 9.4 V$ $V_{R} = 5 V = reference voltage$ $V_{BE(Q5)} = 0.7 V (assumed)$ $R12 = 4.7 k\Omega$

Overcurrent Protection

A current sense inductor, T4, is placed in the primary side of the power transformer, T3, so that it will be responsive to core saturation as well as provide overcurrent limiting by use of the TL494 dead-time control input (Figure 15).

The load fault primary current, Ip, chosen for the design is 8 A based on the peak primary current calculation of the Preliminary Calculations Section.

Pulse Engineering current sense inductor PE51719, when connected to a $100-\Omega$ terminating resistance, is designed to generate an output voltage, V₀, of 1 V/A. Therefore, at the 8-A fault condition, an output voltage, V₀, of approximately 8 V will be produced. At V₀ = 8 V, the voltage divider network consisting of R30 and R31 is designed to turn





on Q6 which turns on Q5. The turned-on Q5 applies the +5 V reference voltage to pin 4 of the dead-time comparator. The reference voltage on pin 4 causes the output drive to be terminated and also toggles the pulse-steering flip-flop to the other output drive prior to the completion of the oscillator period. However, both output drives are inhibited because C15 is discharged through the turned-on Q5 and this action causes a voltage to remain on pin 4 until C15 can charge through R23 according to the normal "soft-start" mode described in this section.

Overvoltage Protection Circuit

The MC3423 is used to sense an overvoltage condition at the 5-V/80-A output and will trigger the crowbar SCR2. The trip voltage is programmed at 5.3 V, reference Equation 15. See Figure 16.



Figure 16. Overvoltage Protection Circuit

$$V_{\text{trip}} \approx V_{\text{REF}} \left[1 + \frac{R36}{R37} \right]$$
 (Eq.19)

where

 $R36 = 4.7 \text{ k}\Omega$ $R37 = 5.1 \text{ k}\Omega$ VREF = 2.75 V max

The MC3423 is also programmed for a $40-\mu s$ minimum duration of overvoltage condition, t_d, before triggering, thus supplying noise immunity, reference Equation 20.

$$t_{d} \approx \left[1.2 \times 10^{4}\right] C20 \tag{Eq.20}$$

where

 $C20 = 0.0033 \ \mu F$

 $t_d = \mu s$ duration overvoltage

Any overvoltage condition that causes crowbar SCR2 to fire also causes a signal to be concurrently sent to SCR1 and it is also caused to fire. The turned-on SCR1 provides base current to Q5. Q5 turns on and provides ≈ 4 V to the TL494 dead-time control, which shuts down the converter and thereby prevents the crowbar SCR from destruction. To reset, the power supply must be turned off for at least 15 seconds.

Base Driver Section

The base driver section is designed to provide an electrical isolation interface between the TL494 control circuit and the TIPL755 power transistor switches. This driver section also provides current outputs of approximately 1 A to the bases of the power switches. It is necessary to provide about 1-A base drive in order for the TIPL755s to switch as much as an 8-A transformer primary current.

To provide the required isolation, Pulse Engineering's 20-kHz Base-Drive Transformer PE62129, with two secondaries, was selected. This transformer is designed with a 15:15:5 turns ratio and 15-V input, 5-V/1.5-A output. An important feature of this base drive transformer is that a clamp winding is provided to eliminate switching transients during the turnoff or converter "dead-time" interval. The clamp winding is shorted to ground during the converter "dead-time" by means of a 1/2 SN75413 OR driver that has its two inputs connected to the respective TL494 outputs. The TL494 is operating in a push-pull mode so that one output is high while the other is low, except during the "dead-time" interval when both emitter follower outputs are low, e.g.:

	TL494			
	(SN7541	SN75413		
	Output A	Output B	Output	
	Н	L	н	
("Dead-Time")	L	L	L	
	L	н	н	
("Dead-Time")	L	L	L	

When driving a 1-A load, the PE62129 primary current is estimated to be = 0.44 A (see the Magnetic Design Section). The maximum current of the TL494 output transistors is only 250 mA, therefore a predriver stage was needed. To meet this requirement, the ULN2066, which has a 1.5-A current rating, was selected to drive the transformer primary. Because the transformer primary is connected in a push-pull configuration operating from +15 V, the ULN2066 must switch 30 V or double the +15-V supply. The ULN2066 has a 50-V rating; therefore, an approximate 20-V safety margin exists. To provide a low impedance off-drive for a reduction of storage time and fall time of the power switches, the circuit shown in Figure 17 was incorporated into the design to provide approximately 1.5-A IB2 reverse-bias current.

Feedback Loop Stabilization

Many papers have been written concerning the mathematical analysis of feedback loop phase-gain calculations and equipment measurement techniques. Some of these papers are listed in the references. The error amplifier and loop compensation network design methods used in this report are based on techniques presented in the Texas Instruments Incorporated, *Switching Power Supply Design Student Guide*, Chicago Regional Technology Center.



Figure 17. Base Driver Section for Power Converter

This power supply system is described by a total linearized single-loop model made up of five stages, as shown in Figure 18.



Figure 18. Linearized Loop Model

Km: Pulse-Width Modulator Gain

The pulse-width modulator converts an error voltage into a drive pulse width. Its gain is the change in pulse width resulting from a change in error voltage. The modulator used in the TL494 is a comparator with a triangular wave applied to one input and the error signal applied to the other; drive command duration is equal to the time the sawtooth exceeds the error voltage. The drive pulse width changes from maximum to minimum as the error signal changes from the minimum ramp value to its maximum.

Therefore

$$Km = \frac{t_{on}(max) - t_{on}(min)}{V_{ramp}(min) - V_{ramp}(max)}$$

where

 $t_{on(max)} = maximum drive period = t = 25 \ \mu s$ $t_{on(min)} = minimum period = 0$ $V_{ramp(min)} \approx 0 \ V$ $V_{ramp(max)} \approx 3 \ V$

$$Km = \frac{25 \ \mu s}{-3 \ V} = -8.34 \ \mu s/V$$

Kc: Converter Gain

The gain of the converter is the change in output voltage relative to a change in drive pulsewidth.

$$Kc = \frac{\Delta V_0}{\Delta t_{on}} = \frac{\frac{V_{CC}}{2 n} - V_D}{t}$$

where

V_{CC} = converter input voltage = 290 V n = turns ratio = 14 V_D = rectifier drop ≈ 1 V t = clock period = 25 μ s Kc = $\frac{\frac{290 \text{ V}}{2 \times 14} - 1 \text{ V}}{25 \ \mu \text{s}}$ = 0.37 V/ μ s.

G(s): Output Filter Response

The model shown in Figure 19 is used to predict the low-pass filter response and filter break frequency, $f_{\rm f}$.



Figure 19. Output Filter Model

where

L = output choke inductance $\approx 8 \ \mu H$ C = output capacitance $\approx 15,000 \ \mu F$ Rs = wiring and choke resistance $\approx 0.01 \ \Omega$ RC = output capacitor ESR $\approx 0.006 \ \Omega$ RL = load resistance $\approx 0.0625 \ \Omega$ minimum

without going through the mathematics,

$$G(s) = \frac{V_0(s)}{V_i(s)}$$

$$= \frac{R_{C}R_{L} (s + 1/R_{c}C)/L (R_{L} + R_{c})}{s^{2} + s\left[\frac{1}{(R_{L} + R_{c})C} + \frac{R_{S}}{L} + \frac{R_{L} R_{c}}{L(R_{L} + R_{c})}\right] + \frac{R_{S} + R_{L}}{L(R_{L} + R_{c})C}$$

The open-loop response of the regulator is

$$\frac{V_{o(s)}}{V_{in}} = Km \times Kc \times G(s)$$

The filter break frequency is

$$f_{f} = \frac{1}{2 \pi \sqrt{LC}}$$

$$f_{f} = \frac{1}{2 \pi \sqrt{8 \times 10^{-6} \text{H} \times 15.000 \times 10^{-6} \text{F}}}$$

A compensation network was designed to provide a zero, f_{z1} near the filter break frequency, f_f , and a pole at a much higher frequency, f_{p2} , where the response has already gone through unity. Since very high gains at low frequencies are required for dc accuracy,

an additional pole, f_{D1}, and a zero, f_{Z2}, are required. The pole, f_{D1}, is positioned at 50 Hz to reduce the gain sufficiently for the regulator response to go through unity gain, fT, beyond the filter breakpoint but well below the regulator operating frequency, $f_0 = 20$ kHz. The zero, f_{z2} , is positioned at the filter break frequency to cancel the slope of the response due to the filter low frequency pole. The net effect is an open-loop response with a slope of approximately -20 dB/decade through unity gain, see Figure 20.



Figure 20. Frequency Response Curves

The following equations and chosen values were used to calculate the component values for the compensation network, see Figure 21.

$$f_{f} = f_{z1} = \frac{1}{2 \pi \sqrt{LC}}$$

$$f_{T} = 2000 \text{ Hz} = \frac{\frac{R13}{(R13 + R15)} \text{ Km} \times \text{Kc}}{2\pi \text{ R19 C17}}$$

$$f_{za} = 50 \text{ Hz} = \frac{1}{2 \pi (R20 + R19) \text{ C17}}$$

$$f_{p1} = 50 \text{ Hz} = \frac{1}{2 \pi [(R13 \| R15) + R16] \text{ C13}}$$

$$f_{z1} = 460 \text{ Hz} = \frac{1}{2\pi \text{ R16 C13}}$$

$$f_{z2} = 460 \text{ Hz} = \frac{1}{2\pi (R13 + R21) \text{ C16}}$$

$$f_{p2} = 8,000 \text{ Hz} = \frac{1}{2\pi [(R13 \| R15 \| R16) + R21] \text{ C16}}$$

$$f_{p3} = 40,000 \text{ Hz} = \frac{1}{2\pi (R13 \| R15 \| R16) + R21] \text{ C16}}$$

$$f_{p3} = 40,000 \text{ Hz} = \frac{1}{2\pi (R13 \| R15 \| R16) + R21] \text{ C16}}$$

$$f_{c} = 1 = 8 \mu \text{H}$$

$$C = 15,000 \mu \text{F}$$

where $L = 8 \ \mu H$ $C = 15,000 \ \mu F$ $Km = 8.34 \ \mu s/V$ $Kc = 0.37 \ V/\mu s$ $C17 = 0.02 \ \mu F$

 $C13 = 0.47 \ \mu F$

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Figure 21. Error Amplifier and Loop Compensation Network

Measurement Results and Conclusions

Measurements of load and line regulation were made at various input voltages while load conditions were changed from 5 A to 80 A at each input voltage. The overall regulation of each of the 10-V and 26-V outputs, which are regulated by linear regulators, was measured as better than 1%. The overall regulation of the 5-V, 80-A output, which is regulated by the TL494 master control, was measured as 0%. The test results are shown in Table 2.

The 40-kHz ripple of the 5-V output was measured as approximately 60 mV peakto-peak (Figure 22). The ripple across the 60-Hz input line voltage capacitors under 80-A full-load conditions was measured as approximately 11-V peak-to-peak (Figure 23).



VERTICAL: 50 mV/cm

HORIZONTAL: 2 ms/cm

 $V_{IN} = 120 V_{rms}$ $V_{CC} = 304 V dc$ LOAD = 80 A/5 V

Figure 22. The 40-kHz 5-V Output Filter Ripple



VERTICAL: 2 V/cm

HORIZONTAL: 2 ms/cm $V_{IN} = 120 V_{rms}$ $V_{CC} = 304 V dc$ LOAD = 80 A/5 V

Figure 23. The 60-Hz Input Line Filter Ripple

One of the more important accomplishments of this work was the design and a subsequent successful evaluation of the overcurrent network described in the Protection Network Section. This network, consisting in part of current sense inductor T4 that is placed in the primary side of the power transformer T3, not only proved its capability to provide short circuit protection for the 80-A output but it also eliminated the need for a capacitor to be connected in series with the primary of the power transformer T3. Usually in bridge-type converter circuits, a low ESR, high-voltage capacitor is required to be connected in series with the primary of the power transformer to provide protection against transformer core saturation due to the switching time differences of the power transistors.

VIN INPUT LINE VOLTAGE (V _{rms})	VCC LINE FILTER VOLTAGE (Vdc)	V ₀ = 5 V		V ₀ = 26 V			. V _o = 10 V			
		V _{om} (V)	l _o (A)	% REG*	V _{om} (V)	I _o (A)	% REG*	V _{om} (V)	l _o (A)	% REG*
96 237	0.07	5.00	80	0	26.03	2	0.115	10.09	2.5	0.9
	5.00	5	0	25.99	2	-0.384	10.08	2.5	0.8	
120 304	5.00	80	0	26.03	2	0.115	10.08	2.5	0.8	
	5.00	5	0	26.00	2	0	10.08	2.5	0.8	
132 335	0.05	5.00	80	0	26.03	2	0.11	10.08	2.5	0.8
	5.00	5	0	25.99	2	-0.038	10.08	2.5	0.8	

Table 2. Measured Regulation Characteristics

*% Regulation = $\frac{V_{om} - V_o}{V_o} \times 100\%$

Figure 24 shows the T3 power transformer primary current, thereby illustrating the excellent current symmetry characteristic obtained under various input voltage conditions of 96 V_{rms} , 120 V_{rms} , and 132 V_{rms} during constant 100% load.

Figures 25 and 26 of the TIPL755 power transistor's collector voltage and current characteristics illustrate the TIPL755 very fast switching speed that was obtained by use of the Base Driver Section.



VERTICAL: 2 A/cm HORIZONTAL: 10 μ s/cm V_{IN} = 96 V_{rms} V_{CC} = 237 V dc LOAD = 100% ALL OUTPUTS



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VERTICAL: 2 A/cm HORIZONTAL: 10 $\mu s/cm$ V_{IN} = 120 V_{rms} V_{CC} = 304 V dc LOAD = 100% ALL OUTPUTS



Figure 24. Power Transformer Primary Current


VERTICAL: $I_C = 2 \text{ A/cm}$ $V_{CE} = 100 \text{ V/cm}$ HORIZONTAL: 10 µs/cm $V_{IN} = 132 \text{ V}_{rms}$ $V_{CC} = 335 \text{ V dc}$ LOAD = 20 A/5 V

Figure 25. TIPL755 Power Transistor Switching Characteristics



VERTICAL: $I_C = 100\%$ $V_{CE} = 100\%$ HORIZONTAL: $1 \ \mu s / cm$ $V_{IN} = 132 \ V_{rms}$ $V_{CC} = 335 \ V \ dc$

LOAD= 20 A/5 V

Figure 26. TIPL755 Power Transistor txo Switching Characteristics

Measurements of the overall power supply efficiency were made at various input voltages, while load conditions were changed from 50% to 100% full load, at each input voltage. An efficiency of 65 to 67% was measured, see Table 3.

In conclusion, the measurement results that were obtained proved the power supply described in this report did meet or exceed all of the requirements of the Power Supply Specification.

Figure 27 shows the power supply as constructed for this report.

V _{IN} (V _{rms})	l _{IN} (A _{rms})	PIN (W)	POWER FACTOR PIN VIN × IIN	POWER OUTPUTS						
				V ₀ =5 V		V ₀ = 10 V		V ₀ = 26 V		De L De L De
				І _о (А)	P1 (W)	l _o (A)	P2 (W)	l _o (A)	P3 (W)	$\eta = \frac{r_1 + r_2 + r_3}{P_{\rm IN}}$
100	9.49	721	0.759	80	400	3	30	2	52	67
99.2	5.78	419	0.731	40	200	3	30	2	52	67
112.8	8.9	738	0.735	80	400	3	30	2	52	65
113.9	5.3	426	0.704	40	200	3	30	2	52	66
132	7.46	733	0.744	80	400	3	30	2	52	66
132	4.67	435	0.705	40	200	3	30	2	52	65

Table 3. Power Supply Efficiency and Power Factor



Figure 27. The 500-W, 80-A, Off-the-Line, Half-Bridge Converter Switching Power Supply



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References

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- 2. Peter Wilson, *The TL494/5 Switching Regulator*, A Texas Instruments Application Report, Bulletin B209.
- 3. Switching Power Supply Design Student Guide, Texas Instruments Incorporated, Semiconductor Group Regional Technology Center.

Parts List

Δ ΤΥ.	CIRCUIT DESIGNATOR	DESCRIPTION					
2	C1, C2	2500-µF, 250-V Electrolytic Capacitor, Sprague 36DX252F250BF2A					
2	C3, C4	25-μF, 25-V Electrolytic Capacitor, Sprague 500D					
2	C5,C6	0.0056-µF, 600-V Polypropylene Capacitor, Sprague 715P56296JA3					
2	C7, C8	4-μF, 400-V Polypropylene Capacitor (made up of 2 each 2-μF Sprague 735P205X9400UTL in parallel)					
1	C10	1000-µF, 50-V Electrolytic Capacitor, Sprague 674D108H050HL5A					
1	C11	270-µF, 50-V Electrolytic Capacitor, Sprague 674D277H050HE5A					
1	C12	100-µF, 50-V Electrolytic Capacitor, Sprague 672D107H050DT5C					
1	C13	0.47-µF, 100-V Mylar Capacitor, Sprague 225P					
2	C14, C19	0.01-µF, 200-V Mylar Capacitor, Sprague					
1	C15	25-µF, 12-V Electrolytic Capacitor, Sprague 500D					
1	C16	0.033-µF, 100-V Mylar Capacitor, Sprague 225P					
1	C17	0.022-µF, 100-V Mylar Capacitor, Sprague 225P					
1	C18	0.001-µF, 200-V Mylar Capacitor, Sprague 192P					
1	C20	0.0033-µF, 100-V Mylar Capacitor, Sprague 225P					
2	C23, C24	0.056-µF, 200-V Polypropylene Capacitor, Sprague 715P56392K					
1	C25	15,000-μF, 715-V Electrolytic Capacitor, Sprague 674D159H7R5JT5A					
5	C26, C28, C30, C32, C34	0.1-µF, 200-V Polypropylene Capacitor, Sprague 715P10402L					
1	C27	680-μF, 20-V Electrolytic Capacitor, Sprague 672D687H020ET5C					
1	C29	330-μF, 40-V Electrolytic Capacitor, Sprague 672D337H040ET5C					
1	D1	25-A, 600-V Bridge Rectifier, Varo VT600S					
12	D2, D3, D6, D7, D8, D9, D10, D11, D18, D19, D20, D21	1N4001 Diode					
2	D4, D5	4-A, 600-V Fast-Recovery Diode, TRW DSR5600X					
2	D12, D13	75-A, 45-V Power Schottky Diode, TRW SD75					
2	D14, D15	10-A, 200-V Fast-Recovery Diode, Varo VH248X					
1	IC1	15-V, 1.5-A Positive Voltage Regulator, TI uA7815C					

PARTS LIST (continued)

ΩΤΥ.	CIRCUIT DESIGNATOR	DESCRIPTION				
1	IC2	5-V, 1.5-A Positive Voltage Regulator, TI uA7805C				
1	IC3	Pulsewidth Modulator Control Circuit, TI TL494CN				
1	IC4	Overvoltage-Sensing Circuit, TI MC3423CP				
1	IC5	High-Current Darlington Switch, TI ULN2066B				
1	IC6	Peripheral OR Driver, TI SN75413				
2	IC7, IC8	1.5-A, 3-Terminal Adjustable Regulator, TI LM317				
1	L1	Output Inductor, 8-µH, 100-A, Pulse Engineering PE50742				
1	L2	Output Inductor, 590-µH, 4-A, Pulse Engineering PE50731				
1	L3	Output Inductor, 2350-µH, 2-A, Pulse Engineering PE50732				
1	т1	60-Hz Auxiliary Transformer, Triad-Utrad F-211Z				
1	Т2	20-kHz Base Drive Transformer, Pulse Engineering PE62129				
1	тз	20-kHz Switching Transformer, Pulse Engineering PE63202				
1	Т4	Current Sense Inductor, Pulse Engineering PE51719				
1	Z1	Line Filter, 220-V, 10-A, Pulse Engineering PE622A10				
1	R1	100-kΩ Resistor, 1/4 W, 5%				
1	R2	Thermistor, 2.5 Ω (cold), 0.045 Ω (hot), 10-A, 5%,				
		Rodan-Surge-Guard SG-7				
2	R3, R4	3.5 kΩ Resistor, 10 W, 5%				
2	R5, R7	5-Ω Resistor, 5 W, 5%				
2	R6, R8	68-Ω Resistor, 1/4 W, 5%				
2	R9, R10	50-Ω, Resistor, 12 W, 5%				
1	R11	5.6-kΩ Resistor, 1/4 W, 5%				
2	R12, R36	4.7-kΩ Resistor, 1/4 W, 5%				
2	R13, R15	12-kΩ Resistor, 1/4 W, 5%				
1	R14	Potentiometer, 1 kΩ				
1	R16	750-Ω Resistor, 1/4 W, 5%				
2	R17, R18	470-Ω Resistor, 1/4 W, 5%				
1	R19	6.8-kΩ Resistor, 1/4 W, 5%				
1	R20	130-kΩ Resistor, 1/4 W, 5%				
1	R21	1.5-kΩ Resistor, 1/4 W, 5%				
1	R22	Potentiometer, 20 kΩ				
5	R23, R33, R34, R47, R54	1-kΩ Resistor, 1/4, 5%				
1	R24	27-kΩ Resistor, 1/4 W, 5%				

PARTS LIST (continued)

ΩΤΥ.	CIRCUIT DESIGNATOR	DESCRIPTION
1	R25	Potentiometer, 10 kΩ
2	R26, R27	51-Ω Resistor, 1/4 W, 5%
2	R28, R29	330-Ω Resistor, 1/4 W, 5%
2	R30, R37	6.1-kΩ Resistor, 1/4 W, 5%
1	R31	56-kΩ Resistor, 1/2 W, 5%
1	R32	100-Ω Resistor, 1/4 W, 5%
1	R35	47-Ω Resistor, 1/4 W, 5%
1	R40	10-Ω Resistor, 1/4 W, 5%
2	R41, R42	10-Ω Resistor, 1/2 W, 5%
1	R43, R50	0.5-Ω Resistor, 2 W, 5%
2	R44, R51	1-Ω Resistor, 1 W, 5%
2	R45, R52	100-Ω Resistor, 1/4 W, 5%
2	R48, R55	82-Ω Resistor, 1/4 W, 5%
1	R49	590-Ω Resistor, 1/4 W, 1%
1	R56	1.6-kΩ Resistor, 1/4 W, 5%
2	Q1, Q3	10-A, 800-V, NPN Fast-Switching Transistor, TIPL755
2	Q2, Q4	6-A, 40-V, NPN Transistor, TIP41
1	Q5	0.2-A, 40-V, PNP Transistor, A8T3702 or MPS3702
1	Q6	0.8-A, 50-V, NPN Transistor, A8T3704 or MPS3704
2	Q7, Q9	6-A, 40-V, PNP Transistor, TIP42
2	Q8, Q10	5-A, 60-V, PNP Darlington Transistor, TIP125
1	SCR1	Sensitive-Gate Thyristor, 2N5060
1	SCR2	12-A, 100-V Thyristor, TIC126A
1	HS1	Schottky Rectifier Heat Sink, Thermalloy 6423B
1	HS2	Power Transistor Heat Sink, Thermalloy 6123B
1	HS3	Clip-On Heat Sink, Linear Regulators, Thermalloy THM 6038B
1	HS4	Power Transistor Heat Sink, Thermalloy THM 6025
1	11	Indicator Light
1	S1	Klixon 15-A Circuit Breaker, TI MC8-122-15
1	S2	Triple-Pole, Double-Throw Switch



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