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				30			TLC533A		
	1	0	13	10	45	1.0	TLC1225A	J, N	3-43
						0.5	TLC1225B		

[†] Analog/digital inputs can be used either as digital logic inputs or inputs for analog to digital conversion. For example: The TLC532/3A can have 11 analog inputs, 5 analog inputs, and 6 digital inputs, or any combination in between.

[‡] Includes access time

[§] Differential input

DATA ACQUISITION AND CONVERSION SELECTION GUIDE

successive-approximation converters

ADDRESS AND DATA I/O FORMAT	SIGNAL INPUTS		RESOLUTION (BITS)	CONVERSION SPEED (μs)[‡]	POWER DISSIPATION (mW TYP)	UNADJUSTED ERROR (MAX) ±LSB	TYPE	PACKAGE	PAGE NO.
	ANALOG DEDICATED	ANALOG[†] DIGITAL							
Serial	1[§]	0	8	84	10	1.0	ADC0831A	P	2-49
						0.5	ADC[illegible]B		
	2[§]					1.0	ADC[illegible]A		
						0.5	ADC0832B		
	4[§]					1.0	A[illegible]A	N	2-57
						0.5	A[illegible]B		
	8					1.0	ADC[illegible]	FN, N	
						0.5	[illegible]		
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				25			TLC541		
	8			40	10		TLC542	FN, N	3-27
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				25			TLC544		
	19			13			TLC545	FN, N	2-173
				25			TLC546		
	1			22			TLC548	D, P	2-181
				25			TLC549		
	11		10	31			TLC1540	FK, FN, J, N	2-199
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				TLC7524	D, FN, N	2-225
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				TLC[illegible]	DW, FN, N	2-233
	Yes			AD7628	FN, N	3-3
Single Multiplying D/A	No	10	150	AD7533C AD7533L		3-65
				TLC7533	D, FN, N	

[†] Analog/digital inputs can be used either as digital logic inputs or inputs for analog to digital conversion. For example: The TLC532/3A can have 11 analog inputs, 5 analog inputs, and 6 digital inputs, or any combination in between.

[‡] Includes access time

[§] Differential input

analog interface for digital signal processors

FUNCTION	TRANSFER CHARACTERISTIC	DYNAMIC RANGE (BITS)	RESOLUTION (BITS)	SAMPLING RATE	ON-BOARD FILTERS	TYPE	PAGE NO.
Discrete Interfaces A/D and D/A	Linear	8	8	1 MHz (A/D)	No	TLC0820/ADC0820	2-189
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						AD7524	2-3
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						AD7528	2-11
		10	10	4 MHz (D/A)		TLC7533/AD7533	3-65
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	8			T [illegible]2		3-55
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	8		375	TL5602		3-23
			125	TLC5602		3-61

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			TLC20/MF10C		
Low Pass, Butterworth	4	±2.5 to ±6	TLC04/MF4A-50	D, P	2-127
			TLC14/MF4A-100		

[†] The TLC32040 and TLC32041 have two differential inputs for the 14-bit A/D and a serial port input for the 14-bit D/A. The A/D conversion accuracy for this device is measured in terms of signal-to-quantization distortion and also in LSB over certain converter ranges. The package types are FN and N. Please refer to the data sheet.

DATA ACQUISITION AND CONVERSION CROSS-REFERENCE GUIDE

Replacements are based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

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Manufacturers are arranged in alphabetical order.

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TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS

INTRODUCTION

These terms, definitions, and letter symbols are in accordance with those currently approved by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

1. GENERAL TERMS

Analog-to-Digital Converter (ADC)

A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of which exclusively represents a fractional part of the total analog input range. (See Figure 1.)

NOTE: This quantization procedure introduces inherent errors of one-half LSB (least significant bit) in the representation since, within this fractional range, only one analog value can be represented free of error by a single digital output code.

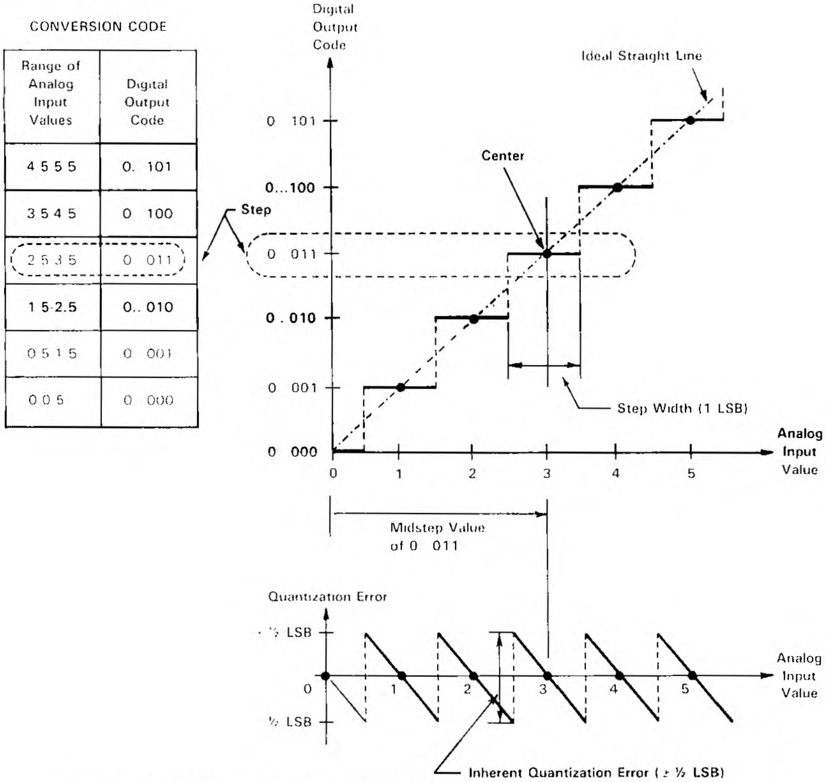


FIGURE 1. ELEMENTS OF TRANSFER DIAGRAM FOR AN IDEAL LINEAR ADC

Analog-to-Digital Processor

An integrated circuit providing the analog part of an ADC; provision of external timing, counting, and arithmetic operations is necessary for implementing a full analog-to-digital converter.

Companding DAC

A DAC whose transfer function complies with a compression or expansion law.

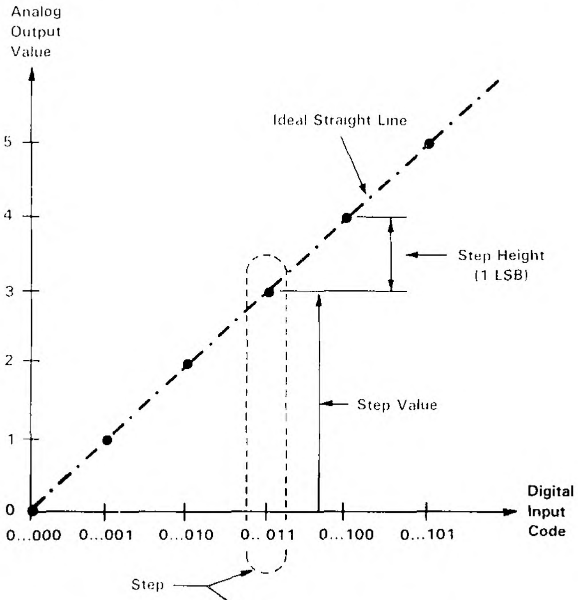
NOTE 1: The corresponding ADC normally consists of such a companding DAC and additional external circuitry.

NOTE 2: The compression or expansion law is usually a logarithmic function, e.g., A-law or μ-law.

Conversion Code (of an ADC or a DAC)

The set of correlations between each of the fractional parts of the total analog input range or each of the digital input codes, respectively, and the corresponding digital output codes or analog output values, respectively. (See Figures 1 and 2.)

NOTE: Examples of output code formats are straight binary, 2's complement, and binary-coded decimal.



CONVERSION CODE

Digital Input Code	0...000	0...001	0 010	0 011	0.. 100	0...101
Analog Output Value	0	1	2	3	4	5

FIGURE 2. ELEMENTS OF TRANSFER DIAGRAM FOR AN IDEAL LINEAR DAC

Digital-to-Analog Converter (DAC)

A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values. (See Figure 2.)

NOTE: Examples of input code formats are straight binary, 2's complement, and binary-coded decimal.

Full Scale (of a unipolar ADC or DAC)

A term used to refer a characteristic to that step within the transfer diagram whose nominal midstep value or nominal step value has the highest absolute value. (See Figure 3a for a linear unipolar ADC.)

NOTE 1: The subscript for the letter symbol of a characteristic at full scale is "FS".

NOTE 2: In place of a letter symbol, the abbreviation "FS" is in common use.

Full Scale, Negative (of a bipolar ADC or DAC) (See Figures 3b and 3c)

A term used to refer a characteristic to the negative end of the transfer diagram, that is, to the step whose nominal midstep value or nominal step value has the most-negative value.

NOTE 1: The subscript for the letter symbol of a characteristic at negative full scale is "FS−" (V_{FS-}, I_{FS-}).

NOTE 2: In place of a letter symbol, the abbreviation "FS−" is in common use.

Full Scale, Positive (of a bipolar ADC or DAC) (See Figure 3b and 3c)

A term used to refer a characteristic to the positive end of the transfer diagram, that is, to the step whose nominal midstep value or nominal step value has the most-positive value.

NOTE 1: The subscript for the letter symbol of a characteristic at positive full scale is "FS+" (V_{FS+}, I_{FS+}).

NOTE 2: In place of a letter symbol, the abbreviation "FS+" is in common use.

Full-Scale Range, Nominal (of a linear ADC or DAC) (V_{FSRnom}, I_{FSRnom}) (See Figure 3)

The total range in analog values that can be coded with uniform accuracy by the total number of steps with this number rounded to the next higher power of 2.

NOTE: In place of the letter symbols, the abbreviation "FSR(nom)" can be used.

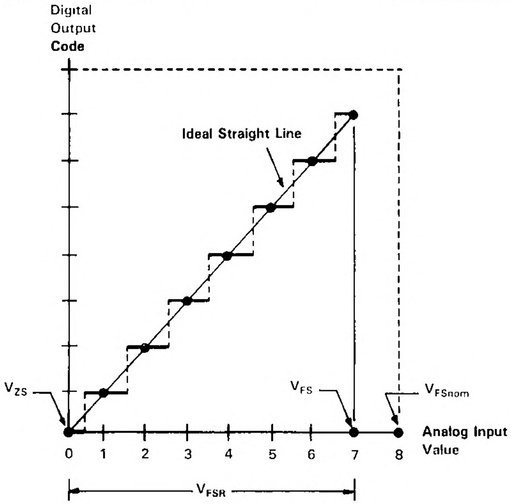
Example: Using a straight binary n-bit code format, it follows:
- for an ADC: FSR(nom) = 2^n × (nominal value of step width)
- for a DAC: FSR(nom) = 2^n × (nominal value of step height)

Full-Scale Value, Nominal (V_{FSnom}, I_{FSnom})

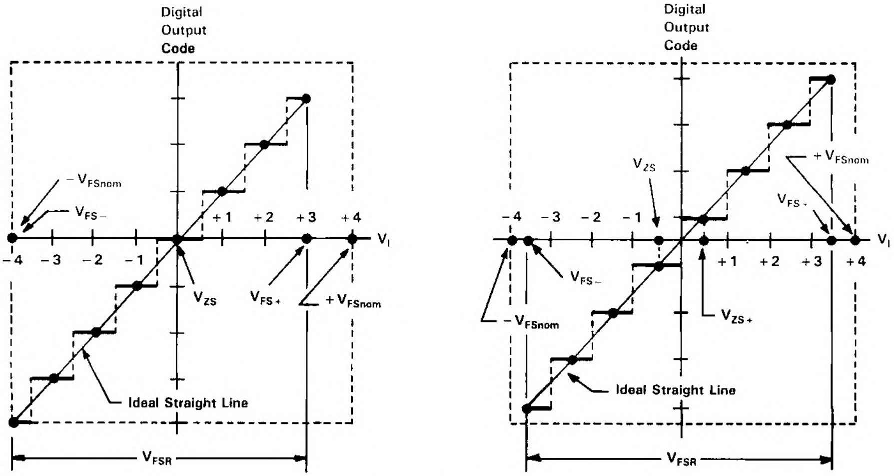
A value derived from the nominal full-scale range:
for a unipolar converter. $V_{FSnom} = V_{FSRnom}$
– for a bipolar converter: $V_{FSnom} = 1/2\ V_{FSRnom}$
(See Figure 3.)

NOTE 1: In a few data sheets, this analog value is used as a reference value for adjustment procedures or as a rounded value for the full-scale range(s).

NOTE 2: In place of letter symbols, the abbreviation "FS(nom)" is in common use.



a. UNIPOLAR ADC



V_I = Analog Input Value

b. BIPOLAR ADC WITH TRUE ZERO

c. BIPOLAR ADC WITH NO TRUE ZERO

FIGURE 3. IDEAL STRAIGHT LINE, FULL-SCALE VALUE AND ZERO-SCALE VALUE (SHOWN FOR IDEAL LINEAR ADCs)

Full-Scale Range, (Practical) (of a linear ADC or DAC) (V_{FSR}, I_{FSR}) (V_{FSRpr}, I_{FSRpr}) (See Figure 3)
The total range of analog values that correspond to the ideal straight line.

NOTE 1: The qualifying adjective "practical" can usually be deleted from this term provided that, in a very few critical cases, the term "nominal full-scale range" is not also shortened in the same way. This permits use of the shorter letter symbols or abbreviations. (See Note 2.)

NOTE 2: In place of the letter symbols, the abbreviations "FSR" and "FSR(pr)" are in common use.

NOTE 3: The (practical) full-scale range has only a nominal value because it is defined by the end points of the ideal straight line.

Example: Using a straight binary n-bit code format, it follows:
– for an ADC: FSR = $(2^n - 1) \times$ (nominal value of step width)
– for a DAC: FSR = $(2^n - 1) \times$ (nominal value of step height)

Gain Point (of an adjustable ADC or DAC)
The point in the transfer diagram corresponding to the midstep value (for an ADC) or the step value (for a DAC) of the step for which gain error is specified (usually full scale), and in reference to which the gain adjustment is performed. (See Figures 4 and 5.)

NOTE: Gain adjustment causes only a change of the slope of the transfer diagram, without changing the offset error.

Ideal Straight Line (of a linear ADC or DAC)
In the transfer diagram, a straight line between the specified points for the most-positive (least-negative) and most-negative (least-positive) nominal midstep values or nominal step values, respectively. (See Figures 1, 2, and 3.)

NOTE: The ideal straight line passes through all the points for nominal midstep values or nominal step values, respectively.

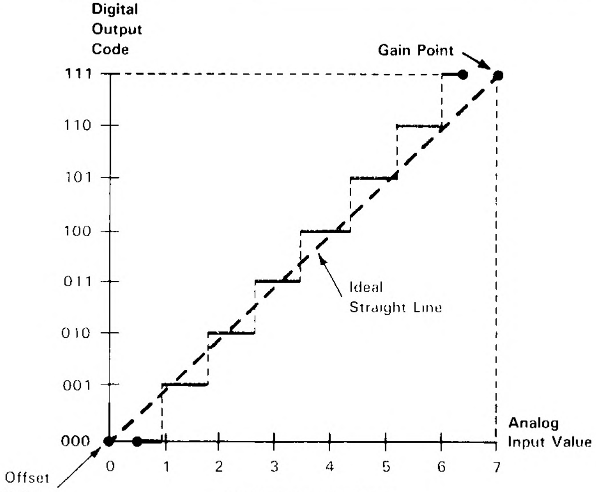
Linear ADC
An ADC having steps ideally of equal width excluding the steps at the two ends of the total range of analog input values.

NOTE: Ideally, the width of each end steps is one half of the width of any other step. (See Figure 1.)

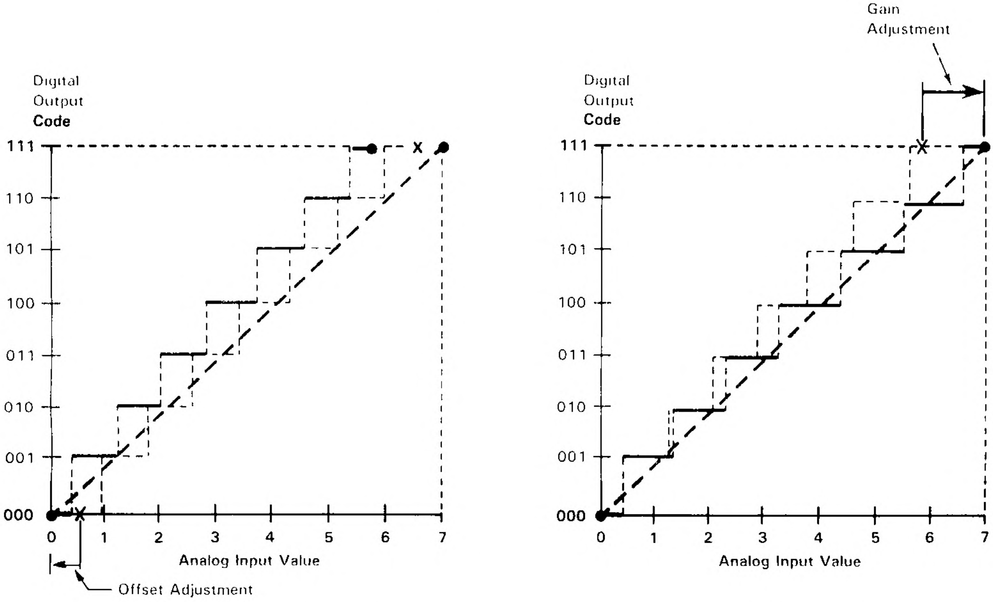
Linear DAC
A DAC having steps ideally of equal height. (See Figure 2.)

LSB, Abbreviation
The abbreviation for "Least Significant Bit", that is, for the bit that has the lowest positional weight in a natural binary numeral.

Example: In the natural binary numeral "1010", the rightmost bit "0" is the LSB.



a BEFORE ADJUSTMENT

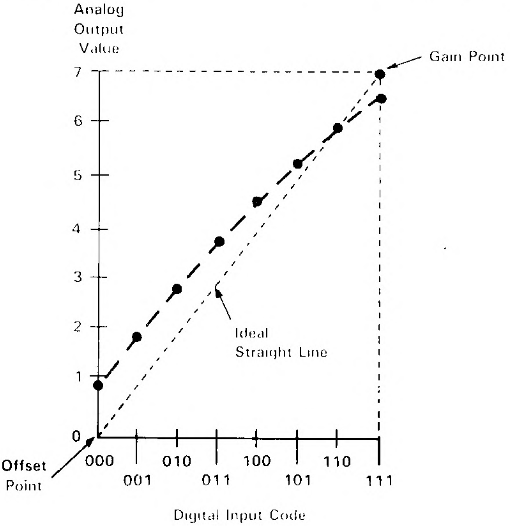


b AFTER OFFSET ADJUSTMENT

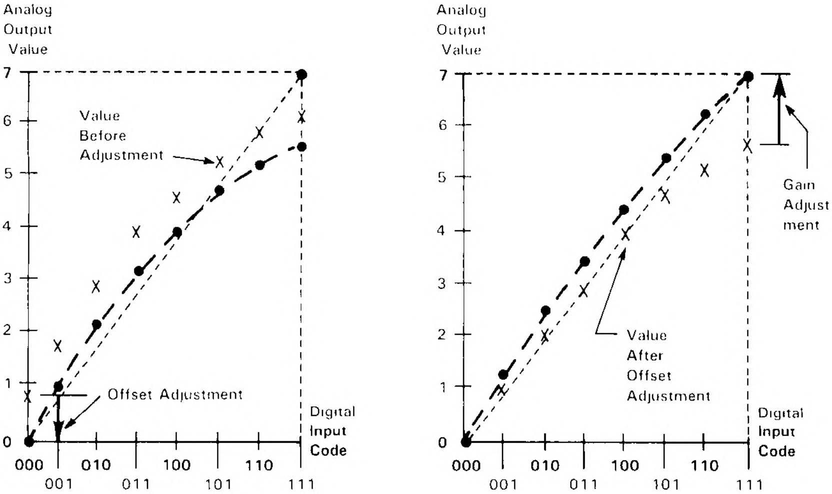
c AFTER OFFSET AND GAIN ADJUSTMENTS

NOTE: In the above examples, the offset point is referred to the step with the digital code 000, and the gain point is referred to the step with the digital code 111.

FIGURE 4. ADJUSTMENT IN OFFSET POINT AND GAIN POINT FOR AN ADC



a BEFORE ADJUSTMENT



b AFTER OFFSET ADJUSTMENT

c. AFTER OFFSET AND GAIN ADJUSTMENTS

NOTE: In the above examples, the offset point is referred to the step with the digital code 000, and the gain point is referred to the step with the digital code 111.

FIGURE 5. ADJUSTMENT IN OFFSET AND GAIN POINT FOR A DAC

LSB, Unit Symbol (for linear converters only)

The unit symbol for the magnitude of the analog resolution of a linear converter, which serves as a reference unit to express the magnitude of other analog quantities of that same converter, especially of analog errors, as multiples or submultiples of the magnitude of the analog resolution.

Example: "1/2 LSB" means an analog quantity equal to 0.5 times the analog resolution.

NOTE: The unit symbol LSB refers to the fact that, for a natural binary code, the analog resolution corresponds to the nominal positional weight attributed to the least significant bit of the binary numeral.

In this case, the identity:

1 LSB = analog resolution

leads, for an n-bit resolution, to:

$$1\ \mathrm{LSB} = \frac{\mathrm{FSR}}{2^n - 1} = \frac{\mathrm{FSR(nom)}}{2^n}$$

Midstep Value (of an ADC)

The analog value for the center of the step excluding the steps at the two ends of the total range of analog input values.

NOTE: For the end steps, the midstep value is defined as the analog value that results when the analog value for the transition to the adjacent step is reduced or enlarged, as appropriate, by half the nominal value of the step width. (See Figure 1.)

Midstep Value, Nominal (of an ADC)

A specified analog value within a step that is ideally represented free of error by the corresponding digital output code. (See Figure 1.)

Missing Code (of an ADC)

An intermediate code that is absent when the changing analog input to an ADC causes a multiple code change in the digital output. (See Figure 6.)

Monotonicity (of an ADC or a DAC)

A property of the transfer function that ensures the consistent increase or decrease of the analog output of a DAC or the digital output of an ADC in response to a consistent increase or decrease of the digital or analog input, respectively. (Figure 7 illustrates nonmonotonic conversion.)

NOTE: An intermediate increment with the value of zero does not invalidate monotonicity.

Multiplying DAC

A DAC having at least two inputs, at least one of which is digital, and whose analog output value is proportional to the product of the inputs.

Nonlinear ADC or DAC

An ADC or a DAC with a specified nonlinear transfer function between the nominal midstep values or nominal step values, respectively, and the corresponding step widths or step heights, respectively.

NOTE: The function may be continuously nonlinear or piece-wise linear.

Offset Point (of an adjustable ADC or DAC)

The point in the transfer diagram corresponding to the midstep value (for an ADC) or the step value (for a DAC) of the step about which the transfer diagram rotates when gain is adjusted. (See Figures 4 and 5.)

NOTE: Offset adjustment must be performed with respect to this point so that it causes only a parallel displacement of the transfer diagram, without changing its slope.

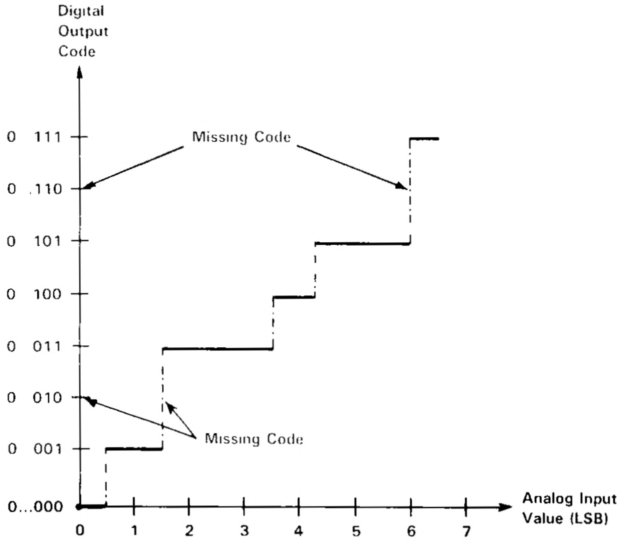


FIGURE 6. MISSING CODE FOR AN ADC

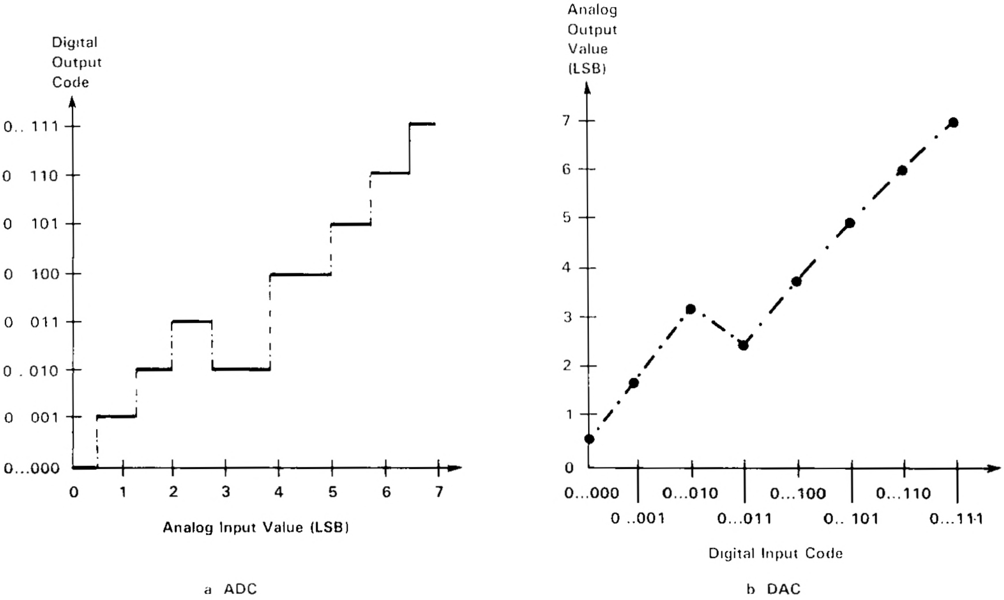


FIGURE 7. NONMONOTONIC CONVERSION OF AN ADC OR DAC

Resolution (general term)

NOTE 1: Resolution as a capability can be expressed in different forms: (see "resolution, analog", "resolution, numerical", and "resolution, relative").

NOTE 2: Resolution is a design parameter and therefore has only a nominal value.

NOTE 3: The terms for these different forms may all be shortened to "resolution" if no ambiguity is likely to occur (for example, when the dimension of the term is also given).

Resolution (of an ADC)
The degree to which nearly equal values of the analog input quantity can be discriminated.

Resolution (of a DAC)
The degree to which nearly equal values of the analog output quantity can be produced.

Resolution, Analog (of a linear or nonlinear ADC or DAC)
For an ADC: The nominal value of the step width.

For a DAC: The nominal value of the step height.

NOTE: For a linear ADC or DAC, the constant magnitude of the analog resolution is often used as the reference unit LSB.

Resolution, Numerical
The number (n) of digits in the chosen numbering system necessary to express the total number of steps.

NOTE 1: The numbering system is normally a binary or a decimal system.

NOTE 2: In the binary-coded-decimal numbering system, the term "1/2 digit" refers to an additional decimal digit with the highest positional value, but limited to the decimal figures "0" or "1" as it is represented by only a single bit. This additional digit serves to double the range of values covered by the other "n" digits.

Resolution, Relative (of a linear ADC or DAC)
The ratio of the analog resolution to the full-scale range (practical or nominal).

NOTE: This ratio is normally expressed as a percentage of the full-scale range [% of FSR, % of FSR(nom)]. For high resolutions (high value of n), it is of little importance whether this ratio refers to the practical or nominal full-scale range.

Step (of an analog-to-digital or digital-to-analog conversion)
In the conversion code: Any of the individual correlations.

In the transfer diagram: Any part of the diagram equating to an individual correlation.

For an ADC, a step represents both a fractional range of analog input values and the corresponding digital output code. (See Figure 1.)

For a DAC, a step represents both a digital input code and the corresponding discrete analog output value. (See Figure 2.)

Step Height (Step Size) (of a DAC)
The absolute value of the difference in step value between two adjacent steps in the transfer diagram. (See Figure 2.)

NOTE: For companding DACs, the term "step size" is in general use.

Step Value (of a DAC)
The value of the analog output representing a digital input code. (See Figure 2.)

Step Value, Nominal (of a DAC)
A specified step value that represents free of error the corresponding digital input code. (See Figure 2.)

Step Width (of an ADC)
The absolute value of the difference between the two ends of the range of analog values corresponding to one step. (See Figure 1.)

Temperature Coefficients of Analog Characteristics (α)

NOTE 1: The letter symbol for the temperature coefficient of an analog characteristic consists of the letter symbol α with a subscript referring to the relevant characteristic.

Example: Temperature coefficient of the gain error: α_{EG}

NOTE 2: Temperature coefficients are usually specified in "parts per million (relative to the full-scale value) per degrees Celsius", that is, in "ppm/°C".

Zero Scale (of an ADC or a DAC with true zero) (See Figures 3a and 3b)
A term used to refer a characteristic to the step whose nominal midstep value or nominal step value equals zero.

NOTE 1: The subscript for the letter symbol of a characteristic at zero scale is "ZS".

NOTE 2: In place of a letter symbol, the abbreviation "ZS" is in common use.

Zero Scale, Negative (of an ADC or a DAC with no true zero) (See Figure 3c)
A term used to refer a characteristic to the negative step closest to analog zero.

NOTE 1: The subscript for the letter symbol of a characteristic at negative zero scale is "ZS−" (V_{ZS-}, I_{ZS-}).

NOTE 2: In place of a letter symbol, the abbreviation "ZS−" is in common use.

Zero Scale, Positive (of an ADC or a DAC with no true zero) (See Figure 3c)
A term used to refer a characteristic to the positive step closest to analog zero.

NOTE 1: The subscript for the letter symbol of a characteristic at positive zero scale is "ZS+" (V_{ZS+}, I_{ZS+})

NOTE 2: In place of a letter symbol, the abbreviation "ZS+" is in common use.

2. STATIC PERFORMANCE

Accuracy (see "Errors", Part 4)

Asymmetry, Full-Scale (of a DAC with a bipolar analog range) (ΔI_{FSS}, ΔV_{FSS})
The difference between the absolute values of the two full-scale analog values.

Compliance, Current (of a DAC) ($I_{O(op)}$)
The permissible range of output current within which the specifications are valid.

Compliance, Voltage (of a DAC) ($V_{O(op)}$)
The permissible range of output voltage within which the specifications are valid.

Errors (see Part 4)

Supply Voltage Sensitivity, (of a DAC) (k_{SVS})
The change in full scale output current (or voltage) caused by a change in supply voltage.

NOTE: This sensitivity is usually expressed as the ratio of the percent change of full-scale current (or voltage) to the percent change of supply voltage.

3. DYNAMIC PERFORMANCE

Conversion Rate (of an externally controlled ADC) (f_c)
The number of conversions per unit time.

NOTE 1: The maximum conversion rate should be specified for full resolution.

NOTE 2: The conversion rate is usually expressed as the number of conversions per second.

NOTE 3: Due to additionally needed settling or recovery times, the maximum specified conversion rate is smaller than the reciprocal of the worst-case conversion time.

Conversion Time (of an ADC) (t_c)
The time elapsed between the command to perform a conversion and the appearance at the converter output of the complete digital representation of the analog input value.

Delay Time, (Digital) (of a linear or a multiplying DAC) (t_d, t_{dd})
The time interval between the instant when the digital input changes and the instant when the analog output passes a specified value that is close to its initial value, ignoring glitches. (See Figure 8.)

NOTE: For a multiplying DAC, the full term and the additional subscript d must be used to distinguish between the digital and the delay time.

Delay Time, Reference (of a multiplying DAC) (t_{dr})
The time interval between the instant when a step change of the reference voltage occurs and the instant when the analog output passes a specified value that is close to its initial value.

Feedthrough Capacitance (C_F)
The value of the capacitance for a specified value of R in an equivalent circuit for the calculation of the feedthrough error.

NOTE: The equivalent circuit consists of a high-pass R-C filter between the reference input and the analog output.

Feedthrough Error (see Part 4)

Glitch (of a DAC)
A short, undesirable transient in the analog output occurring following a code change at the digital input. (See Figure 8.)

Glitch Area (of a DAC)
The time integral of the analog value of the glitch transient.

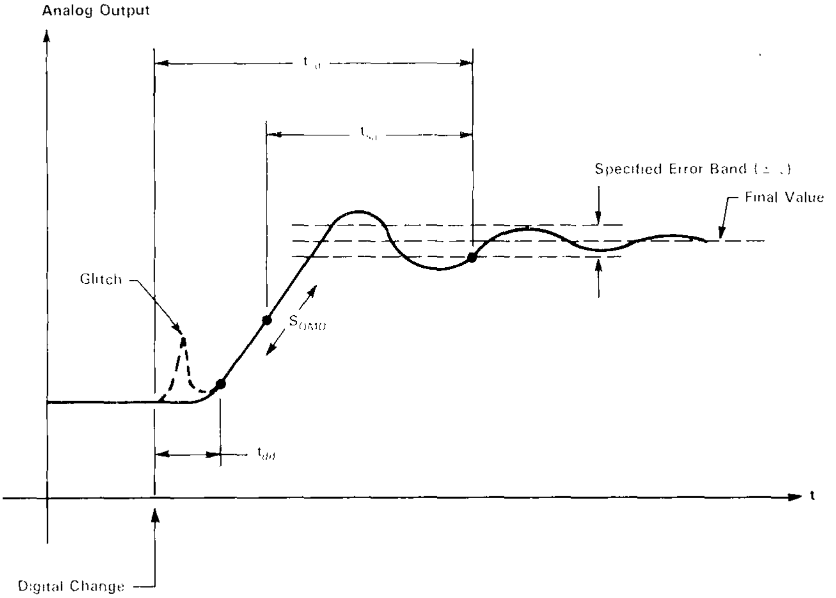
NOTE 1: Usually, the maximum specified glitch area refers to a specified worst-case code change.

NOTE 2: Instead of a letter symbol, the abbreviation "GA" is in use.

Glitch Energy (of a DAC)
The time integral of the electrical power of the glitch transient.

NOTE 1: Usually, the maximum specified glitch energy refers to a specified worst-case code change.

NOTE 2: Instead of a letter symbol, the abbreviation "GE" is in use.



t_{sd} - (Digital) Settling Time
t_{sa} - Analog Settling Time
S_{OMD} - (Digital) Slew Rate
t_{dd} - (Digital) Delay Time

FIGURE 8. OUTPUT CHARACTERISTICS OF A LINEAR OR A MULTIPLYING DAC FOR A STEP CHANGE IN THE DIGITAL INPUT CODE

Pedestal (Error) (E_p) (see Part 4)

Ramp Delay, Steady-State (of a multiplying DAC) ($t_{d(ramp)}$)

The time separation between the actual curve of the analog output and the theoretical curve (with no delay) for a ramp in reference voltage, after the settling time to steady-state ramp has elapsed. (See Figure 9.)

Settling Time, Analog (of a DAC) (t_{sa})

The time interval between the instant when the analog output passes a specified value and the instant when the analog output enters for the last time a specified error band about its final value. (See Figures 8 and 10.)

Settling Time, (Digital) (of a linear or a multiplying DAC) (t_s, t_{sd})

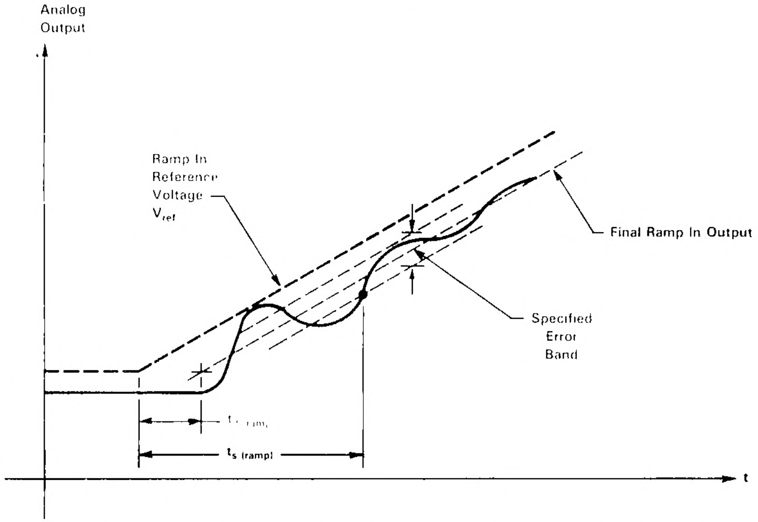
The time interval between the instant when the digital input changes and the instant when the analog output value enters for the last time a specified error band about its final value. (See Figure 8.)

NOTE: For a multiplying DAC, the full term and the additional subscript d must be used to distinguish between the digital and the settling time.

Settling Time, Reference (of a multiplying DAC) (t_{sr})

The time interval between the instant when a step change of the reference voltage occurs and the instant when the analog output enters for the last time a specified error band about its final value. (See Figure 10.)

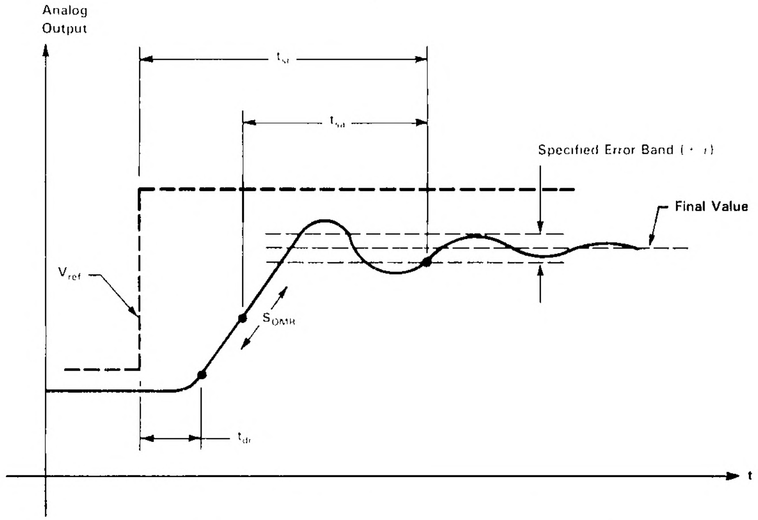
NOTE: Specifications for the reference settling time are usually given for the highest allowed step change in reference voltage.



$t_{s\,(ramp)}$ = Settling Time To Steady-State Ramp Delay

$t_{d\,(ramp)}$ = Steady-State Ramp Delay

FIGURE 9. OUTPUT CHARACTERISTICS FOR A RAMP IN REFERENCE VOLTAGE OF A MULTIPLYING DAC



t_{dr} = Reference Delay Time

t_{sr} = Reference Settling Time

t_{sa} = Analog Settling Time

S_{OMR} = Reference Slew Rate

FIGURE 10. OUTPUT CHARACTERISTICS FOR A STEP CHANGE IN REFERENCE VOLTAGE OF A MULTIPLYING DAC

Settling Time to Steady-State Ramp (of a multiplying DAC) ($t_{s(ramp)}$)
The time interval between the instant a ramp in the reference voltage starts and the instant when the analog output value enters for the last time a specified error band about the final ramp in the output. (See Figure 9.)

Skewing Time, Internal (of a DAC)
The difference in internal delay between the individual output transitions for a given change of digital input.

NOTE: The internal (and external) skew has a major influence on the settling time for critical changes in the digital input, for example, for a 1-LSB change from 011 . . . 111 to 100 . . . 000, and is an important source of commutation noise.

Slew Rate, (Digital) (of a linear or a multiplying DAC) (S_{OM}, S_{OMD})
The maximum rate of change of the analog output value when a change of the digital input code causes a large step change of the analog output value. (See Figure 8.)

NOTE 1: For a multiplying DAC, the full term and the additional subscript D must be used to distinguish between the digital and the slew rate.

NOTE 2: The abbreviations "SR" and "SR(dig)" are also used.

Slew Rate, Reference (of a multiplying DAC) (S_{OMR})
The maximum rate of change of the analog output following a large step change of the reference voltage. (See Figure 10.)

NOTE: The abbreviation "SR(ref)" is also used.

4. ERRORS, ACCURACY

The definitions in this section describe the errors as the difference between the actual value and the nominal value of the analog quantity. As such they may be expressed in conventional units (for example, millivolts) or as multiples or submultiples of 1 LSB. An error can also be expressed as a relative value, for example, in "% of FSR". In this case, it is common practice to use the same term as for the analog value.

Absolute Accuracy Error
Synonym for total error.

Feedthrough Error (of a multiplying DAC) (E_F)
An error in analog output due to variation in the reference voltage that appears as an offset error and is proportional to frequency and amplitude of the reference signal.

NOTE 1: The specification for the feedthrough error is given for the digital input for which the offset error is specified, and for a reference signal of specified frequency and amplitude.

NOTE 2: This error may also be expressed as a peak-to-peak analog value.

Full-Scale Error (of a linear ADC or DAC) (E_{FS})
The difference between the actual midstep value or step value and the nominal midstep value or step value, respectively, at specified full scale.

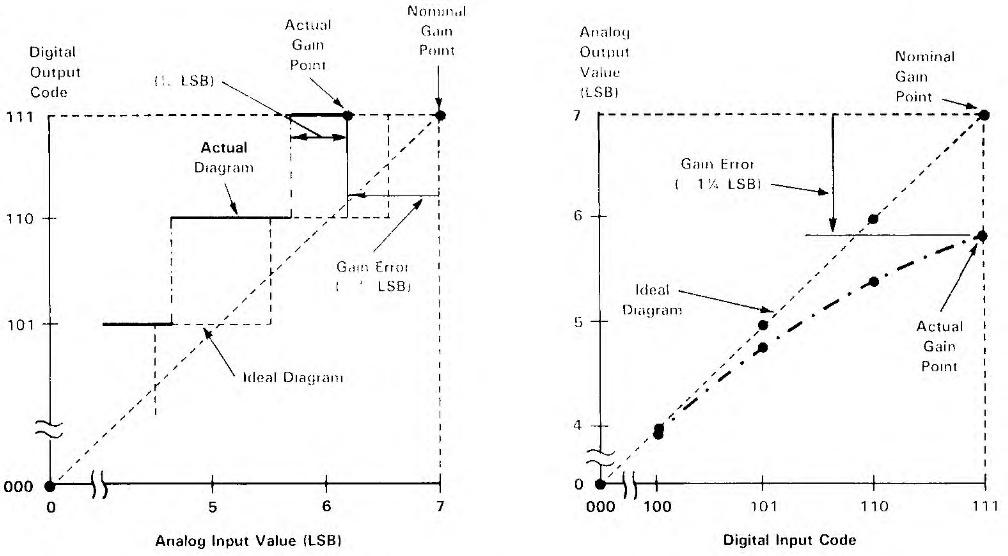
NOTE: Normally, this error specification is applied to converters that have no arrangement for an external adjustment of offset error and gain error.

Gain Error (of a linear ADC or DAC) (E_G)

For an ADC: The difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. (See Figure 11a.)

For a DAC: The difference between the actual step value and the nominal step value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. (See Figure 11b.)

NOTE: See Notes 1 and 2 under "Offset Error".



a. ADC

b. DAC

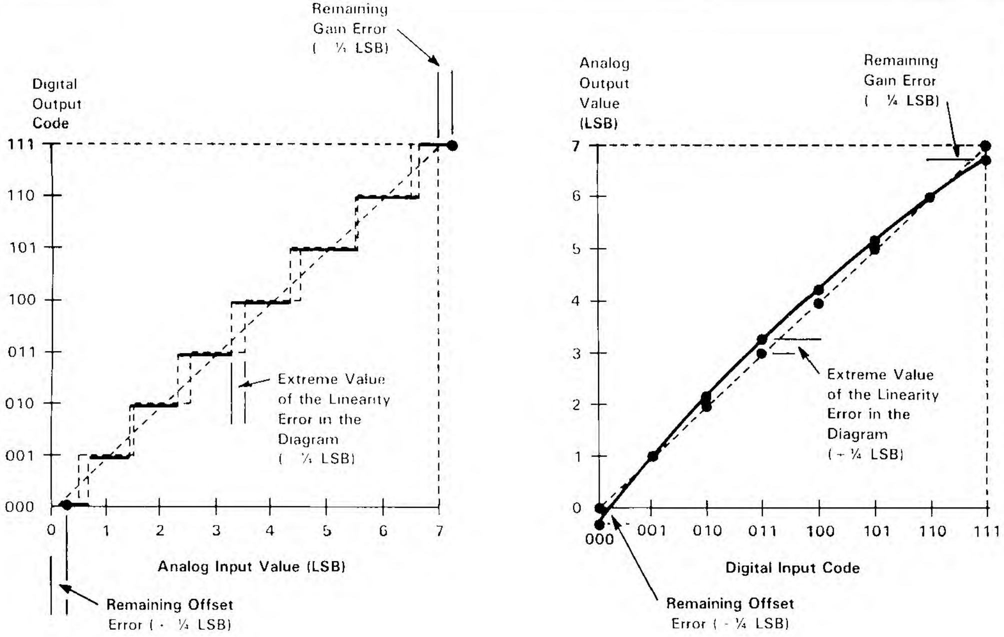
FIGURE 11. GAIN ERROR OF A LINEAR 3-BIT NATURAL BINARY CODE CONVERTER (SPECIFIED AT STEP 111), AFTER CORRECTION OF THE OFFSET ERROR

Instability, Long-Term (Accuracy) ($\Delta E_{(\Delta t)}$, $\Delta E_{(t)}$)
The additional error caused by the aging of the components and specified for a longer period in time.

Linearity Error, Best-Straight-Line (of a linear and adjustable ADC) ($E_{L(adj)}$)
The difference between the actual analog value at the transition between any two adjacent steps and its *ideal* value after offset error and gain error have been adjusted to minimize the magnitude of the extreme values of this difference. (See Figure 12a.)

NOTE 1: The inherent quantization error is not included in the best-straight-line linearity error of an ADC. The ideal value for the transition corresponds to the nominal midstep value ±1/2 LSB.

NOTE 2: For a uniformly curved transfer diagram, the extreme values will be very close to half of the magnitude of the end-point linearity error. (See Figure 12a.)



a ADC

b DAC

FIGURE 12. BEST-STRAIGHT-LINE LINEARITY ERROR OF A LINEAR 3-BIT NATURAL BINARY-CODED CONVERTER (VALUES BETWEEN ± ¼ LSB)

Linearity Error, Best-Straight-Line (of a linear and adjustable DAC) ($E_{L(adj)}$)

The difference between the actual step value and the nominal step value after offset error and gain error have been adjusted to minimize the magnitude of the extreme values of this difference. (See Figure 12b.)

NOTE: For a uniformly curved transfer diagram, the extreme values will be very close to half of the magnitude of the end-point linearity error. (See Figure 12b.)

Linearity Error, Differential (of a linear ADC or DAC) (E_D)

The difference between the actual step width or step height and the ideal value (1 LSB). (See Figure 13.)

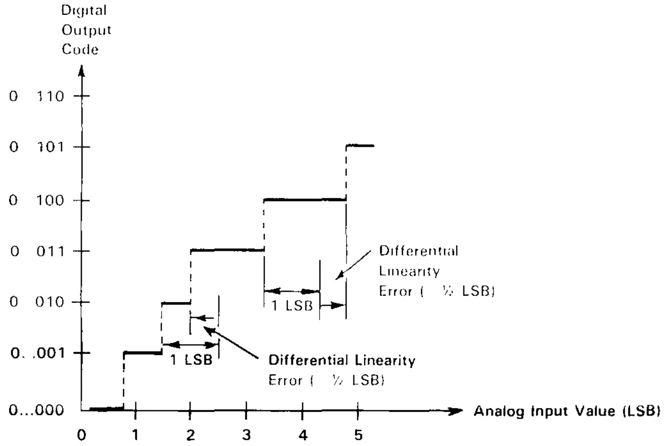
NOTE: A differential linearity error greater than 1 LSB can lead to missing codes in an ADC or to nonmonotonicity of an ADC or a DAC. (See Figures 6 and 7.)

Linearity Error, End-Point (of a linear and adjustable ADC) (E_L)

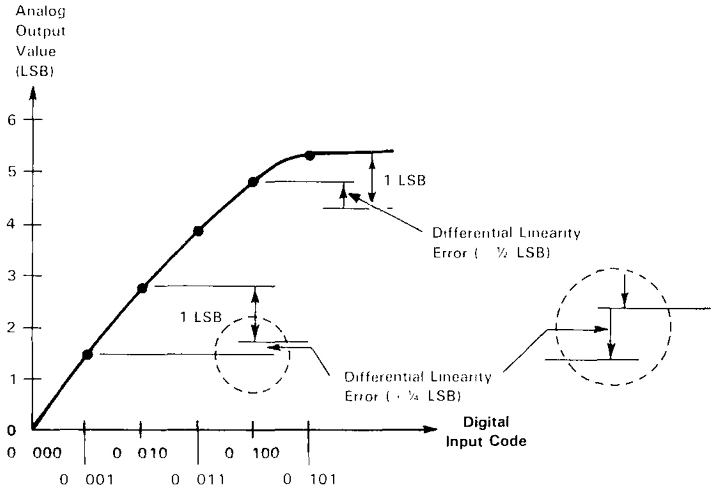
The difference between the actual analog value at the transition between any two adjacent steps and its ideal value after offset error and gain error have been adjusted to zero. (See Figure 14a.)

NOTE 1: The short term "linearity error" is in common use and is sufficient if no ambiguity with the "best-straight-line linearity error" is likely to occur.

NOTE 2: The inherent quantization error is not included in the linearity error of an ADC. The ideal value for the transition corresponds to the nominal midstep value ±1/2 LSB.



a ADC



b DAC

FIGURE 13. DIFFERENTIAL LINEARITY ERROR OF A LINEAR ADC OR DAC

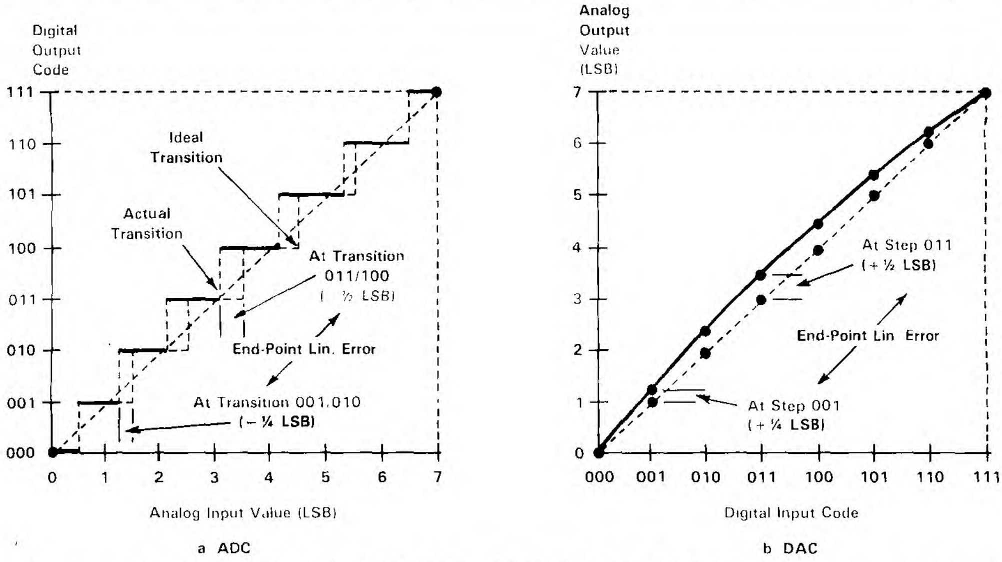


FIGURE 14. END-POINT LINEARITY ERROR OF A LINEAR 3-BIT NATURAL BINARY-CODED ADC OR DAC (OFFSET ERROR AND GAIN ERROR ARE ADJUSTED TO THE VALUE ZERO)

Linearity Error, End-point (of a linear and adjustable DAC) (E_L)

The difference between the actual step value and the nominal step value after offset error and gain error have been adjusted to zero. (See Figure 14b.)

NOTE: The short term "linearity error" is in common use and is sufficient if no ambiguity with the "best-straight-line linearity error" is likely to occur.

Offset Error (of a linear ADC or DAC) (E_O)

For an ADC: The difference between the actual midstep value and the nominal midstep value at the offset point. (See Figure 15a.)

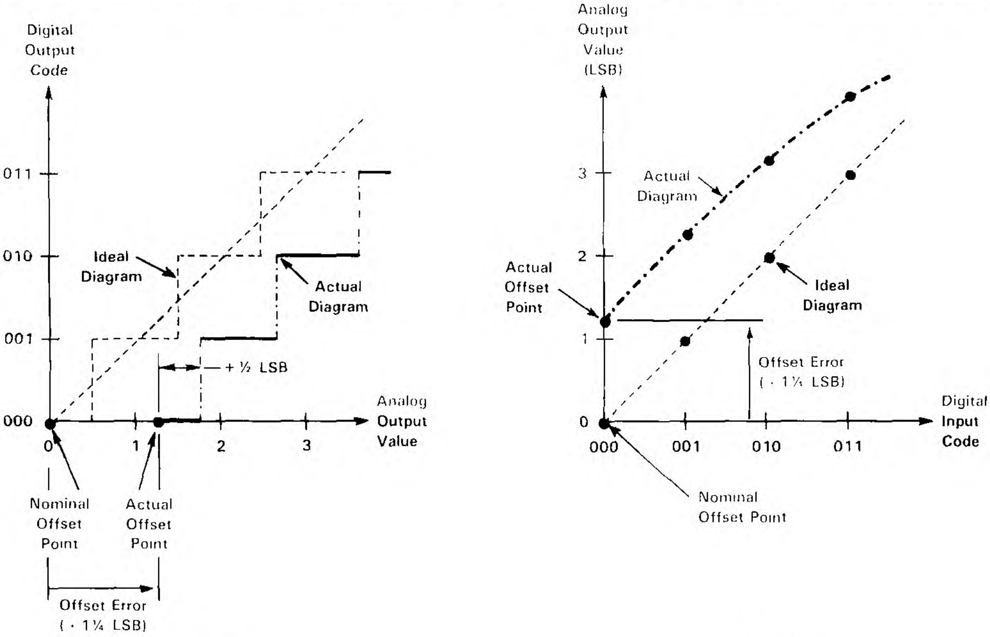
For a DAC: The difference between the actual step value and the nominal step value at the offset point. (See Figure 15b.)

NOTE 1: Usually, the specified steps for the specification of offset error and gain error are the steps at the ends of the practical full-scale range. For an ADC, the midstep value of these steps is defined as the value for a point 1/2 LSB apart from the adjacent transition. (See Figures 11 and 15.)

NOTE 2: The terms "offset error" and "gain error" should be used only for errors that can be adjusted to zero. Otherwise, the terms "zero-scale error" and "full-scale error" should be used.

Pedestal (Error) (E_P)

A dynamic offset error produced in the commutation process.



a ADC b DAC

FIGURE 15. OFFSET ERROR OF A LINEAR 3-BIT NATURAL BINARY CODE CONVERTER (SPECIFIED AT STEP 000)

Quantization Error, Inherent (of an ideal ADC)

Within a step, the maximum (positive or negative) possible deviation of the actual analog input value from the nominal midstep value.

NOTE 1: This error follows necessarily from the quantization procedure. For a linear ADC, its value equals ±1/2 LSB. (See Figure 1.)

NOTE 2: The term "resolution error" for the "inherent quantization error" is deprecated, because "resolution" as a design parameter has only a nominal value.

Rollover Error (of an ADC with decimal output and auto-polarity) (E_{RO})

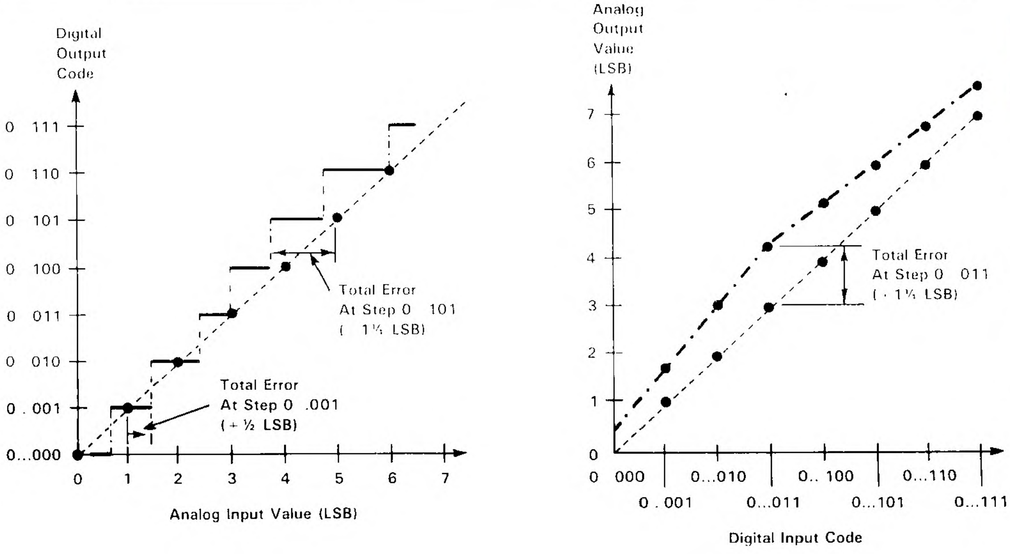
The difference in output readings with the analog input switched between positive and negative values of the same magnitude (close to full scale).

Total Error (of a linear ADC) (E_T)

The maximum difference (positive or negative) between an analog value and the nominal midstep value within any step. (See Figure 16a.)

NOTE 1: If this error is expressed as a relative value, the term "relative accuracy error" should be used instead of "absolute accuracy error".

NOTE 2: This error includes contributions from offset error, gain error, linearity error, and the inherent quantization error.



a ADC

b DAC

FIGURE 16. ABSOLUTE ACCURACY ERROR, TOTAL ERROR OF A LINEAR ADC OR DAC

Total Error (of a linear DAC) (E_T)

The difference (positive or negative) between the actual step value and the nominal step value for any step. (See Figure 16b.)

NOTE 1: If this error is expressed as a relative value, the term "relative accuracy error" should be used instead of "absolute accuracy error".

NOTE 2: This error includes contributions from offset error, gain error, and linearity error.

Zero-Scale Error (of a linear ADC or DAC) (E_{ZS})

The difference between the actual midstep value or step value and the nominal midstep value or step value, respectively, at specified zero scale

NOTE: Normally, this error specification is applied to converters that have no arrangement for an external adjustment of offset error and gain error.