

General Information

1

Data Sheets

2

Product Previews

3

Mechanical Data

4



Contents

	Page
Alphanumeric Index	1-3
Selection Guide	1-7
Cross-Reference Guide	1-11
Glossary	1-17

AD7524	2-3	LM339	VOL 1	MF10A	2-139
AD7528	2-11	LM348	VOL 1	MF10C	2-139
AD7533	3-65	LM358	VOL 1	NE555	VOL 1
AD7628	3-3	LM385-2.5	VOL 3	NE556	VOL 1
ADC0803	2-23	LM393	VOL 1	NE592	VOL 1
ADC0804	2-29	LM2900	VOL 1	NE5532	VOL 1
ADC0805	2-23	LM2901	VOL 1	NE5534	VOL 1
ADC0808	2-35	LM2902	VOL 1	OP07	VOL 1
ADC0808M	2-41	LM2903	VOL 1	OP07C	VOL 1
ADC0809	2-35	LM2904	VOL 1	OP07D	VOL 1
ADC0820B	2-189	LM2907	VOL 1	OP07E	VOL 1
ADC0820C	2-189	LM2917	VOL 1	OP27A	VOL 1
ADC0831A	2-49	LM2930-5	VOL 3	OP27C	VOL 1
ADC0831B	2-49	LM2930-8	VOL 3	OP27E	VOL 1
ADC0832A	2-49	LM2931-5AQ	VOL 3	OP27G	VOL 1
ADC0832B	2-49	LM3302	VOL 1	OP37A	VOL 1
ADC0834A	2-57	LM3900	VOL 1	OP37C	VOL 1
ADC0834B	2-57	LP111	VOL 1	OP37E	VOL 1
ADC0838A	2-57	LP211	VOL 1	OP37G	VOL 1
ADC0838B	2-57	LP239	VOL 1	RC4136	VOL 1
ICL7135	2-69	LP311	VOL 1	RC4558	VOL 1
LF198	VOL 1	LP339	VOL 1	RC4559	VOL 1
LF347	VOL 1	LP2901	VOL 1	RM4136	VOL 1
LF351	VOL 1	LT1001	VOL 1	RM4558	VOL 1
LF353	VOL 1	LT1004	VOL 3	RV4136	VOL 1
LF398	VOL 1	LT1007	VOL 1	RV4558	VOL 1
LF411C	VOL 1	LT1008	VOL 1	SA555	VOL 1
LF412C	VOL 1	LT1009	VOL 3	SA556	VOL 1
LM101A	VOL 1	LT1011	VOL 1	SE555	VOL 1
LM107	VOL 1	LT1012	VOL 1	SE555C	VOL 1
LM108	VOL 1	LT1013	VOL 1	SE556	VOL 1
LM111	VOL 1	LT1016	VOL 1	SE556C	VOL 1
LM124	VOL 1	LT1028	VOL 1	SE592	VOL 1
LM139	VOL 1	LT1036M	VOL 3	SE5534	VOL 1
LM148	VOL 1	LT1036C	VOL 3	SG2524	VOL 3
LM158	VOL 1	LT1037	VOL 1	SG3524	VOL 3
LM185-2.5	VOL 3	LT1054	VOL 3	SN28827	VOL 1
LM193	VOL 1	LT1070	VOL 3	SN28828	VOL 1
LM201A	VOL 1	LT1084	VOL 3	SN76494/A	VOL 1
LM207	VOL 1	LTC1044	VOL 3	SN76496/A	VOL 1
LM211	VOL 1	LTC1052	VOL 1	TL0101	VOL 1
LM217	VOL 3	LTC7652	VOL 1	TL010C	VOL 1
LM218	VOL 1	MC1445	VOL 1	TL011	VOL 1
LM224	VOL 1	MC1458	VOL 1	TL012	VOL 1
LM237	VOL 3	MC1558	VOL 1	TL014A	VOL 1
LM239	VOL 1	MC3303	VOL 1	TL021	VOL 1
LM248	VOL 1	MC3403	VOL 1	TL022M	VOL 1
LM258	VOL 1	MC3423	VOL 3	TL022C	VOL 1
LM293	VOL 1	MC3470	VOL 1	TL026C	VOL 1
LM301A	VOL 1	MC34060	VOL 3	TL027C	VOL 1
LM307	VOL 1	MC79L05	VOL 3	TL031	VOL 1
LM308	VOL 1	MC79L05A	VOL 3	TL032	VOL 1
LM311	VOL 1	MC79L12	VOL 3	TL034	VOL 1
LM317	VOL 3	MC79L12A	VOL 3	TL040C	VOL 1
LM318	VOL 1	MC79L15	VOL 3	TL041C	VOL 1
LM324	VOL 1	MC79L15A	VOL 3	TL044M	VOL 1
LM330-5	VOL 3	MF4A-50	2-127	TL044C	VOL 1
LM337	VOL 3	MF4A-100	2-127	TL051	VOL 1

ALPHANUMERIC INDEX

General Information

TL052	VOL 1	TL499A	VOL 3	TL7712A	VOL 3
TL054	VOL 1	TL500	2-93	TL7715A	VOL 3
TL060	VOL 1	TL501	2-93	TL7770-5	VOL 3
TL061	VOL 1	TL502	2-93	TL7770-12	VOL 3
TL062	VOL 1	TL503	2-93	TL7770-15	VOL 3
TL064	VOL 1	TL505	2-107	TL7780-5	VOL 3
TL066M	VOL 1	TL507	2-115	TL7780-12	VOL 3
TL066I	VOL 1	TL514M	VOL 1	TL7780-15	VOL 3
TL066C	VOL 1	TL592	VOL 1	TLC04	2-127
TL070	VOL 1	TL592B	VOL 1	TLC0820A	2-189
TL071	VOL 1	TL594I	VOL 3	TLC0820B	2-189
TL072	VOL 1	TL594C	VOL 3	TLC10	2-139
TL074	VOL 1	TL595C	VOL 3	TLC14	2-127
TL075	VOL 1	TL598	VOL 3	TLC20	2-139
TL080	VOL 1	TL601	2-121	TLC251C	VOL 1
TL081	VOL 1	TL604	2-121	TLC252C	VOL 1
TL082	VOL 1	TL607	2-121	TLC254C	VOL 1
TL083	VOL 1	TL610	2-121	TLC25L2C	VOL 1
TL084	VOL 1	TL712	VOL 1	TLC25L4C	VOL 1
TL085	VOL 1	TL714C	VOL 1	TLC25M2C	VOL 1
TL087	VOL 1	TL721	VOL 1	TLC25M4C	VOL 1
TL088	VOL 1	TL750L05	VOL 3	TLC271	VOL 1
TL0808	2-81	TL750L08	VOL 3	TLC272	VOL 1
TL0809	2-81	TL750L10	VOL 3	TLC274	VOL 1
TL136C	VOL 1	TL750L12	VOL 3	TLC277	VOL 1
TL170C	VOL 1	TL750M05	VOL 3	TLC279	VOL 1
TL172C	VOL 1	TL750M08	VOL 3	TLC27L2	VOL 1
TL173I	VOL 1	TL750M10	VOL 3	TLC27L4	VOL 1
TL173C	VOL 1	TL750M12	VOL 3	TLC27L7	VOL 1
TL182	2-87	TL751L05	VOL 3	TLC27L9	VOL 1
TL185	2-87	TL751L08	VOL 3	TLC27M2	VOL 1
TL188	2-87	TL751L10	VOL 3	TLC27M4	VOL 1
TL191	2-87	TL751L12	VOL 3	TLC27M7	VOL 1
TL287	VOL 1	TL751M05	VOL 3	TLC27M9	VOL 1
TL288	VOL 1	TL751M08	VOL 3	TLC339M	VOL 1
TL317M	VOL 3	TL751M10	VOL 3	TLC339I	VOL 1
TL317C	VOL 3	TL751M12	VOL 3	TLC339C	VOL 1
TL321I	VOL 1	TL780-05	VOL 3	TLC352M	VOL 1
TL321C	VOL 1	TL780-12	VOL 3	TLC352I	VOL 1
TL322I	VOL 1	TL780-15	VOL 3	TLC352C	VOL 1
TL322C	VOL 1	TL783C	VOL 3	TLC354M	VOL 1
TL331I	VOL 1	TL851	VOL 1	TLC354I	VOL 1
TL331C	VOL 1	TL852	VOL 1	TLC354C	VOL 1
TL430I	VOL 3	TL853	VOL 1	TLC372M	VOL 1
TL430C	VOL 3	TL1451AC	VOL 3	TLC372I	VOL 1
TL431AI	VOL 3	TL3013C	VOL 1	TLC372C	VOL 1
TL431AC	VOL 3	TL3019C	VOL 1	TLC374M	VOL 1
TL431M	VOL 3	TL3020C	VOL 1	TLC374I	VOL 1
TL431I	VOL 3	TL3101I	VOL 1	TLC374C	VOL 1
TL431C	VOL 3	TL3101C	VOL 1	TLC393M	VOL 1
TL441AM	VOL 1	TL3103I	VOL 1	TLC393I	VOL 1
TL493	VOL 3	TL3103C	VOL 1	TLC393C	VOL 1
TL494	VOL 3	TL5501	3-13	TLC532A	2-155
TL495	VOL 3	TL5601	3-19	TLC533A	2-155
TL496C	VOL 3	TL5602	3-23	TLC540	2-165
TL497AM	VOL 3	TL7702A	VOL 3	TLC541	2-165
TL497AI	VOL 3	TL7705A	VOL 3	TLC542	3-27
TL497AC	VOL 3	TL7709A	VOL 3	TLC543	3-35

TLC544	3-35	uA748C	VOL 1	uA79M24C	VOL 3
TLC545	2-173	uA2240C	VOL 1	UC1846	VOL 3
TLC546	2-173	uA7805	VOL 3	UC1847	VOL 3
TLC548	2-181	uA7806	VOL 3	UC2842	VOL 3
TLC549	2-181	uA7808	VOL 3	UC2843	VOL 3
TLC551C	VOL 1	uA7810	VOL 3	UC2844	VOL 3
TLC552C	VOL 1	uA7812	VOL 3	UC2845	VOL 3
TLC555M	VOL 1	uA7815	VOL 3	UC2846	VOL 3
TLC555I	VOL 1	uA7818	VOL 3	UC2847	VOL 3
TLC555C	VOL 1	uA7824	VOL 3	UC3842	VOL 3
TLC556M	VOL 1	uA7885	VOL 3	UC3843	VOL 3
TLC556I	VOL 1	uA78L02AC	VOL 3	UC3844	VOL 3
TLC556C	VOL 1	uA78L02C	VOL 3	UC3845	VOL 3
TLC1078	VOL 1	uA78L05AC	VOL 3	UC3846	VOL 3
TLC1079	VOL 1	uA78L05C	VOL 3	UC3847	VOL 3
TLC1225A	3-43	uA78L06AC	VOL 3		
TLC1225B	3-43	uA78L06C	VOL 3		
TLC1540	2-199	uA78L08AC	VOL 3		
TLC1541	2-199	uA78L08C	VOL 3		
TLC2201	VOL 1	uA78L09AC	VOL 3		
TLC2652	VOL 1	uA78L09C	VOL 3		
TLC2654	VOL 1	uA78L10AC	VOL 3		
TLC3702M	VOL 1	uA78L10C	VOL 3		
TLC3702I	VOL 1	uA78L12AC	VOL 3		
TLC3702C	VOL 1	uA78L12C	VOL 3		
TLC3704M	VOL 1	uA78L15AC	VOL 3		
TLC3704I	VOL 1	uA78L15C	VOL 3		
TLC3704C	VOL 1	uA78M05M	VOL 3		
TLC4016	2-209	uA78M05C	VOL 3		
TLC4066	2-217	uA78M06	VOL 3		
TLC5502	3-55	uA78M08	VOL 3		
TLC5602	3-61	uA78M09	VOL 3		
TLC7135	2-69	uA78M10	VOL 3		
TLC7524	2-225	uA78M112M	VOL 3		
TLC7528	2-233	uA78M112C	VOL 3		
TLC7533	3-65	uA78M15M	VOL 3		
TLC7701I	VOL 3	uA78M15C	VOL 3		
TLC7705I	VOL 3	uA78M20	VOL 3		
TLC7721I	VOL 3	uA78M24	VOL 3		
TLC7725I	VOL 3	uA7905	VOL 3		
TLC32040	2-247	uA7906	VOL 3		
TLC32041	2-247	uA7908	VOL 3		
TLC32042	2-247	uA7912	VOL 3		
TLC32044	2-277	uA7915	VOL 3		
TLC32045	2-311	uA7918	VOL 3		
TLE2021	VOL 1	uA7924	VOL 3		
TLE2022	VOL 1	uA7952	VOL 3		
TLE2024	VOL 1	uA79M05M	VOL 3		
uA709M	VOL 1	uA79M05C	VOL 3		
uA709C	VOL 1	uA79M06M	VOL 3		
uA723M	VOL 3	uA79M106C	VOL 3		
uA723C	VOL 3	uA79M108M	VOL 3		
uA733M	VOL 1	uA79M108C	VOL 3		
uA733C	VOL 1	uA79M1012M	VOL 3		
uA741M	VOL 1	uA79M1012C	VOL 3		
uA741C	VOL 1	uA79M1015M	VOL 3		
uA747M	VOL 1	uA79M1015C	VOL 3		
uA747C	VOL 1	uA79M20C	VOL 3		

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199	199	199	199
200	200	200	200



single-slope and dual-slope A/D converters

CONVERSION FUNCTION	RESOLUTION	SPEED (ms)	TYPE	PACKAGE	PAGE NO.
Dual Slope A/D with BCD Output	4 1/2 Digits	34	TLC7135 ICL7135	FN, N	2-69
Dual-Slope Analog Processors	4 1/2 Digits	80	TL500	J, DW	2-93
	3 1/2 Digits		TL501		
Digital Processors with Seven-Segment Outputs	4 1/2 Digits		TL502	N	
Digital Processors with BCD Outputs	4 1/2 Digits	TL503			
Dual-Slope Analog	10 Bits	50	T		2-107
Pulse-Width Modulator for Single-Slope Converter	7 Bits	1	T	P	2-115

successive-approximation and semi-flash converters

ADDRESS AND DATA I/O FORMAT	SIGNAL INPUTS		RESOLUTION (BITS)	CONVERSION SPEED (μ s) [‡]	POWER DISSIPATION (mW TYP)	UNADJUSTED ERROR (MAX) \pm LSB	TYPE	PACKAGE	PAGE NO.
	ANALOG DEDICATED	ANALOG [†] DIGITAL							
Parallel	1 [§]		8	100	10	0.5	ADC0803	N	2-23
						1.0	ADC0804		2-29
							ADC0805		2-23
	8	0				0.75	ADC0808	FN, N	2-35
						0.75	ADC0808M	FK, JD	2-41
						1.25	ADC0809		2-35
	1 [§]		1	35	0.5	0.75	TL0808	FN, N	2-81
						1.25	TL0809		
						0.5	ADC0820B	DW, FN, N	
						1.0	ADC0820C		
	1.0	TLC0820A							
	5	6				0.5	TLC0820B	FN, N	2-155
							TLC532A		
	1	0	13	10	45	1.0	TLC1225A	J, N	3-43
0.5						TLC1225B			

[†]Analog/digital inputs can be used either as digital logic inputs or inputs for analog to digital conversion. For example: The TLC532/3A can have 11 analog inputs, 5 analog inputs, and 6 digital inputs, or any combination in between.

[‡]Includes access time

[§]Differential input

DATA ACQUISITION AND CONVERSION SELECTION GUIDE

successive-approximation converters

ADDRESS AND DATA I/O FORMAT	SIGNAL INPUTS		RESOLUTION (BITS)	CONVERSION SPEED (μ s) [†]	POWER DISSIPATION (mW TYP)	UNADJUSTED ERROR (MAX) \pm LSB	TYPE	PACKAGE	PAGE NO.	
	ANALOG DEDICATED	ANALOG [‡] DIGITAL								
Serial	1 [§] 2 [§] 4 [§] 8	0	8	64	10	1.0	ADC0831A	P	2-49	
							ADC B			
							ADC A			
							ADC0832B			
							A 'A			
							A 'B			
	11 8 5 19 1 11	0	8	31	6	10	0.5	TLC540	DW, FN, N	2-165
								TLC541		
								TLC542		
								TLC543		
								TLC544		
								TLC545		
								TLC546		
								TLC548		
								TLC549		
								TLC1540		
								TLC1541		
								1.0		

D/A converters (5 V to 15 V)

FUNCTION	TTL COMPATIBILITY AT 15 V	RESOLUTION (BITS)	SETTLING TIME (ns)	TYPE	PACKAGE	PAGE NO.
Single Multiplying D/A	No	8	100	AD7524A	N	2-3
				AD7524J	FN, N	
				TLC7524	D, FN, N	2-225
Dual Multiplying D/A	Yes	8	100	AD7528B	FN, N	2-11
				AD7528	FN, N	2-233
				TLC7528	DW, FN, N	
Single Multiplying D/A	No	10	150	AD7533C	FN, N	3-65
				AD7533L	FN, N	
				TLC7533	D, FN, N	

[†] Analog/digital inputs can be used either as digital logic inputs or inputs for analog to digital conversion. For example: The TLC532/3A can have 11 analog inputs, 5 analog inputs, and 6 digital inputs, or any combination in between.

[‡] Includes access time

[§] Differential input

DATA ACQUISITION AND CONVERSION SELECTION GUIDE

1

General Information

analog interface for digital signal processors

FUNCTION	TRANSFER CHARACTERISTIC	DYNAMIC RANGE (BITS)	RESOLUTION (BITS)	SAMPLING RATE	ON-BOARD FILTERS	TYPE	PAGE NO.
Discrete Interfaces A/D and D/A	Linear	8	8	1 MHz (A/D)	No	TLC0820/ADC0820	2-189
				5 MHz (D/A)		TLC7524	2-225
				5 MHz (Dual D/A)		AD7524	2-3
				4 MHz (D/A)		TLC7528	2-233
		10	10			AD7528	2-11
						TLC7533/AD7533	3-65
High Performance Combo	Linear	14	14	19.2 kHz (Programmable)	Yes (Programmable)	TLC32040† TLC30041† TLC32042†	2-247
Voiceband AIC	Linear	14	14	20 kHz	Yes	TLC32044 TLC32045	2-277 2-311

video converters

CONVERSION FUNCTION	RESOLUTION (BITS)	CONVERSION FREQUENCY (MHz)	POWER DISSIPATION (mW)	TYPE	PACKAGE	PAGE NO.
Video A/D Converter	6	20	300	T	N	3-13
	8			T I2		3-55
Video D/A Converter	6		325	TL5601		3-19
	8		375	TL5602		3-23
		125	TLC5602	3-61		

analog switches and multiplexers

FUNCTION	POWER SUPPLIES (V)	VOLTAGE RANGE (V)	TYPICAL IMPEDANCE (OHMS)	TYPE	PACKAGE	PAGE NO.
Twin SPDT	± 15	± 10	100	TL182	N	2-87
Dual SPST			150	TL185		
Twin Dual SPST			100	TL188		
SPDT			150	TL191		
Dual SPDT	± 25	- 17 to + 25	100	TL601	JG, P	2-121
Dual SPDT			100	TL604		
SPST with Enable			100	TL607		
SPST with Logic Inputs			80	TL610		
Quad Bilateral Analog Switch	12	2 to 12	50	TLC4016	D, J, N	2-209
			30	TLC4066		2-217

switched-capacitor filter ICs

FUNCTION	FILTER ORDER	POWER SUPPLIES (V)	TYPE	PACKAGE	PAGE NO.
Dual Filter, General Purpose	2	± 4 to ± 5	TLC10/MF10A	FN, N	2-139
			TLC20/MF10C		
Low Pass, Butterworth	4	± 2.5 to ± 6	TLC04/MF4A-50	D, P	2-127
			TLC14/MF4A-100		

† The TLC32040 and TLC32041 have two differential inputs for the 14-bit A/D and a serial port input for the 14-bit D/A. The A/D conversion accuracy for this device is measured in terms of signal-to-quantization distortion and also in LSB over certain converter ranges. The package types are FN and N. Please refer to the data sheet.

1

General Information

DATA ACQUISITION AND CONVERSION CROSS-REFERENCE GUIDE

1

General Information

Replacements are based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

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Manufacturers are arranged in alphabetical order.

ANALOG DEVICES	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
AD570JN		ADC0803CN	2-23
AD7512DIJN		TL182CN	2-87
AD7512DIJQ		TL182IN	2-87
AD7512DIKN		TL182CN	2-87
AD7512DIKQ		TL182IN	2-87
AD7512DISD		TL182MJ	2-87
AD7512DITD		TL182MJ	2-87
AD7520	TLC7533, AD7533B		3-65
AD7524AD	AD7524AN	TLC7524IN	2-3
AD7524JN	AD7524JN	TLC7524CN	2-3
AD7528BQ	AD7528BN	TLC7528IN	2-11
AD7528KN	AD7528KN	TLC7528CN	2-11
AD7533	TLC7533, AD7533		3-65
AD7820K/B/T	TLC0820A, ADC0820CC		2-189
AD7820L/C/U	TLC0820B, ADC0820BC		2-189
AD7533	TLC7533, AD7533		3-65
AD7820	TLC0820, ADC0820		2-189
ADC82AG		TLC0820BIN, ADC0820BCIN	2-189 2-189
ADC82AM		TLC0820AIN, ADC0820CCIN	2-189 2-189
ADC-830C			2-23
ADC-EK12DC		TL500/1/3CN	2-93
		TLC7135CN	2-69
		TLC7135CFN	2-69
		ICL7135CN	2-69
ADC-EK12DR		TL500/1/3CN	2-93
		TLC7135CN	2-69
		TLC7135CFN	2-69
		ICL7135CN	2-69
		ICL7135CFN	2-69
FUJITSU	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
MB4053P		TL507IN	2-115
MB40576	TL5501		3-13
MB40578	TLC5502		3-55
MB40776	TL5601		3-19
MB40778	TLC5602		3-61

DATA ACQUISITION AND CONVERSION CROSS-REFERENCE GUIDE

	DIRECT TI REPLACEMENT		PAGE NO.
HARRIS	TLC10		2-139
INTERSIL	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
ADC0803LCD	ADC0803IN		2-23
ADC0803LCN	ADC0803CN		2-23
ADC0804LCD	ADC0804IN		2-29
ADC0804LCN	ADC0804CN		2-29
DGM182AK	TL182MN	TL604MP	2-87
DGM182BJ	TL182CN IN	TL604CP/IP	2-87
DGM185AK	TL185MN	TL604MP	2-87
DGM185BJ	TL185CN/IN	TL604CP/IP	2-87
DGM188AK	TL188MN	TL610MP	2-87
DGM188BJ	TL188CN IN	TL610CP/IP	2-87
DGM191AK	TL191MN	TL610MP	2-87
DGM191BJ	TL191CN/IN	TL610CP/IP	2-87
ICL7135CPI	ICL7135CN		2-69
	ICL7135CFN		2-69
	TLC7135CN		2-69
	TLC7135CFN		2-69
LINEAR TECHNOLOGY	DIRECT TI REPLACEMENT		PAGE NO.
LTC1060ACN	TLC10N		2-139
LTC1060CN	TLC20N		2-139
MAXIM	DIRECT TI REPLACEMENT		PAGE NO.
MF10BN	TLC10N		2-139
MF10CN	TLC20N		2-139
MICRO NETWORKS		SUGGESTED TI REPLACEMENT	PAGE NO.
MN5100/5101		TLC0820ACN/TLC0820BCN, ADC0820BCN/ADC0820CCN	2-189
MN5120/5130/5140		TLC0820ACN/TLC0820BCN, ADC0820BCN/ADC0820CCN	2-189
			2-189
MICRO POWER SYSTEMS		SUGGESTED TI REPLACEMENT	PAGE NO.
MP7138AN		TL500/1/3CN	2-93
		TLC7135CN	2-69
		TLC7135CFN	2-69
		ICL7135CN	2-69
		ICL7135CFN	2-69
MP7574AD/BD		ADC0805IN series	2-23
MP7574JN/KN		ADC0804CN or ADC0805CN series	2-29
MP7581/JN/KN/AD/BD		ADC0808N/ADC0809N	2-35

DATA ACQUISITION AND CONVERSION CROSS-REFERENCE GUIDE

1

General Information

MOTOROLA	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
MC1405L		TL500CN/TL501CN/ TL505CN	2-93 2-107
MC14433P		TL500/1/3CN TLC7135CN TLC7135CFN ICL7135CN ICL7135CFN	2-93 2-69 2-69 2-69 2-69
MC14442L	TLC533AMJ	TLC532AMJ	2-155
MC14442P	TLC533AIN	TLC532AIN	2-155
MC14443P		TL507IN	2-115
MC14444P		TLC546IN	2-173
MC14447P		TL507IP	2-115
MC145040FN	TLC541MFN	TLC540MFN	2-165
MC145040L	TLC541MJ	TLC540MJ	2-165
MC145040P	TLC541MN	TLC540MN	2-165
MC145041P1	TLC542IN		3-27
MC54HC4016J	TLC4016MJ		2-209
MC74HC4016J	TLC4016IN		2-209
MC74HC4016N	TLC4016IN		2-209
MC54HC4066J	TLC4066MJ		2-217
MC74HC4066J	TLC4066IN		2-217
MC74HC4066N	TLC4066IN		2-217

NATIONAL	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO
ADC0803LCD	ADC0803IN		2-23
ADC0803LCN	ADC0803IN		2-23
ADC0804LCD	ADC0804IN		2-29
ADC0804LCN	ADC0804CN		2-29
ADC0805LCN	ADC0805IN		2-23
ADC0808CCJ	ADC0808N		2-35
	TI0808N		2-81
ADC0808CCN	ADC0808N		2-35
	TI0808N		2-81
ADC0809CCN	ADC0809N		2-35
	TL0809N		2-81
ADC0811BCJ	TLC541IN	1LC540IN	2-165
ADC0811BCN	TLC541IN	TLC540IN	2-165
ADC0811BCV	TLC541FN	TLC540IFN	2-165
ADC0811BJ	TLC541MJ	TLC540MJ	2-165
ADC0811CCJ	TLC541IN	TLC540IN	2-165
ADC0811CCN	TLC541N	1LC540IN	2-165
ADC0811CCV	TLC541FN	TLC540IFN	2-165
ADC0811CJ	TLC541MJ	TLC540MJ	2-165
ADC0820BCD	TLC0820BIN, ADC0820BCIN		2-189 2-189
ADC0820BCN	TLC0820BCN, ADC0820BCN		2-189 2-189
ADC0820BD	TLC0820BMJ, ADC0820BJ		2-189 2-189
ADC0820CCD	TLC0820AIN, ADC0820CCIN		2-189 2-189
ADC0820CCN	TLC0820ACN, ADC0820CCN		2-189 2-189
ADC0820CD	TLC0820AMJ, ADC0820CJ		2-189 2-189
ADC0829BCN	TLC533AIN	TLC532AIN	2-155
ADC0829CCN	TLC533AIN	TLC532AIN	2-155
ADC0830BCN		TLC546IN	2-173
ADC0830CCN		TLC546IN	2-173

DATA ACQUISITION AND CONVERSION CROSS-REFERENCE GUIDE

(Continued)

General Information

NATIONAL	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
ADC0831BCJ	ADC0831BIP	TLC549IN	2-49
ADC0831BCN	ADC0831BCP	TLC549IN	2-49
ADC0831CCJ	ADC0831AIP	TLC549IN	2-49
ADC0831CCN	ADC0831ACP	TLC549IN	2-49
ADC0832BCJ	ADC0832BIP		2-49
ADC0832BCN	ADC0832BCP		2-49
ADC0832CCJ	ADC0832AIP		2-49
ADC0832CCN	ADC0832ACP		2-49
ADC0834BCJ	ADC0834BIN		2-57
ADC0834BCN	ADC0834BCN		2-57
ADC0834CCJ	ADC0834AIN		2-57
ADC0834CCN	ADC0834ACN		2-57
ADC0838BCJ	ADC0838BIN		2-57
ADC0838BCN	ADC0838BCN		2-57
ADC0838CCJ	ADC0838AIN		2-57
ADC0838CCN	ADC0838ACN		2-57
ADC1001CCJ		TLC1541IN	2-199
ADC1005BCJ		TLC1541IN	2-199
ADC1005CCJ		TLC1541IN	2-199
ADC1225		TLC1225	3-43
ADC3511CCN		TL500/1/3CN	2-93
		TLC7135CN	2-69
		TLC7135CFN	2-69
		ICL7135CN	2-69
		ICL7135CFN	2-69
ADC3711CCN		TL500/1/3CN	2-93
		TLC7135CN	2-69
		TLC7135CFN	2-69
		ICL7135CN	2-69
		ICL7135CFN	2-69
ADD3501CCN		TL500/1/2CN	2-93
ADD3701CCN		TL500/1/2CN	2-93
MF10AN	TLC10CN		2-139
MF10CN	TLC20CN		2-139
MM54HC4016J	TLC4016MJ		2-209
MM54HC4066J	TLC4066MJ		2-217
MM74HC4016N/J	TLC4016IN		2-209
MM74HC4066N/J	TLC4066IN		2-217
MF4-50	TLC04 MF4A 50		2-127
MF4-100	TLC14 MF4A-100		2-127
PRECISION MONOLITHICS		SUGGESTED TI REPLACEMENT	PAGE NO
PM7524FQ		TLC7524IN, AD7524AN	2-225
PM7524FP		TLC7524CN, AD7524JN	2-225
PM7528		TLC7528, AD7528	2-233
PM7533		TLC7533, AD7533B	3-65
RCA	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
CD4016AD	TLC4016MJ		2-209
CD4016AE	TLC4016IN		2-209
CD4066AD	TLC4066MJ		2-217
CD4066AE	TLC4066IN		2-217
CA3162E		TL501CN/TL503CN	2-93

DATA ACQUISITION AND CONVERSION CROSS-REFERENCE GUIDE

SIGNETICS	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO
ADC0803/4/5-1LCN	ADC0803/4 5IN		2 23
ADC0804-1CN	ADC0804CN		2 29
NE5034F		TLC532AIN	2 155
NE5036FE/N/D		TLC549CN/CD	2 181
NE5037F/N/D		TLC549CN/CD	2 181
SILICONIX	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO
DG182AP	TL182MN	TL610MP	2-87
DG182BP	TL182CN/IN	TL610CP/IP	2 87
DG185AP	TL185MN	TL604MP	2 87
DG185BP	TL185CN/IN	TL604CP/IP	2-87
DG188AP	TL188MN	TL604MP	2 87
DG188BP	TL188CN IN	TL604CP IP	2 87
DG191AP	TL191MN	TL604MP	2-87
DG191BP	TL191CN-IN	TL604CP IP	2 87
LD110CJ		TL503CN	2-93
		TLC7135CN	2-69
		TLC7135CFN	2-69
		ICL7135CN	2-69
		ICL7135CFN	2-69
LD111ACJ		TL501CN	2 93
		TLC7135CN	2 69
		TLC7135CFN	2 69
		ICL7135CN	2 69
		ICL7135CFN	2 69
LD120CJ		TL500CN	2 93
		TLC7135CN	2-69
		TLC7135CFN	2 69
		ICL7135CN	2 69
		ICL7135CFN	2-69
LD121ACJ		TL503CN	2-93
		TLC7135CN	2-69
		TLC7135CFN	2 69
		ICL7135CN	2 69
		ICL7135CFN	2 69
S:520DJ		ADC0808N/	2 35
		ADC0809N	2 35
Si7135CJ	TLC7135CN		2 69
	TLC7135CFN		2-69
	ICL7135CN		2-69
	ICL7135CFN		2 69

1
General Information

DATA ACQUISITION AND CONVERSION CROSS-REFERENCE GUIDE



General Information

TELEDYNE	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO
TSC7135CPI	TLC7135CN TLC7135CFN ICL7135CN ICL7135CFN		2-69 2-69 2-69 2-69
TSC8700		ADC0808N	2-35
TSC8701		TLC1541IN	2-199
TSC8703		ADC0808N	2-35
TSC8704		TLC1541IN	2-199
TSC14433CN		TLC7135CN TLC7135CFN ICL7135CN ICL7135CFN	2-69 2-69 2-69 2-69



TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR
ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS

INTRODUCTION

These terms, definitions, and letter symbols are in accordance with those currently approved by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

1. GENERAL TERMS

Analog-to-Digital Converter (ADC)

A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of which exclusively represents a fractional part of the total analog input range. (See Figure 1.)

NOTE: This quantization procedure introduces inherent errors of one-half LSB (least significant bit) in the representation since, within this fractional range, only one analog value can be represented free of error by a single digital output code.

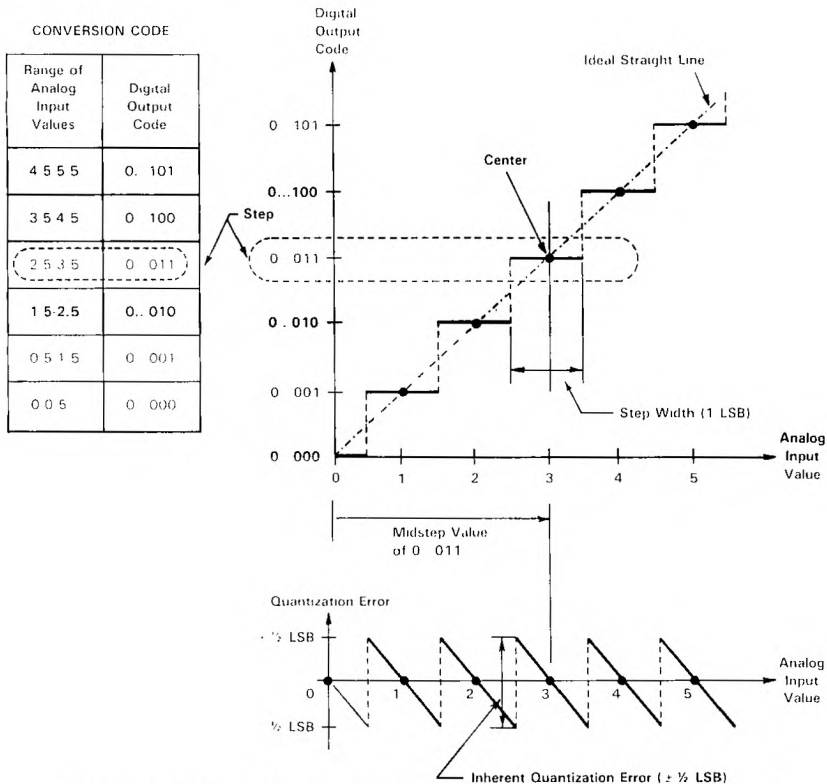


FIGURE 1. ELEMENTS OF TRANSFER DIAGRAM FOR AN IDEAL LINEAR ADC

GLOSSARY

TERMS, DEFINITIONS AND LETTER SYMBOLS

Analog-to-Digital Processor

An integrated circuit providing the analog part of an ADC; provision of external timing, counting, and arithmetic operations is necessary for implementing a full analog-to-digital converter.

Companding DAC

A DAC whose transfer function complies with a compression or expansion law.

NOTE 1: The corresponding ADC normally consists of such a companding DAC and additional external circuitry.

NOTE 2: The compression or expansion law is usually a logarithmic function, e.g., A-law or μ -law.

Conversion Code (of an ADC or a DAC)

The set of correlations between each of the fractional parts of the total analog input range or each of the digital input codes, respectively, and the corresponding digital output codes or analog output values, respectively. (See Figures 1 and 2.)

NOTE: Examples of output code formats are straight binary, 2's complement, and binary-coded decimal.

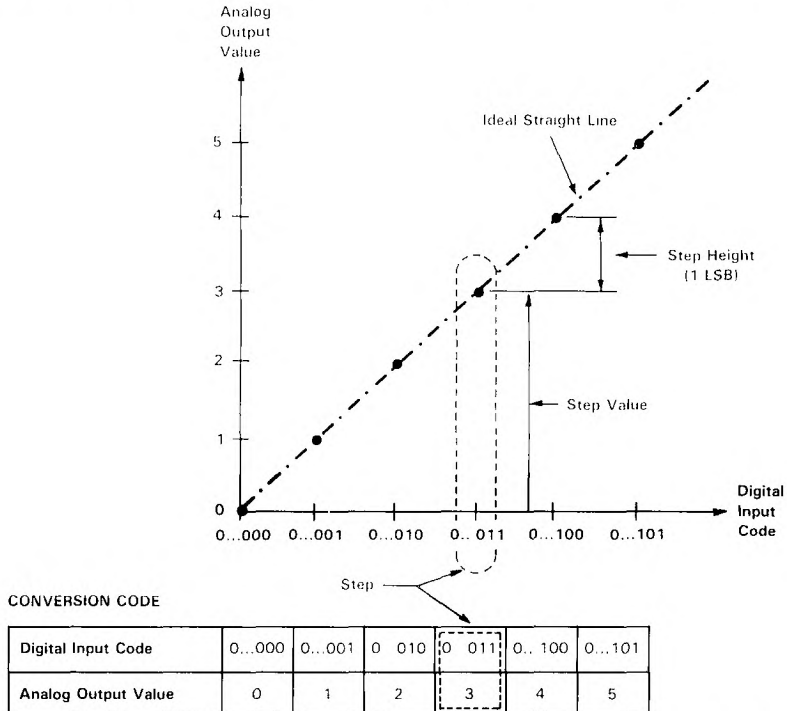


FIGURE 2. ELEMENTS OF TRANSFER DIAGRAM FOR AN IDEAL LINEAR DAC

Digital-to-Analog Converter (DAC)

A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values. (See Figure 2.)

NOTE: Examples of input code formats are straight binary, 2's complement, and binary-coded decimal.

Full Scale (of a unipolar ADC or DAC)

A term used to refer a characteristic to that step within the transfer diagram whose nominal midstep value or nominal step value has the highest absolute value. (See Figure 3a for a linear unipolar ADC.)

NOTE 1: The subscript for the letter symbol of a characteristic at full scale is "FS".

NOTE 2: In place of a letter symbol, the abbreviation "FS" is in common use.

Full Scale, Negative (of a bipolar ADC or DAC) (See Figures 3b and 3c)

A term used to refer a characteristic to the negative end of the transfer diagram, that is, to the step whose nominal midstep value or nominal step value has the most-negative value.

NOTE 1: The subscript for the letter symbol of a characteristic at negative full scale is "FS-" (V_{FS-} , I_{FS-}).

NOTE 2: In place of a letter symbol, the abbreviation "FS-" is in common use.

Full Scale, Positive (of a bipolar ADC or DAC) (See Figure 3b and 3c)

A term used to refer a characteristic to the positive end of the transfer diagram, that is, to the step whose nominal midstep value or nominal step value has the most-positive value.

NOTE 1: The subscript for the letter symbol of a characteristic at positive full scale is "FS+" (V_{FS+} , I_{FS+}).

NOTE 2: In place of a letter symbol, the abbreviation "FS+" is in common use.

Full-Scale Range, Nominal (of a linear ADC or DAC) (V_{FSRnom} , I_{FSRnom}) (See Figure 3)

The total range in analog values that can be coded with uniform accuracy by the total number of steps with this number rounded to the next higher power of 2.

NOTE: In place of the letter symbols, the abbreviation "FSR(nom)" can be used.

Example: Using a straight binary n-bit code format, it follows:

- for an ADC: $FSR(nom) = 2^n \times (\text{nominal value of step width})$
- for a DAC: $FSR(nom) = 2^n \times (\text{nominal value of step height})$

Full-Scale Value, Nominal (V_{FSnom} , I_{FSnom})

A value derived from the nominal full-scale range:

- for a unipolar converter: $V_{FSnom} = V_{FSRnom}$
 - for a bipolar converter: $V_{FSnom} = 1/2 V_{FSRnom}$
- (See Figure 3.)

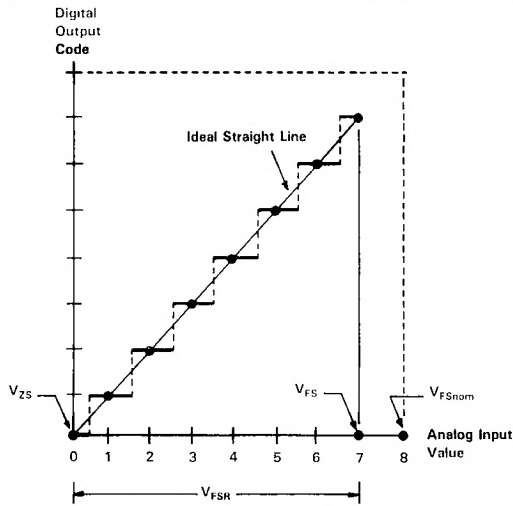
NOTE 1: In a few data sheets, this analog value is used as a reference value for adjustment procedures or as a rounded value for the full-scale range(s).

NOTE 2: In place of letter symbols, the abbreviation "FS(nom)" is in common use.

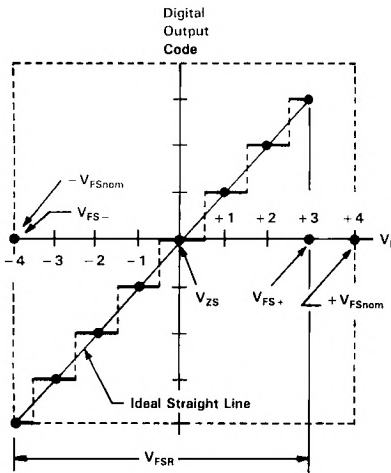
GLOSSARY TERMS, DEFINITIONS AND LETTER SYMBOLS

1

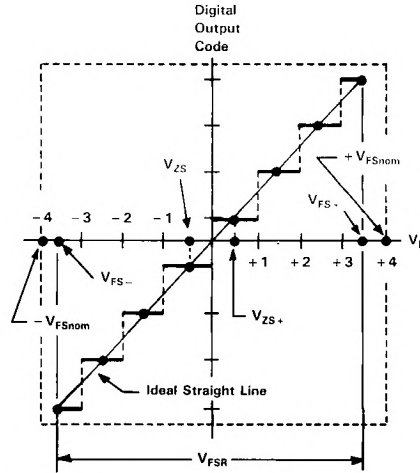
General Information



a. UNIPOLAR ADC



b. BIPOLAR ADC WITH TRUE ZERO



c. BIPOLAR ADC WITH NO TRUE ZERO

V_i = Analog Input Value

FIGURE 3. IDEAL STRAIGHT LINE, FULL-SCALE VALUE AND ZERO-SCALE VALUE (SHOWN FOR IDEAL LINEAR ADCs)

Full-Scale Range, (Practical) (of a linear ADC or DAC) (V_{FSR} , I_{FSR}) (V_{FSRpr} , I_{FSRpr}) (See Figure 3)
The total range of analog values that correspond to the ideal straight line.

NOTE 1: The qualifying adjective "practical" can usually be deleted from this term provided that, in a very few critical cases, the term "nominal full-scale range" is not also shortened in the same way. This permits use of the shorter letter symbols or abbreviations. (See Note 2.)

NOTE 2: In place of the letter symbols, the abbreviations "FSR" and "FSR(pr)" are in common use.

NOTE 3: The (practical) full-scale range has only a nominal value because it is defined by the end points of the ideal straight line.

Example: Using a straight binary n-bit code format, it follows:
– for an ADC: $FSR = (2^n - 1) \times (\text{nominal value of step width})$
– for a DAC: $FSR = (2^n - 1) \times (\text{nominal value of step height})$

Gain Point (of an adjustable ADC or DAC)

The point in the transfer diagram corresponding to the midstep value (for an ADC) or the step value (for a DAC) of the step for which gain error is specified (usually full scale), and in reference to which the gain adjustment is performed. (See Figures 4 and 5.)

NOTE: Gain adjustment causes only a change of the slope of the transfer diagram, without changing the offset error.

Ideal Straight Line (of a linear ADC or DAC)

In the transfer diagram, a straight line between the specified points for the most-positive (least-negative) and most-negative (least-positive) nominal midstep values or nominal step values, respectively. (See Figures 1, 2, and 3.)

NOTE: The ideal straight line passes through all the points for nominal midstep values or nominal step values, respectively.

Linear ADC

An ADC having steps ideally of equal width excluding the steps at the two ends of the total range of analog input values.

NOTE: Ideally, the width of each end steps is one half of the width of any other step. (See Figure 1.)

Linear DAC

A DAC having steps ideally of equal height. (See Figure 2.)

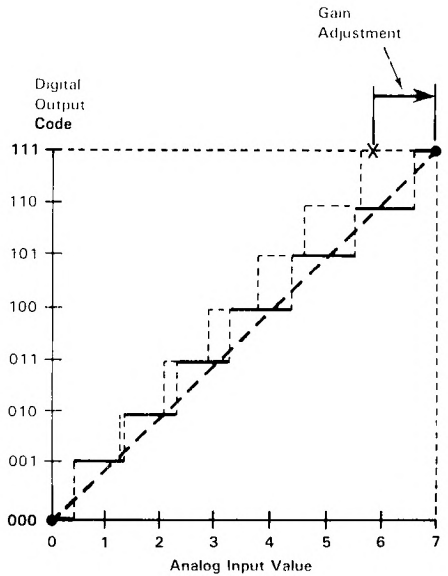
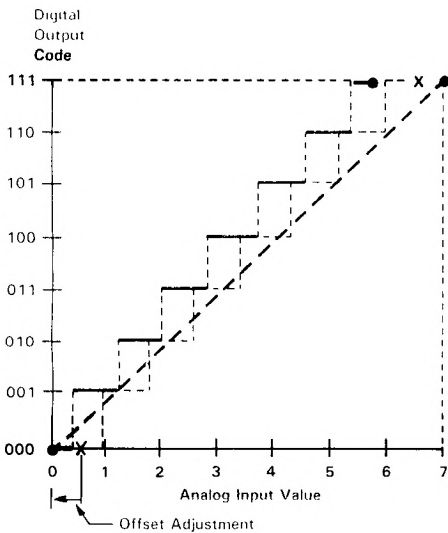
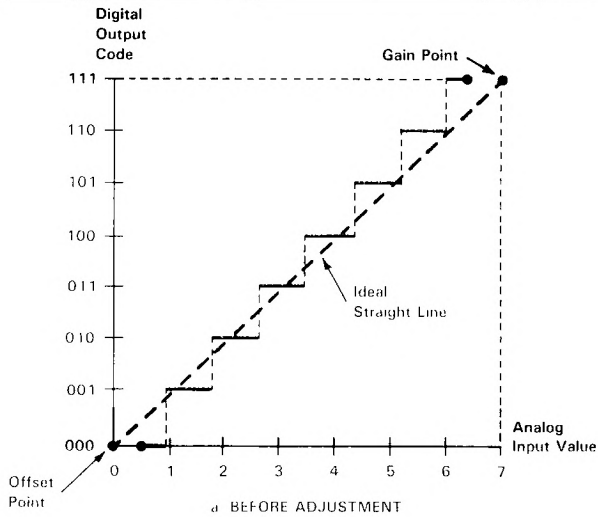
LSB, Abbreviation

The abbreviation for "Least Significant Bit", that is, for the bit that has the lowest positional weight in a natural binary numeral.

Example: In the natural binary numeral "1010", the rightmost bit "0" is the LSB.

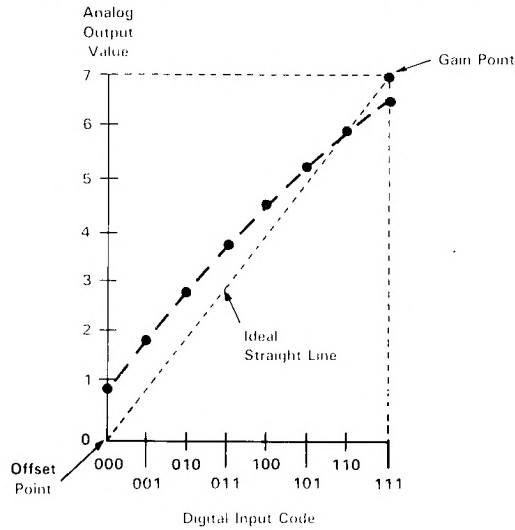
GLOSSARY

TERMS, DEFINITIONS AND LETTER SYMBOLS

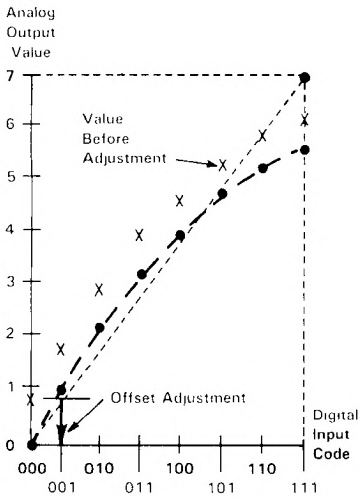


NOTE: In the above examples, the offset point is referred to the step with the digital code 000, and the gain point is referred to the step with the digital code 111.

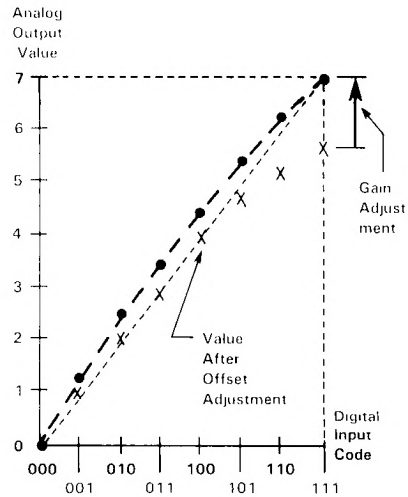
FIGURE 4. ADJUSTMENT IN OFFSET POINT AND GAIN POINT FOR AN ADC



a BEFORE ADJUSTMENT



b AFTER OFFSET ADJUSTMENT



c. AFTER OFFSET AND GAIN ADJUSTMENTS

NOTE: In the above examples, the offset point is referred to the step with the digital code 000, and the gain point is referred to the step with the digital code 111.

FIGURE 5. ADJUSTMENT IN OFFSET AND GAIN POINT FOR A DAC

GLOSSARY

TERMS, DEFINITIONS AND LETTER SYMBOLS

LSB, Unit Symbol (for linear converters only)

The unit symbol for the magnitude of the analog resolution of a linear converter, which serves as a reference unit to express the magnitude of other analog quantities of that same converter, especially of analog errors, as multiples or submultiples of the magnitude of the analog resolution.

Example: "1/2 LSB" means an analog quantity equal to 0.5 times the analog resolution.

NOTE: The unit symbol LSB refers to the fact that, for a natural binary code, the analog resolution corresponds to the nominal positional weight attributed to the least significant bit of the binary numeral.

In this case, the identity:

$$1 \text{ LSB} = \text{analog resolution}$$

leads, for an n-bit resolution, to:

$$1 \text{ LSB} = \frac{\text{FSR}}{2^n - 1} = \frac{\text{FSR}(\text{nom})}{2^n}$$

Midstep Value (of an ADC)

The analog value for the center of the step excluding the steps at the two ends of the total range of analog input values.

NOTE: For the end steps, the midstep value is defined as the analog value that results when the analog value for the transition to the adjacent step is reduced or enlarged, as appropriate, by half the nominal value of the step width. (See Figure 1.)

Midstep Value, Nominal (of an ADC)

A specified analog value within a step that is ideally represented free of error by the corresponding digital output code. (See Figure 1.)

Missing Code (of an ADC)

An intermediate code that is absent when the changing analog input to an ADC causes a multiple code change in the digital output. (See Figure 6.)

Monotonicity (of an ADC or a DAC)

A property of the transfer function that ensures the consistent increase or decrease of the analog output of a DAC or the digital output of an ADC in response to a consistent increase or decrease of the digital or analog input, respectively. (Figure 7 illustrates nonmonotonic conversion.)

NOTE: An intermediate increment with the value of zero does not invalidate monotonicity.

Multiplying DAC

A DAC having at least two inputs, at least one of which is digital, and whose analog output value is proportional to the product of the inputs.

Nonlinear ADC or DAC

An ADC or a DAC with a specified nonlinear transfer function between the nominal midstep values or nominal step values, respectively, and the corresponding step widths or step heights, respectively.

NOTE: The function may be continuously nonlinear or piece-wise linear.

Offset Point (of an adjustable ADC or DAC)

The point in the transfer diagram corresponding to the midstep value (for an ADC) or the step value (for a DAC) of the step about which the transfer diagram rotates when gain is adjusted. (See Figures 4 and 5.)

NOTE: Offset adjustment must be performed with respect to this point so that it causes only a parallel displacement of the transfer diagram, without changing its slope.

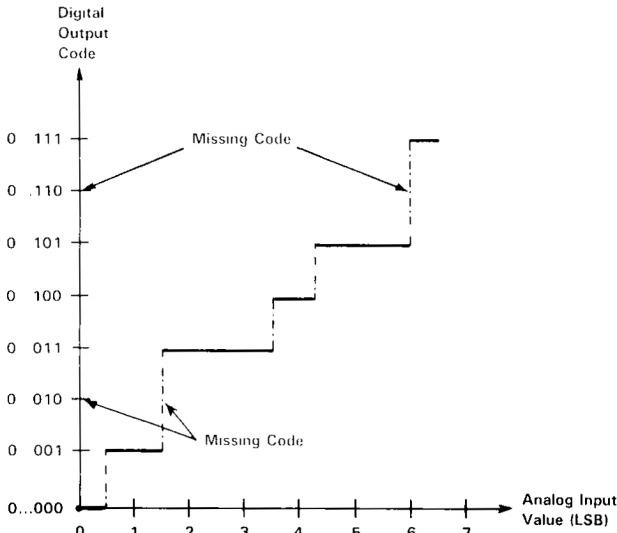


FIGURE 6. MISSING CODE FOR AN ADC

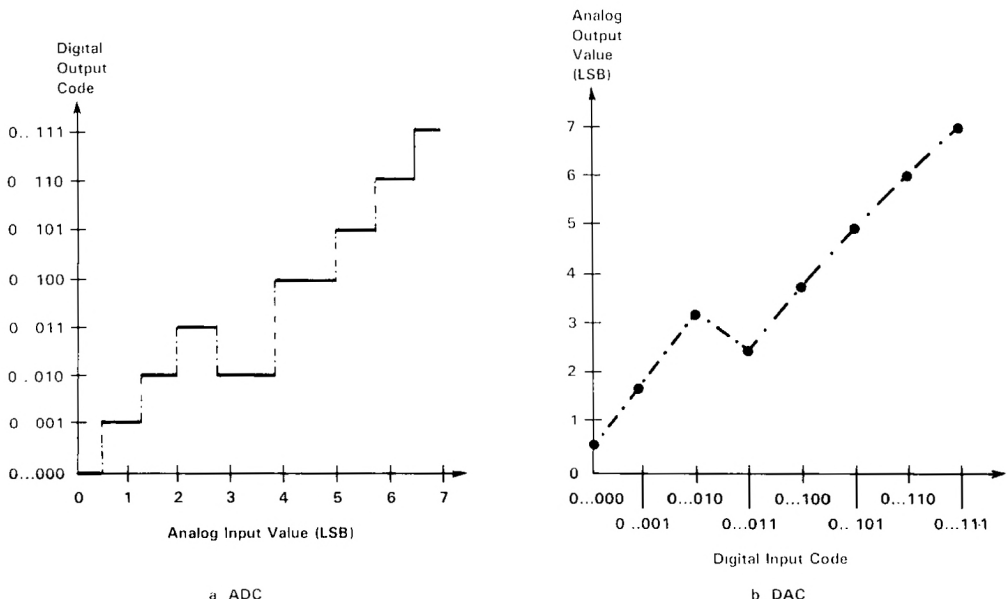


FIGURE 7. NONMONOTONIC CONVERSION OF AN ADC OR DAC

GLOSSARY

TERMS, DEFINITIONS AND LETTER SYMBOLS

Resolution (general term)

NOTE 1: Resolution as a capability can be expressed in different forms: (see "resolution, analog", "resolution, numerical", and "resolution, relative").

NOTE 2: Resolution is a design parameter and therefore has only a nominal value.

NOTE 3: The terms for these different forms may all be shortened to "resolution" if no ambiguity is likely to occur (for example, when the dimension of the term is also given).

Resolution (of an ADC)

The degree to which nearly equal values of the analog input quantity can be discriminated.

Resolution (of a DAC)

The degree to which nearly equal values of the analog output quantity can be produced.

Resolution, Analog (of a linear or nonlinear ADC or DAC)

For an ADC: The nominal value of the step width.

For a DAC: The nominal value of the step height.

NOTE: For a linear ADC or DAC, the constant magnitude of the analog resolution is often used as the reference unit LSB.

Resolution, Numerical

The number (n) of digits in the chosen numbering system necessary to express the total number of steps.

NOTE 1: The numbering system is normally a binary or a decimal system.

NOTE 2: In the binary-coded-decimal numbering system, the term "1/2 digit" refers to an additional decimal digit with the highest positional value, but limited to the decimal figures "0" or "1" as it is represented by only a single bit. This additional digit serves to double the range of values covered by the other "n" digits.

Resolution, Relative (of a linear ADC or DAC)

The ratio of the analog resolution to the full-scale range (practical or nominal).

NOTE: This ratio is normally expressed as a percentage of the full-scale range [% of FSR, % of FSR(nom)]. For high resolutions (high value of n), it is of little importance whether this ratio refers to the practical or nominal full-scale range.

Step (of an analog-to-digital or digital-to-analog conversion)

In the conversion code: Any of the individual correlations.

In the transfer diagram: Any part of the diagram equating to an individual correlation.

For an ADC, a step represents both a fractional range of analog input values and the corresponding digital output code. (See Figure 1.)

For a DAC, a step represents both a digital input code and the corresponding discrete analog output value. (See Figure 2.)

Step Height (Step Size) (of a DAC)

The absolute value of the difference in step value between two adjacent steps in the transfer diagram. (See Figure 2.)

NOTE: For companding DACs, the term "step size" is in general use.

Step Value (of a DAC)

The value of the analog output representing a digital input code. (See Figure 2.)

Step Value, Nominal (of a DAC)

A specified step value that represents free of error the corresponding digital input code. (See Figure 2.)

Step Width (of an ADC)

The absolute value of the difference between the two ends of the range of analog values corresponding to one step. (See Figure 1.)

Temperature Coefficients of Analog Characteristics (α)

NOTE 1: The letter symbol for the temperature coefficient of an analog characteristic consists of the letter symbol α with a subscript referring to the relevant characteristic.

Example: Temperature coefficient of the gain error: α_{EG}

NOTE 2: Temperature coefficients are usually specified in "parts per million (relative to the full-scale value) per degrees Celsius", that is, in "ppm/°C".

Zero Scale (of an ADC or a DAC with true zero) (See Figures 3a and 3b)

A term used to refer a characteristic to the step whose nominal midstep value or nominal step value equals zero.

NOTE 1: The subscript for the letter symbol of a characteristic at zero scale is "ZS".

NOTE 2: In place of a letter symbol, the abbreviation "ZS" is in common use.

Zero Scale, Negative (of an ADC or a DAC with no true zero) (See Figure 3c)

A term used to refer a characteristic to the negative step closest to analog zero.

NOTE 1: The subscript for the letter symbol of a characteristic at negative zero scale is "ZS-" (V_{ZS-} , I_{ZS-}).

NOTE 2: In place of a letter symbol, the abbreviation "ZS-" is in common use.

Zero Scale, Positive (of an ADC or a DAC with no true zero) (See Figure 3c)

A term used to refer a characteristic to the positive step closest to analog zero.

NOTE 1: The subscript for the letter symbol of a characteristic at positive zero scale is "ZS+" (V_{ZS+} , I_{ZS+})

NOTE 2: In place of a letter symbol, the abbreviation "ZS+" is in common use.

2. STATIC PERFORMANCE

Accuracy (see Errors', Part 4)

Asymmetry, Full-Scale (of a DAC with a bipolar analog range) (ΔI_{FSS} , ΔV_{FSS})

The difference between the absolute values of the two full-scale analog values.

Compliance, Current (of a DAC) ($I_{O(op)}$)

The permissible range of output current within which the specifications are valid.

Compliance, Voltage (of a DAC) ($V_{O(op)}$)

The permissible range of output voltage within which the specifications are valid.

Errors (see Part 4)

GLOSSARY

TERMS, DEFINITIONS AND LETTER SYMBOLS

Supply Voltage Sensitivity, (of a DAC) (k_{SVS})

The change in full scale output current (or voltage) caused by a change in supply voltage.

NOTE: This sensitivity is usually expressed as the ratio of the percent change of full-scale current (or voltage) to the percent change of supply voltage.

3. DYNAMIC PERFORMANCE

Conversion Rate (of an externally controlled ADC) (f_c)

The number of conversions per unit time.

NOTE 1: The maximum conversion rate should be specified for full resolution.

NOTE 2: The conversion rate is usually expressed as the number of conversions per second.

NOTE 3: Due to additionally needed settling or recovery times, the maximum specified conversion rate is smaller than the reciprocal of the worst-case conversion time.

Conversion Time (of an ADC) (t_c)

The time elapsed between the command to perform a conversion and the appearance at the converter output of the complete digital representation of the analog input value.

Delay Time, (Digital) (of a linear or a multiplying DAC) (t_d , t_{dd})

The time interval between the instant when the digital input changes and the instant when the analog output passes a specified value that is close to its initial value, ignoring glitches. (See Figure 8.)

NOTE: For a multiplying DAC, the full term and the additional subscript d must be used to distinguish between the digital and the delay time.

Delay Time, Reference (of a multiplying DAC) (t_{dr})

The time interval between the instant when a step change of the reference voltage occurs and the instant when the analog output passes a specified value that is close to its initial value.

Feedthrough Capacitance (C_F)

The value of the capacitance for a specified value of R in an equivalent circuit for the calculation of the feedthrough error.

NOTE: The equivalent circuit consists of a high-pass R-C filter between the reference input and the analog output.

Feedthrough Error (see Part 4)

Glitch (of a DAC)

A short, undesirable transient in the analog output occurring following a code change at the digital input. (See Figure 8.)

Glitch Area (of a DAC)

The time integral of the analog value of the glitch transient.

NOTE 1: Usually, the maximum specified glitch area refers to a specified worst-case code change.

NOTE 2: Instead of a letter symbol, the abbreviation "GA" is in use.

Glitch Energy (of a DAC)

The time integral of the electrical power of the glitch transient.

NOTE 1: Usually, the maximum specified glitch energy refers to a specified worst-case code change.

NOTE 2: Instead of a letter symbol, the abbreviation "GE" is in use.

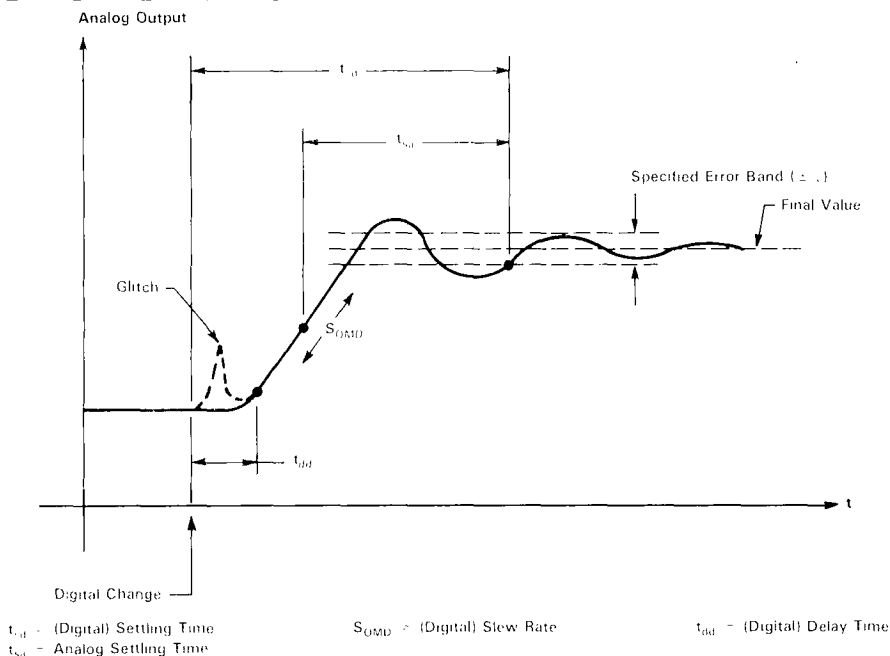


FIGURE 8. OUTPUT CHARACTERISTICS OF A LINEAR OR A MULTIPLYING DAC FOR A STEP CHANGE IN THE DIGITAL INPUT CODE

Pedestal (Error) (E_p) (see Part 4)

Ramp Delay, Steady-State (of a multiplying DAC) ($t_d(\text{ramp})$)

The time separation between the actual curve of the analog output and the theoretical curve (with no delay) for a ramp in reference voltage, after the settling time to steady-state ramp has elapsed. (See Figure 9.)

Settling Time, Analog (of a DAC) (t_{sa})

The time interval between the instant when the analog output passes a specified value and the instant when the analog output enters for the last time a specified error band about its final value. (See Figures 8 and 10.)

Settling Time, (Digital) (of a linear or a multiplying DAC) (t_s , t_{sd})

The time interval between the instant when the digital input changes and the instant when the analog output value enters for the last time a specified error band about its final value. (See Figure 8.)

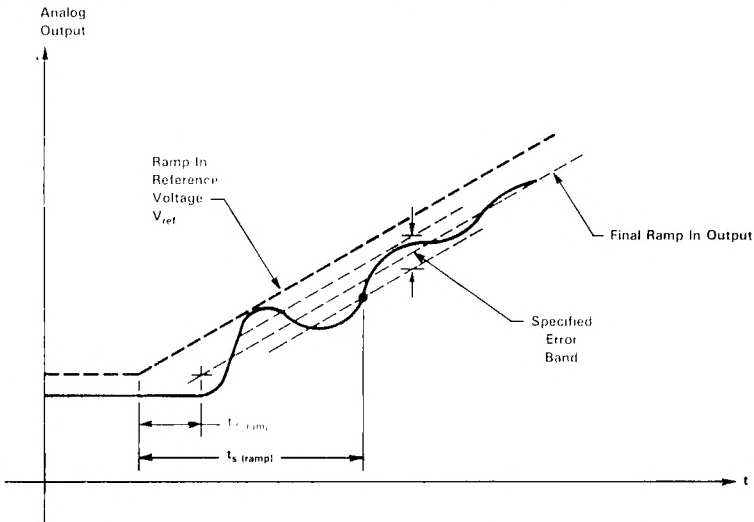
NOTE: For a multiplying DAC, the full term and the additional subscript d must be used to distinguish between the digital and the settling time.

Settling Time, Reference (of a multiplying DAC) (t_{sr})

The time interval between the instant when a step change of the reference voltage occurs and the instant when the analog output enters for the last time a specified error band about its final value. (See Figure 10.)

NOTE: Specifications for the reference settling time are usually given for the highest allowed step change in reference voltage.

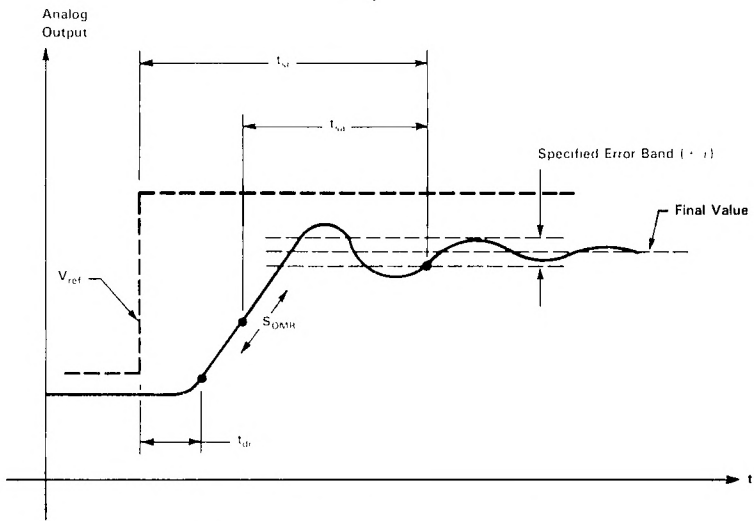
GLOSSARY TERMS, DEFINITIONS AND LETTER SYMBOLS



$t_s(\text{ramp})$ = Settling Time To Steady-State Ramp Delay

$t_d(\text{ramp})$ = Steady-State Ramp Delay

FIGURE 9. OUTPUT CHARACTERISTICS FOR A RAMP IN REFERENCE VOLTAGE OF A MULTIPLYING DAC



t_{dr} = Reference Delay Time

t_{sr} = Reference Settling Time

$S_{0.0511}$ = Reference Slew Rate

t_{sa} = Analog Settling Time

FIGURE 10. OUTPUT CHARACTERISTICS FOR A STEP CHANGE IN REFERENCE VOLTAGE OF A MULTIPLYING DAC

Settling Time to Steady-State Ramp (of a multiplying DAC) ($t_{s(\text{ramp})}$)

The time interval between the instant a ramp in the reference voltage starts and the instant when the analog output value enters for the last time a specified error band about the final ramp in the output. (See Figure 9.)

Skewing Time, Internal (of a DAC)

The difference in internal delay between the individual output transitions for a given change of digital input.

NOTE: The internal (and external) skew has a major influence on the settling time for critical changes in the digital input, for example, for a 1-LSB change from 011 . . . 111 to 100 . . . 000, and is an important source of commutation noise.

Slew Rate, (Digital) (of a linear or a multiplying DAC) (S_{OM} , S_{OMD})

The maximum rate of change of the analog output value when a change of the digital input code causes a large step change of the analog output value. (See Figure 8.)

NOTE 1: For a multiplying DAC, the full term and the additional subscript D must be used to distinguish between the digital and the slew rate.

NOTE 2: The abbreviations "SR" and "SR(dig)" are also used.

Slew Rate, Reference (of a multiplying DAC) (S_{OMR})

The maximum rate of change of the analog output following a large step change of the reference voltage. (See Figure 10.)

NOTE: The abbreviation "SR(ref)" is also used.

4. ERRORS, ACCURACY

The definitions in this section describe the errors as the difference between the actual value and the nominal value of the analog quantity. As such they may be expressed in conventional units (for example, millivolts) or as multiples or submultiples of 1 LSB. An error can also be expressed as a relative value, for example, in "% of FSR". In this case, it is common practice to use the same term as for the analog value.

Absolute Accuracy Error

Synonym for total error.

Feedthrough Error (of a multiplying DAC) (E_f)

An error in analog output due to variation in the reference voltage that appears as an offset error and is proportional to frequency and amplitude of the reference signal.

NOTE 1: The specification for the feedthrough error is given for the digital input for which the offset error is specified, and for a reference signal of specified frequency and amplitude.

NOTE 2: This error may also be expressed as a peak-to-peak analog value.

Full-Scale Error (of a linear ADC or DAC) (E_{FS})

The difference between the actual midstep value or step value and the nominal midstep value or step value, respectively, at specified full scale.

NOTE: Normally, this error specification is applied to converters that have no arrangement for an external adjustment of offset error and gain error.

GLOSSARY

TERMS, DEFINITIONS AND LETTER SYMBOLS

Gain Error (of a linear ADC or DAC) (E_G)

For an ADC: The difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. (See Figure 11a.)

For a DAC: The difference between the actual step value and the nominal step value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. (See Figure 11b.)

NOTE: See Notes 1 and 2 under "Offset Error".

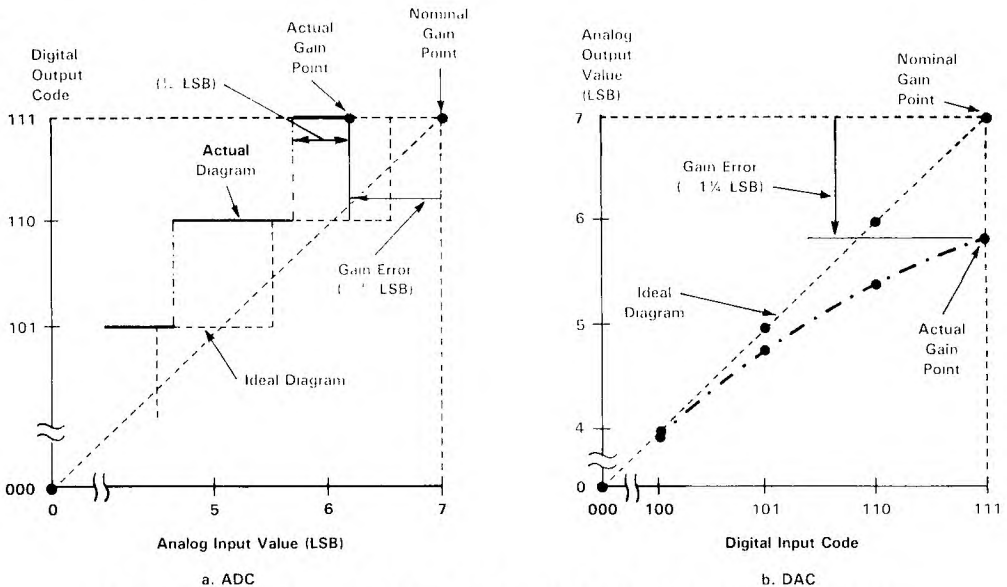


FIGURE 11. GAIN ERROR OF A LINEAR 3-BIT NATURAL BINARY CODE CONVERTER (SPECIFIED AT STEP 111), AFTER CORRECTION OF THE OFFSET ERROR

Instability, Long-Term (Accuracy) ($\Delta E(\Delta t)$, $\Delta E(t)$)

The additional error caused by the aging of the components and specified for a longer period in time.

Linearity Error, Best-Straight-Line (of a linear and adjustable ADC) ($E_{L(adj)}$)

The difference between the actual analog value at the transition between any two adjacent steps and its *ideal* value after offset error and gain error have been adjusted to minimize the magnitude of the extreme values of this difference. (See Figure 12a.)

NOTE 1: The inherent quantization error is not included in the best-straight-line linearity error of an ADC. The ideal value for the transition corresponds to the nominal midstep value $\pm 1/2$ LSB.

NOTE 2: For a uniformly curved transfer diagram, the extreme values will be very close to half of the magnitude of the end-point linearity error. (See Figure 12a.)

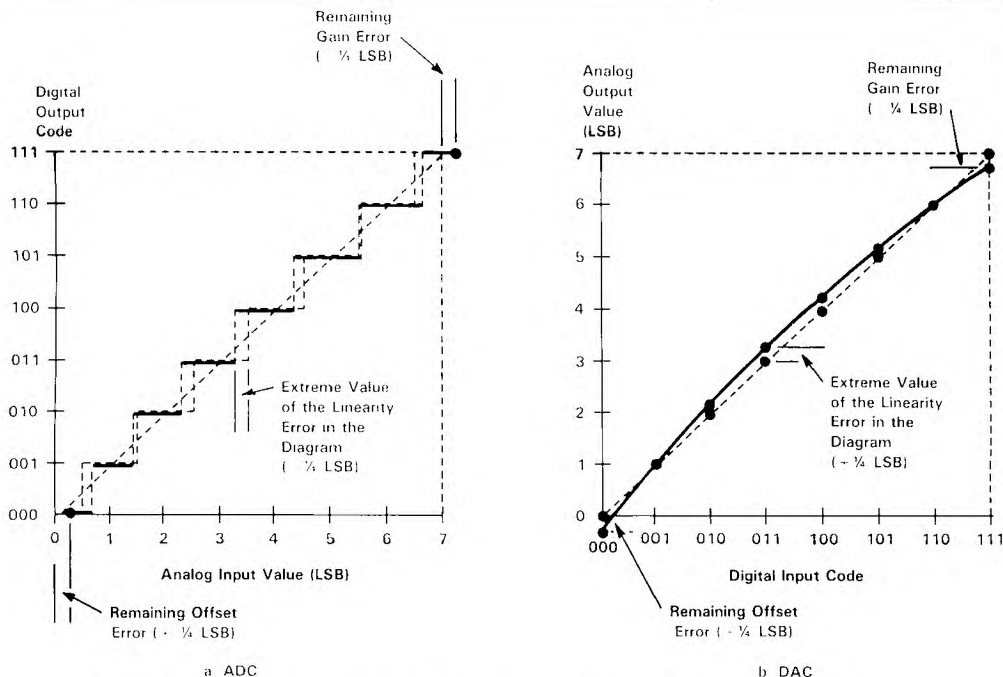


FIGURE 12. BEST-STRAIGHT-LINE LINEARITY ERROR OF A LINEAR 3-BIT NATURAL BINARY-CODED CONVERTER (VALUES BETWEEN $\pm 1/4$ LSB)

Linearity Error, Best-Straight-Line (of a linear and adjustable DAC) ($E_{L(adj)}$)

The difference between the actual step value and the nominal step value after offset error and gain error have been adjusted to minimize the magnitude of the extreme values of this difference. (See Figure 12b.)

NOTE: For a uniformly curved transfer diagram, the extreme values will be very close to half of the magnitude of the end-point linearity error. (See Figure 12b.)

Linearity Error, Differential (of a linear ADC or DAC) (E_D)

The difference between the actual step width or step height and the ideal value (1 LSB). (See Figure 13.)

NOTE: A differential linearity error greater than 1 LSB can lead to missing codes in an ADC or to nonmonotonicity of an ADC or a DAC. (See Figures 6 and 7.)

Linearity Error, End-Point (of a linear and adjustable ADC) (E_L)

The difference between the actual analog value at the transition between any two adjacent steps and its ideal value after offset error and gain error have been adjusted to zero. (See Figure 14a.)

NOTE 1: The short term "linearity error" is in common use and is sufficient if no ambiguity with the "best-straight-line linearity error" is likely to occur.

NOTE 2: The inherent quantization error is not included in the linearity error of an ADC. The ideal value for the transition corresponds to the nominal midstep value $\pm 1/2$ LSB.

GLOSSARY TERMS, DEFINITIONS AND LETTER SYMBOLS

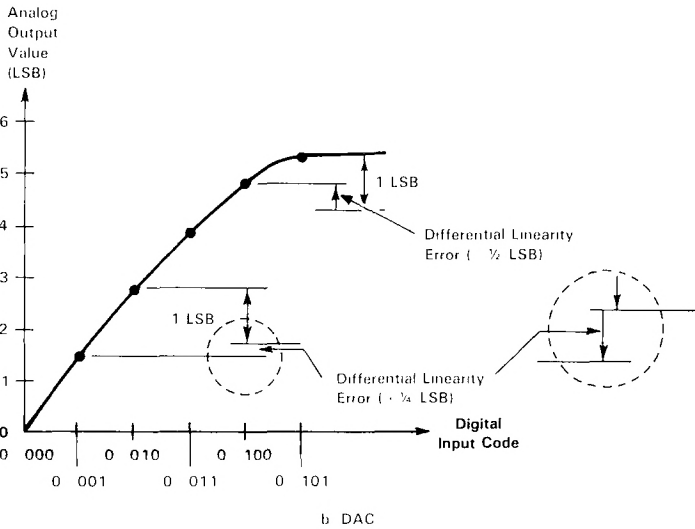
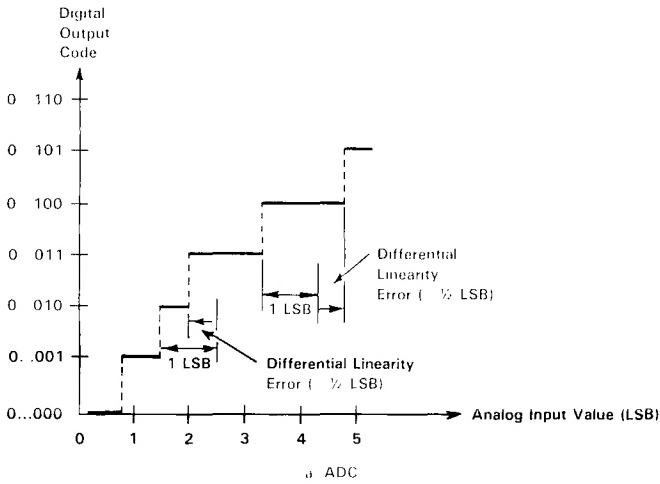


FIGURE 13. DIFFERENTIAL LINEARITY ERROR OF A LINEAR ADC OR DAC

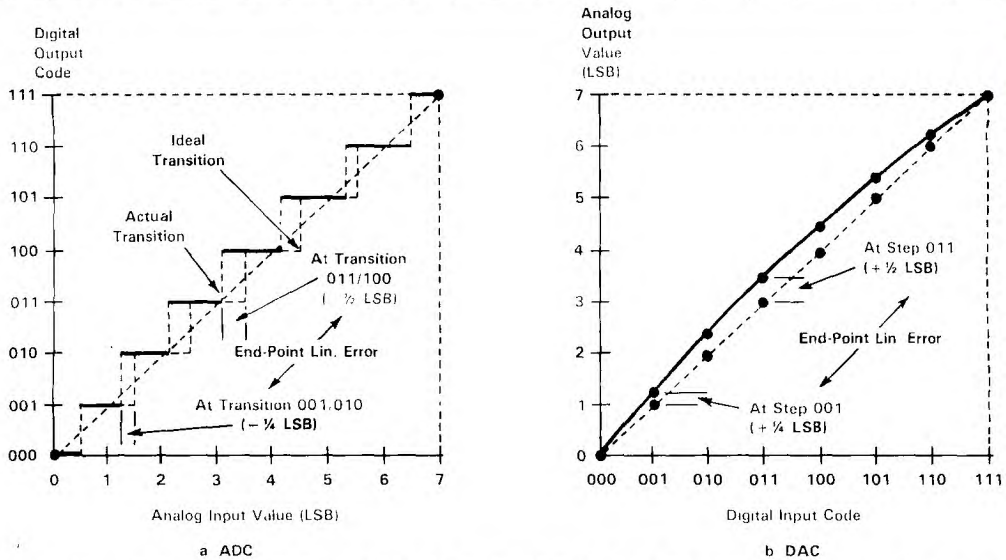


FIGURE 14. END-POINT LINEARITY ERROR OF A LINEAR 3-BIT NATURAL BINARY-CODED ADC OR DAC (OFFSET ERROR AND GAIN ERROR ARE ADJUSTED TO THE VALUE ZERO)

Linearity Error, End-point (of a linear and adjustable DAC) (E_L)

The difference between the actual step value and the nominal step value after offset error and gain error have been adjusted to zero. (See Figure 14b.)

NOTE: The short term "linearity error" is in common use and is sufficient if no ambiguity with the "best-straight-line linearity error" is likely to occur.

Offset Error (of a linear ADC or DAC) (E_O)

For an ADC: The difference between the actual midstep value and the nominal midstep value at the offset point. (See Figure 15a.)

For a DAC: The difference between the actual step value and the nominal step value at the offset point. (See Figure 15b.)

NOTE 1: Usually, the specified steps for the specification of offset error and gain error are the steps at the ends of the practical full-scale range. For an ADC, the midstep value of these steps is defined as the value for a point 1/2 LSB apart from the adjacent transition. (See Figures 11 and 15.)

NOTE 2: The terms "offset error" and "gain error" should be used only for errors that can be adjusted to zero. Otherwise, the terms "zero-scale error" and "full-scale error" should be used.

Pedestal (Error) (E_P)

A dynamic offset error produced in the commutation process.

GLOSSARY

TERMS, DEFINITIONS AND LETTER SYMBOLS

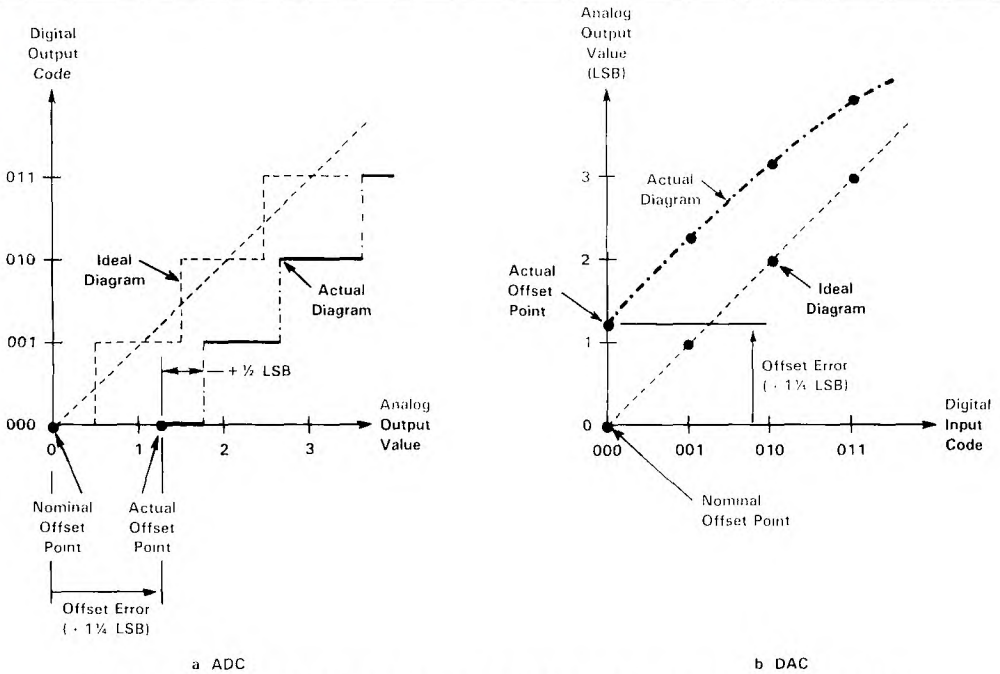


FIGURE 15. OFFSET ERROR OF A LINEAR 3-BIT NATURAL BINARY CODE CONVERTER (SPECIFIED AT STEP 000)

Quantization Error, Inherent (of an ideal ADC)

Within a step, the maximum (positive or negative) possible deviation of the actual analog input value from the nominal midstep value.

NOTE 1: This error follows necessarily from the quantization procedure. For a linear ADC, its value equals $\pm 1/2$ LSB. (See Figure 1.)

NOTE 2: The term "resolution error" for the "inherent quantization error" is deprecated, because "resolution" as a design parameter has only a nominal value.

Rollover Error (of an ADC with decimal output and auto-polarity) (ERO)

The difference in output readings with the analog input switched between positive and negative values of the same magnitude (close to full scale).

Total Error (of a linear ADC) (ET)

The maximum difference (positive or negative) between an analog value and the nominal midstep value within any step. (See Figure 16a.)

NOTE 1: If this error is expressed as a relative value, the term "relative accuracy error" should be used instead of "absolute accuracy error".

NOTE 2: This error includes contributions from offset error, gain error, linearity error, and the inherent quantization error.

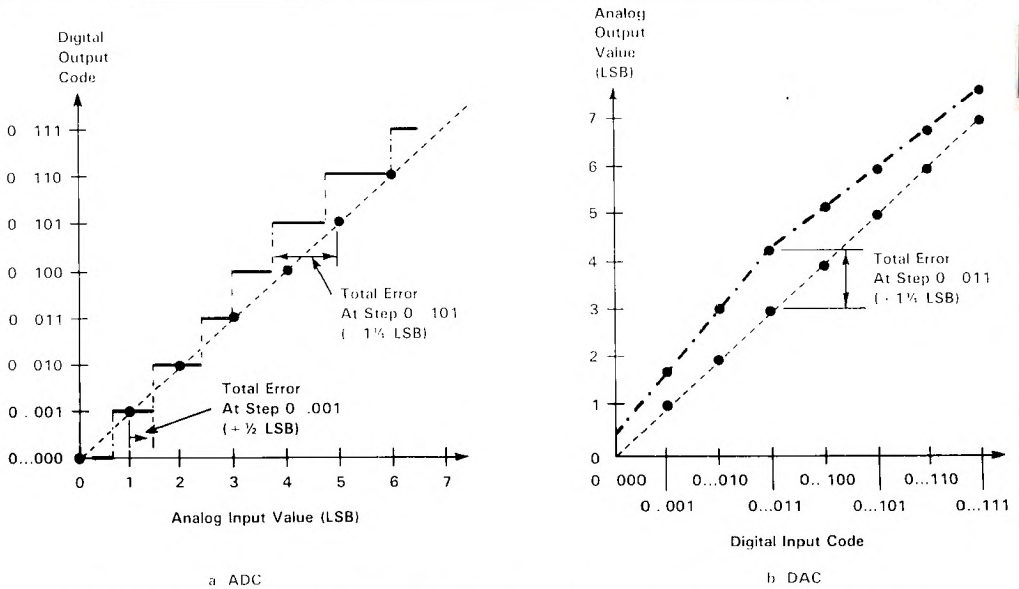


FIGURE 16. ABSOLUTE ACCURACY ERROR, TOTAL ERROR OF A LINEAR ADC OR DAC

Total Error (of a linear DAC) (E_T)

The difference (positive or negative) between the actual step value and the nominal step value for any step. (See Figure 16b.)

NOTE 1: If this error is expressed as a relative value, the term "relative accuracy error" should be used instead of "absolute accuracy error".

NOTE 2: This error includes contributions from offset error, gain error, and linearity error.

Zero-Scale Error (of a linear ADC or DAC) (E_{ZS})

The difference between the actual midstep value or step value and the nominal midstep value or step value, respectively, at specified zero scale

NOTE: Normally, this error specification is applied to converters that have no arrangement for an external adjustment of offset error and gain error.

1 General Information



FIGURE 1-1

FIGURE 1-2

FIGURE 1-3

FIGURE 1-4

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