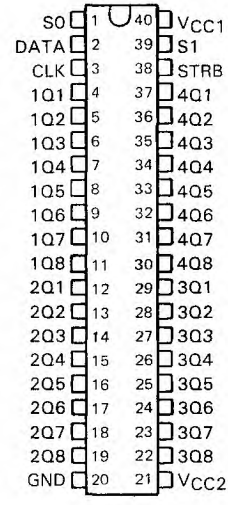
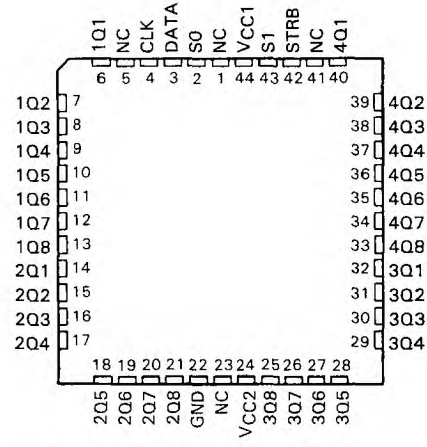
D2471, DECEMBER 1984—REVISED MAY 1990

- Controls 32 Electrodes
- 100-V Totem-Pole Outputs
- Low Stand-by Power Consumption
- All Outputs Contain Sink and Source Clamp Diodes
- 15 mA Steady-State Output Current
- Rugged DMOS Outputs
- CMOS Inputs
- Dependable Texas Instruments Quality and Reliability
- Direct Replacement for SN55500D

JD PACKAGE
(TOP VIEW)



FD PACKAGE
(TOP VIEW)



NC—No internal connection

description

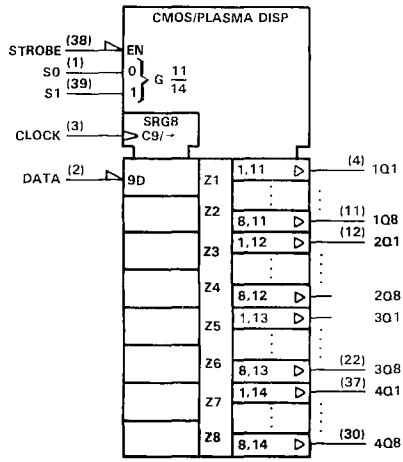
The SN55500E is a monolithic BIDFET† integrated circuit designed to perform the line select operation of a matrix-addressable display. The device inputs are diode-clamped CMOS inputs.

The outputs of the driver are normally low and can be selectively switched high when the strobe input is low. Selection of the outputs is achieved through the data, S0, and S1 inputs. The 8-bit data stored internally in the serial register is inverted and sent to one of four output sections by the 2-line to 4-line decoder. All other outputs remain low. Internal circuits provide a high-current pulse to the level-shifting circuit during positive output transitions. When the output transition is complete, the low steady-state current reduces the circuits standby power consumption. All outputs contain clamp diodes to the V_{CC2} and GND supply inputs.

The SN55500E is characterized for operation over the full military temperature range of −55°C to 125°C.

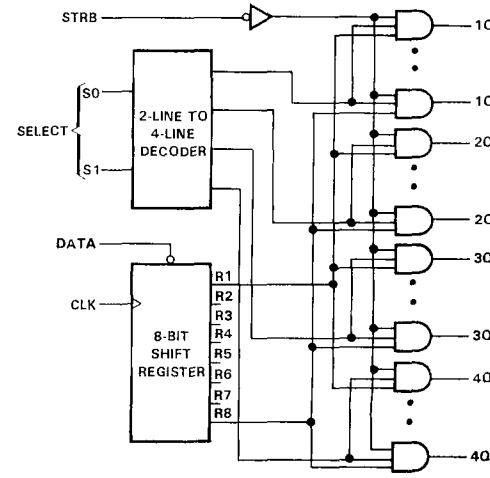
† BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JD package.

functional block diagram (positive logic)

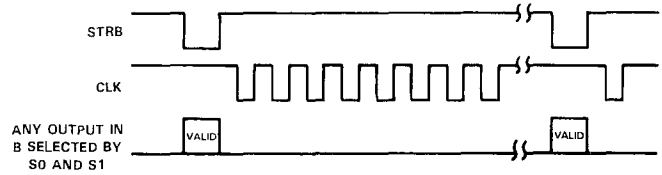


FUNCTION TABLE

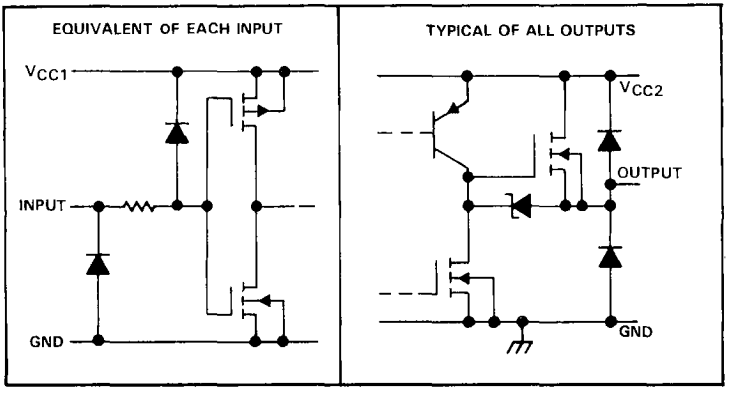
FUNCTION	INPUTS					OUTPUTS						
	DATA	CLK	SELECT		STRB	SHIFT REGISTER			1Q1 ... 1Q8	2Q1 ... 2Q8	3Q1 ... 3Q8	4Q1 ... 4Q8
			S1	S0		R1	R2	R3 ... R8				
LOAD	H	↑	X	X	H	L	$R1_n$	$R2_n$ ... $R7_n$	L ... L	L ... L	L ... L	L ... L
	L	↑	X	X	H	H	$R1_n$	$R2_n$ ... $R7_n$	L ... L	L ... L	L ... L	L ... L
STROBE	X	X	X	X	H	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	L ... L	L ... L	L ... L
	X	H	L	L	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	R1 ... R8	L ... L	L ... L	L ... L
	X	H	L	H	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	R1 ... R8	L ... L	L ... L
	X	H	H	L	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	L ... L	R1 ... R8	L ... L
	X	H	H	H	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	L ... L	L ... L	R1 ... R8

H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
R1 . . . R8 = levels currently at internal outputs of shift registers one through eight, respectively.
$R1_n$ . . . $R8_n$ = levels at outputs R1 through R8 respectively, before the most recent ↑ transition of the clock.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 13.8 V
Supply voltage, V_{CC2} . . . . . 100 V
Input voltage . . . . . V_{CC1} +0.3 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1825 mW
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FD package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JD package . . . . . 300°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, see Dissipation Rating Table.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
FD	1825 mW	14.6 mW/°C	25°C
JD	1825 mW	22 mW/°C	67°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	13.2	V
Supply voltage, V_{CC2}		0		100	V
High-level input voltage, V_{IH}, as a percentage of V_{CC1}		75%			
Low-level input voltage, V_{IL}, as a percentage of V_{CC1}				25%	
High-level output clamp current				20	mA
Low-level output clamp current				−20	mA
Clock frequency, f_{clock} (see Figure 2)		0		8	MHz
Duration of high or low clock pulse, t_w		62			ns
Setup time, t_{su}	Data inputs before clock↑	20			ns
	Select inputs before strobe↓	50			
Hold time, t_h	Data inputs after clock↑ (see Note 3)	50			ns
	Strobe input high after clock↑	50			
	Select inputs after strobe↑	50			
Operating free-air temperature, T_A		−55			°C
Operating case temperature, T_C				125	°C

NOTE 3: For operation above 25°C junction temperature, refer to Figure 2.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

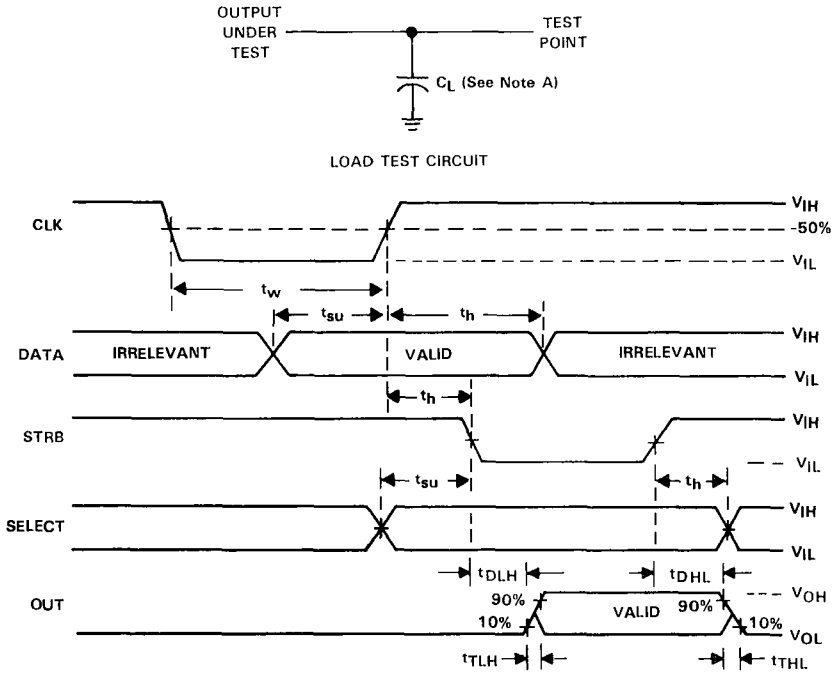
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC1} = 12 V,	I_I = −12 mA		−1	−1.5	V
V_{OH}	High-level output voltage	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	94	97.5		V
			I_{OH} = −10 mA	92	94.5		
			I_{OH} = −15 mA	90	93.5		
V_{OL}	Low-level output voltage	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2	V
			I_{OL} = 10 mA		2	4	
			I_{OL} = 15 mA		2.75	5	
V_{OK}	Output clamp voltage	V_{CC2} = 0	I_O = 20 mA		1	2.5	V
			I_O = −20 mA		−1.2	−2.5	
I_{IH}	High-level input current	V_{CC1} = 13.2 V,	V_I = V_{IH} min			1	μA
I_{IL}	Low-level input current	V_{CC1} = 13.2 V,	V_I = V_{IL} max			−1	μA
I_{CC1}	Supply current	V_{CC1} = 13.2 V,	V_{CC2} = 100 V		0.05	1	mA
I_{CC2}	Supply current	V_{CC2} = 100 V			1	5	mA

† All typical values are at V_{CC} = 12 V, T_A = 25°C.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 100 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 30 pF, See Figure 1		250	ns
t_{DLH}	Delay time, low-to-high-level output from strobe input			450	ns
t_{THL}	Transition time, high-to-low-level output			200	ns
t_{TLH}	Transition time, low-to-high-level output			300	ns

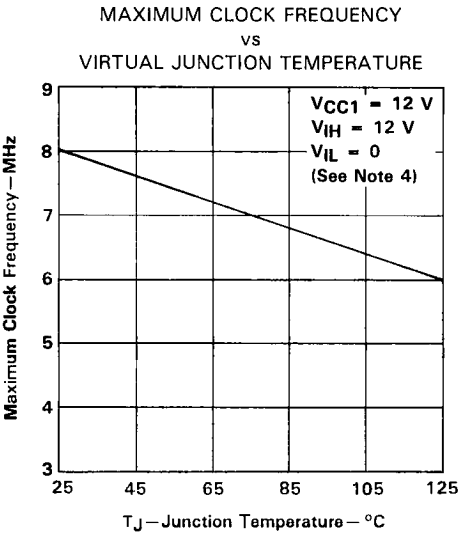
PARAMETER MEASUREMENT INFORMATION



NOTE A. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS



NOTE 4: This curve assumes a symmetrical clock pulse.

FIGURE 2

THERMAL INFORMATION

junction temperature formula

$$T_J = T_A + P_D R_{\theta JA}$$
$$T_J = T_C + P_D R_{\theta JC}$$

where

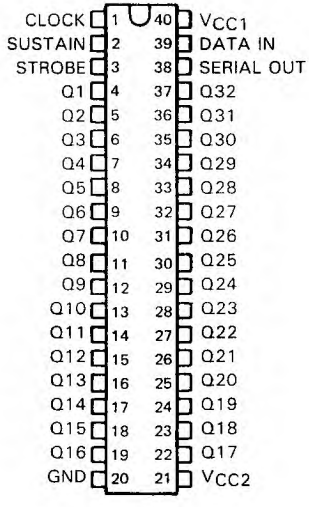
T_J = virtual junction temperature
T_A = free-air temperature
P_D = average device power dissipation
R_θ = thermal resistance (junction-to-air, $R_{\theta JA}$, or junction-to-case, $R_{\theta JC}$)

PACKAGE TYPE	$R_{\theta JA}$	$R_{\theta JC}$
FD 44-pin ceramic	68°C/W	20°C/W
JD 40-pin ceramic	45°C/W	12°C/W

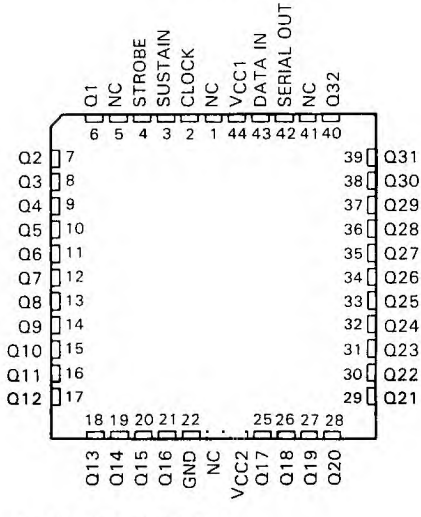
D2472, APRIL 1986—REVISED DECEMBER 1989

- Controls 32 Electrodes
- 100-V Totem-Pole Outputs
- Low Stand-by Power Consumption
- All Outputs Contain Sink and Source Clamp Diodes
- 15-mA Steady-State Output Current
- Rugged DMOS Outputs
- CMOS Inputs
- Direct Replacement for SN55501C, SN55501D

J PACKAGE
(TOP VIEW)



FD OR FJ PACKAGE
(TOP VIEW)



NC—No internal connection

description

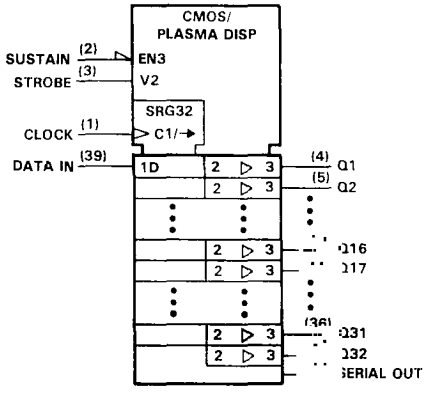
The SN55501E is a monolithic BIDFET† integrated circuit designed to provide the serial-to-parallel conversion and level translation of data in a matrix-addressable display. This device has diode-clamped CMOS inputs.

The Q outputs of these drivers are normally high and can be switched either selectively or together. Any output whose associated register bit (in the internal 32-bit serial register) contains a low will switch low when STROBE is low if SUSTAIN is high. All other outputs remain high. When SUSTAIN is switched low, all outputs switch low independently of the data or strobe inputs. This feature can be used to generate a portion of the SUSTAIN pulse required in the operation of an ac plasma display. The internal level-shift circuits provide additional drive during the times that the outputs switch high to facilitate fast rise times while maintaining low stand-by power consumption. All outputs contain clamp diodes to the V_{CC2} and GND supply inputs.

The SN55501E is characterized for operation over the full military temperature range of −55°C to 125°C.

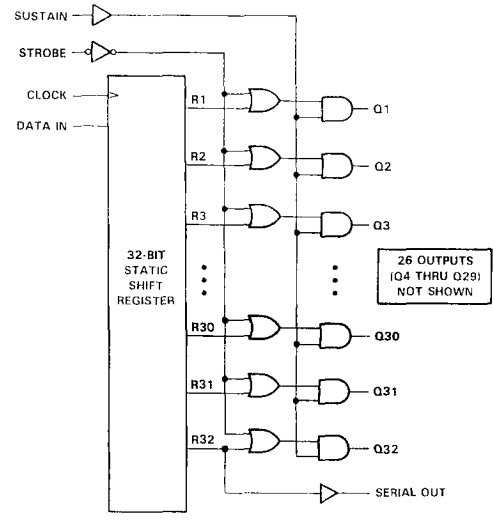
†BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J package.

functional block diagram (positive logic)

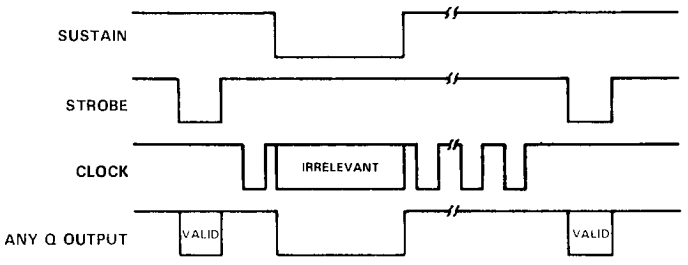


FUNCTION TABLE

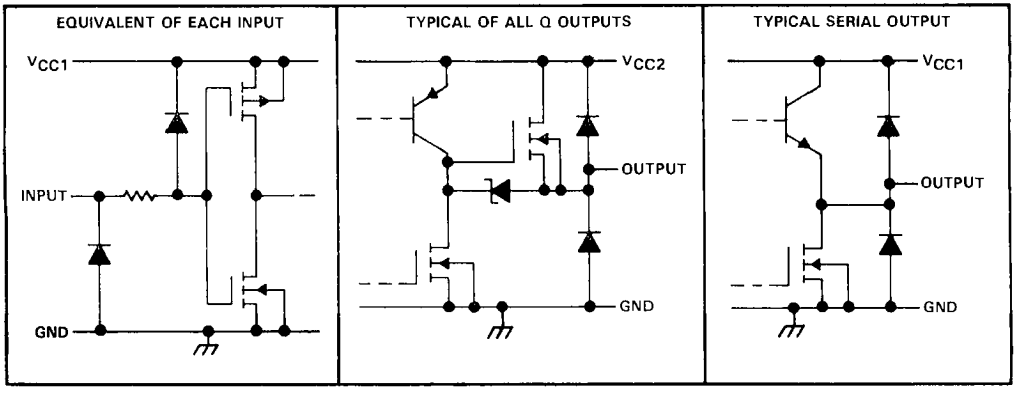
FUNCTION	INPUTS				OUTPUTS						
	DATA	CLOCK	STROBE	SUSTAIN	SHIFT REGISTER R1	SHIFT REGISTER R2	SHIFT REGISTER R3.. R32	SERIAL DATA	Q1	Q2	Q3....Q32
LOAD	H	↑	H	H	H	$R1_n$	$R2_n$..	$R32_n$	H	H	H....H
	L	↑	H	H	L	$R1_n$	$R2_n$...$R31_n$	$R32_n$	H	H	H....H
STROBE	X	X	H	H	$R1_n$	$R2_n$	$R3_n$...$R32_n$	$R32_n$	H	H	H....H
	X	H	L	H	$R1_n$	$R2_n$	$R3_n$...$R32_n$	$R32_n$	R1	R2	R3....R32
SUSTAIN	X	X	X	L	$R1_n$	$R2_n$	$R3_n$...$R32_n$	$R32_n$	L	L	L....L

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
R1...R32 = levels currently at internal outputs of shift registers one through thirty-two, respectively.
$R1_n$...$R32_n$ = levels at shift-register outputs R1 through R32 respectively, before the most recent ↑ transition at the CLOCK input.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 100 V
Input voltage . . . . . V_{CC1} + 0.3 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FD or FJ package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 125°C$ POWER RATING
FD or FJ	1825 mW	14.6 mW/°C	25°C	365 mW
J	1825 mW	22.0 mW/°C	67°C	550 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	13.2	V
Supply voltage, V_{CC2}		0		100	V
High-level input voltage, V_{IH}		0.75 V_{CC1}			
Low-level input voltage, V_{IL}				0.25 V_{CC1}	
Peak high-level Q output current, I_{OH}				−20	mA
Peak low-level Q output current, I_{OL}				20	mA
High-level Q output clamp current, I_{OKH}				20	mA
Low-level Q output clamp current, I_{OKL}				−20	mA
Clock frequency, f_{clock}, at or below, 25°C junction temperature (see Note 2)		0		8	MHz
Duration of high or low clock pulse, t_w		62			ns
Setup time, t_{su}	Data inputs before CLOCK↑	20			ns
Hold time, t_h	Data hold time after CLOCK↑	50			ns
	STROBE high after CLOCK↑	150			
	S̄ high after SUSTAIN↑	250			
Operating free-air temperature, T_A		−55		125	°C
Operating case temperature, T_C				125	

NOTE 2: See Figure 3 for maximum clock frequency when devices are operated in cascade or for operation above T_J = 25°C.

electrical characteristics over recommended operating temperature range

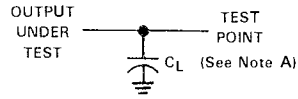
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC1} = 12 V,	I_I = 12 mA		−1	−1.5	V
V_{OH}	High-level output voltage	Q outputs	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	94	97.5		V
				I_{OH} = −10 mA	92	94.5		
				I_{OH} = −15 mA	90	93.5		
		SERIAL OUT	V_{CC1} = 10.8 V,	I_{OH} = −100 μA	9	10		
V_{OL}	Low-level output voltage	Q outputs	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2	V
				I_{OL} = 10 mA		2	4	
				I_{OL} = 15 mA		2.75	5	
		SERIAL OUT	V_{CC1} = 10.8 V,	I_{OL} = 100 μA		0.1	1	
V_{OK}	Output clamp voltage	Q outputs	V_{CC2} = 0	I_{OK} = 20 mA		1	2.5	V
				I_{OK} = −20 mA		−1.2	−2.5	
I_{IH}	High-level input current		V_{CC1} = 13.2 V, V_{CC2} = 100 V	V_{IH} = V_{IH}min,			1	μA
I_{IL}	Low-level input current		V_{CC1} = 13.2 V, V_{CC2} = 100 V	V_{IL} = V_{IL}max,			−1	μA
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 13.2 V,	V_{CC2} = 100 V‡		0.05	1	mA
I_{CC2}	Supply current from V_{CC2}		V_{CC1} = 13.2 V, V_{CC2} = 100 V	Outputs low		0.1	1	mA
				Outputs high		1	5	

†Typical values are at V_{CC1} = 12 V, T_A = 25°C.
‡Measure with inputs at V_{CC1} and again with inputs at GND.

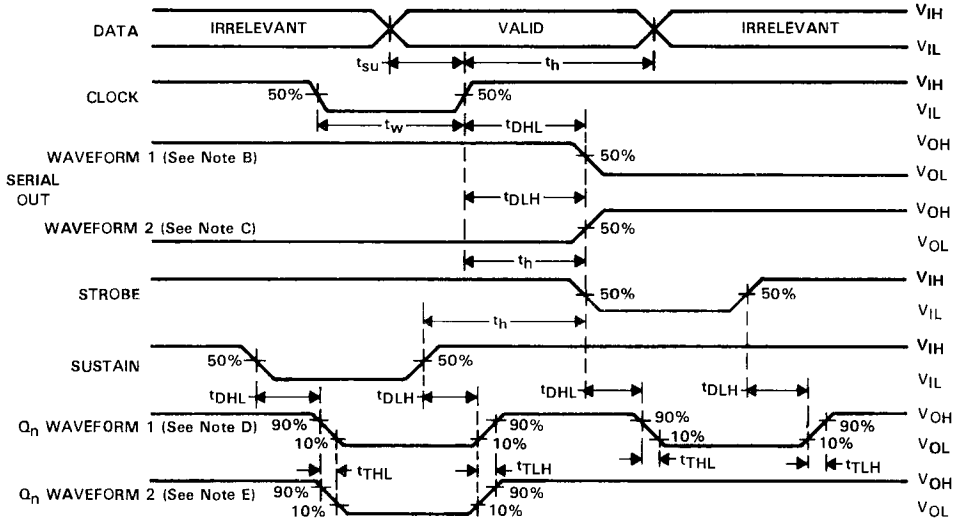
switching characteristics, V_{CC1} = 12 V, V_{CC2} = 100 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level outputs	STROBE to Q outputs	C_L = 30 pF			250	ns
		SUSTAIN to Q outputs	C_L = 30 pF			250	
		CLOCK to SERIAL OUT	C_L = 20 pF			147	
t_{DLH}	Delay time, low-to-high-level outputs	STROBE to Q outputs	C_L = 30 pF			450	ns
		SUSTAIN to Q outputs	C_L = 30 pF			450	
		CLOCK to SERIAL OUT	C_L = 20 pF			147	
t_{THL}	Transition time, high-to-low-level Q output		C_L = 30 pF			200	ns
t_{TLH}	Transition time, low-to-high-level Q output		C_L = 30 pF			300	ns

PARAMETER MEASUREMENT INFORMATION



LOAD TEST CIRCUIT



NOTES: A. C_L includes probe and jig capacitance.
B. Serial out waveform for internal conditions such that a low is registered in R32.
C. Serial out waveform for internal conditions such that a high is registered in R32.
D. Q_n output with a low stored in associated register R_n.
E. Q_n output with a high stored in associated register R_n.

VOLTAGE WAVEFORMS

FIGURE 1. SWITCHING CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS

MAXIMUM CLOCK FREQUENCY
vs
JUNCTION TEMPERATURE

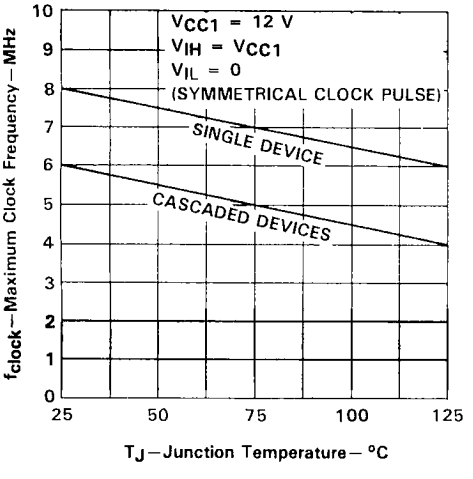


FIGURE 2

INPUT VOLTAGE LOGIC LEVEL LIMITS
vs
V_{CC1} SUPPLY VOLTAGE

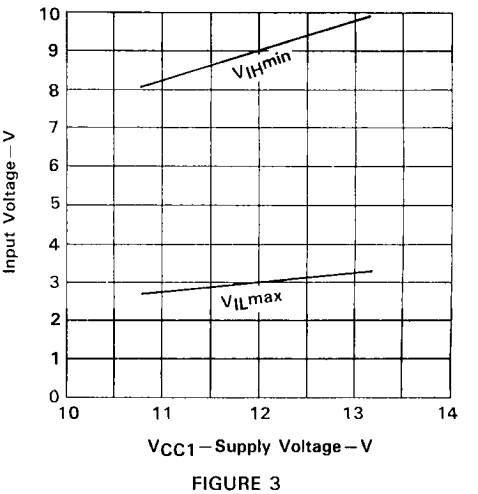


FIGURE 3

THERMAL CHARACTERISTICS

junction temperature formula

$$T_J = T_A + P_D R_\theta$$

where

T_J = virtual junction temperature
T_A = free-air temperature
P_D = average device power dissipation
R_θ = thermal resistance (junction-to-air, $R_{\theta JA}$, or junction-to-case, $R_{\theta JC}$)

PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$
FD or FJ	68°C/W	20°C/W
J	45°C/W	12°C/W

D2743, APRIL 1986

- Each Device Drives 32 Electrodes
- High-Voltage Open-Drain DMOS Outputs
- 50-mA Output Current Capability
- CMOS-Compatible Inputs
- Very Low Steady-State Power Consumption

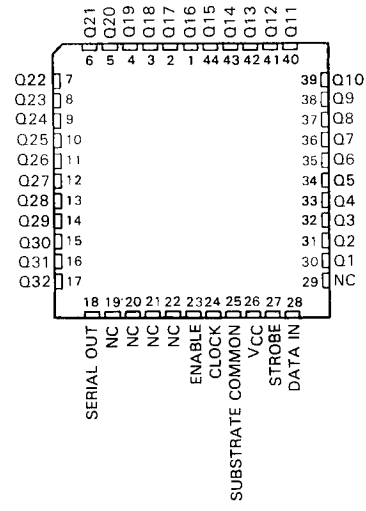
description

The SN55551 and SN55552 are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS-compatible and all outputs are high-voltage open-drain DMOS transistors. The SN55552 output sequence has been reversed from the SN55551 for ease in printed circuit board layout.

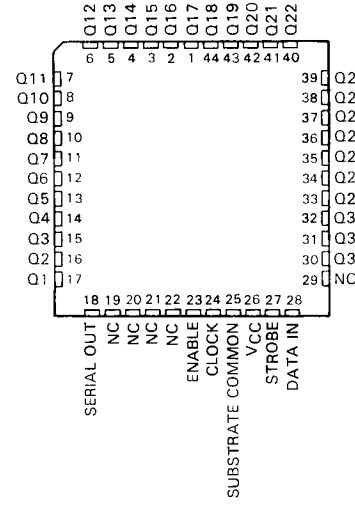
The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to the Substrate Common terminal. Serial data is entered into the shift register on the high-to-low transition of the clock input. A high Enable input allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When the Strobe input is low, all output transistors are turned on. The Serial Data output from the shift register may be used to cascade additional devices. This output is not affected by the Enable or Strobe inputs.

The SN55551 and SN55552 are characterized for operation over the full military temperature range of −55°C to 125°C.

SN55551 . . . FD PACKAGE
(TOP VIEW)



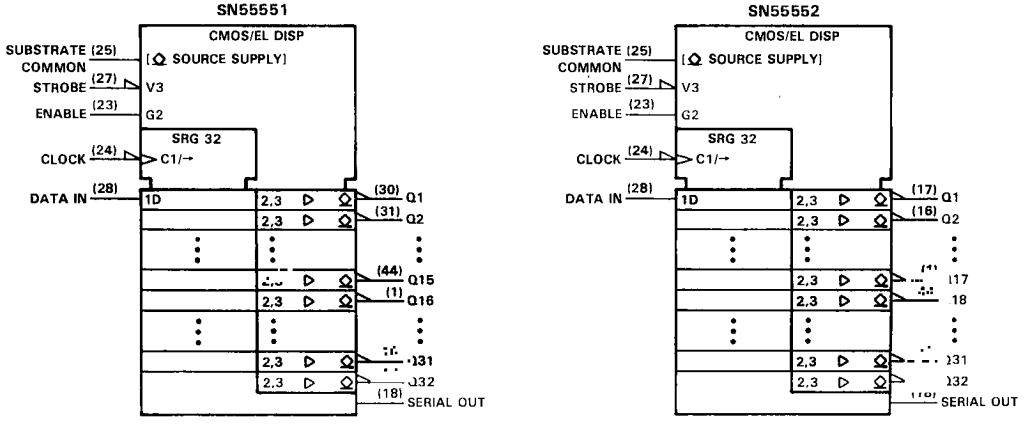
SN55552 . . . FD PACKAGE
(TOP VIEW)



NC—No internal connection

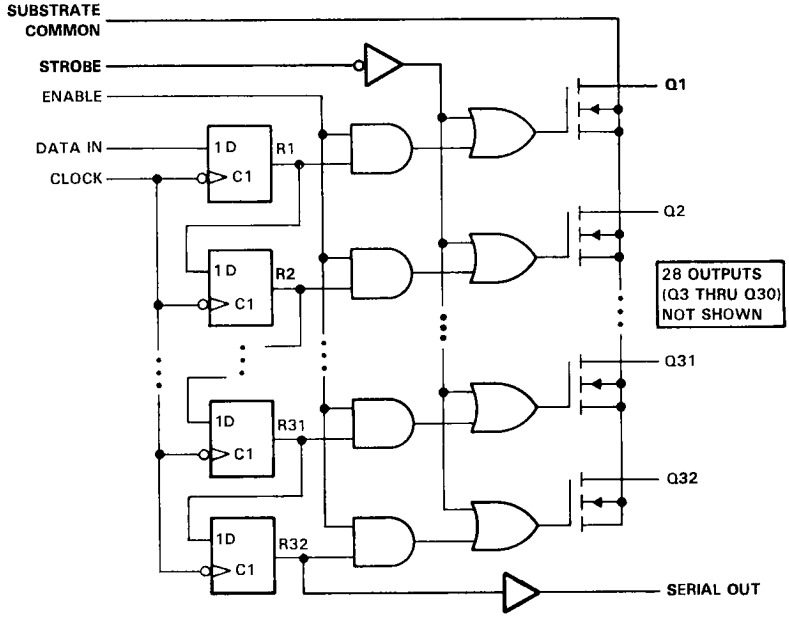
† BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. The symbol ◇ here indicates an n-channel open-drain output.

logic diagram (positive logic)

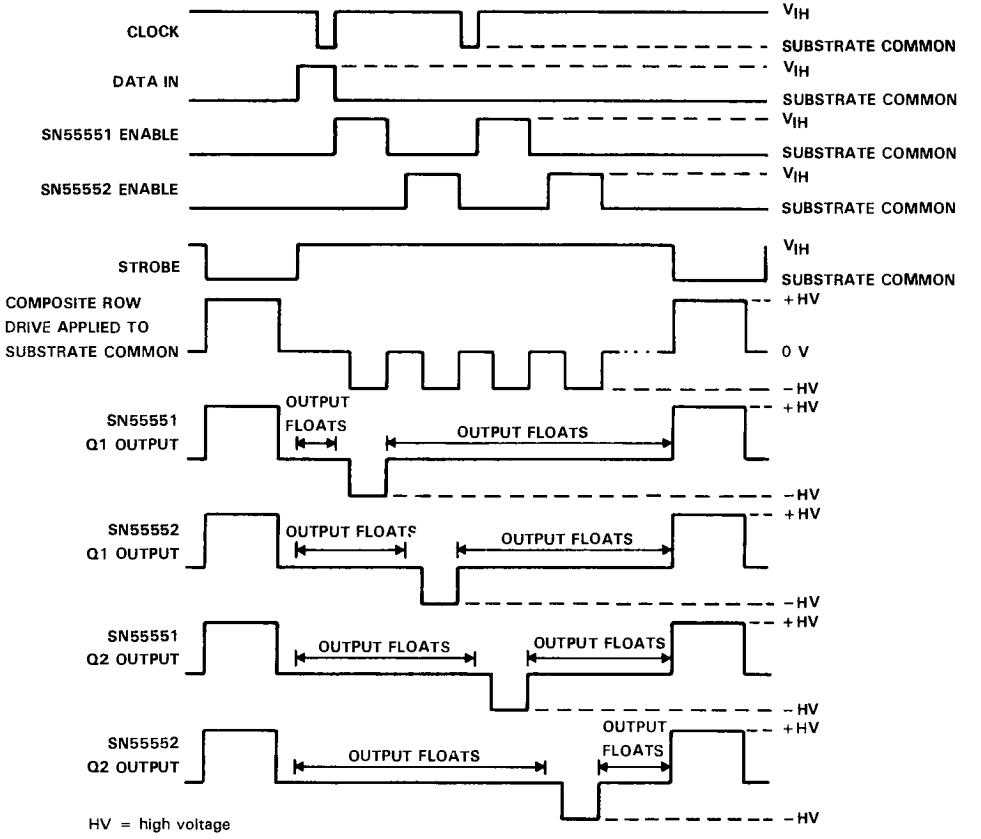


FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R32	OUTPUTS	
	CLOCK	ENABLE	STROBE		SERIAL	Q1 THRU Q32
LOAD	↓	X	X	Load and Shift†	R32	Determined by Enable and Strobe
	No. ↓	X	X	No Change	R32	Determined by Enable and Strobe
ENABLE	X	L	H	As determined above	R32	All Q outputs off
	X	H	H	As determined above	R32	Determined by R1 through R32
STROBE	X	X	L	As determined above	R32	All Q outputs on

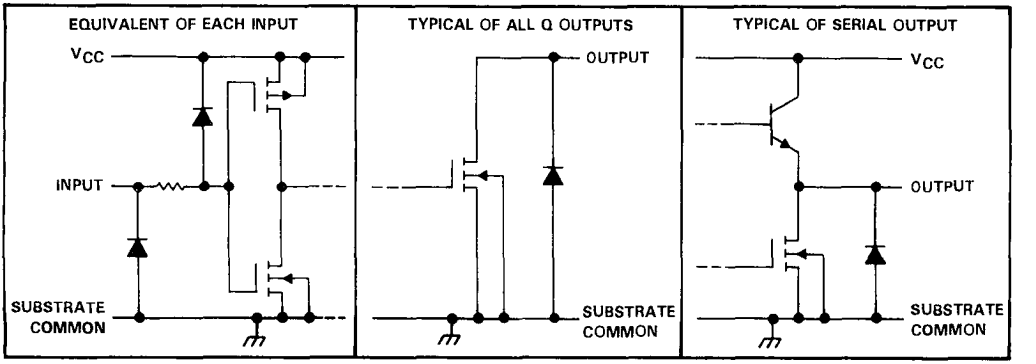
H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition.
†Register R32 takes on the state of R31, R31 takes on the state of R30,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



NOTE: During operation Clock, Data In, Enable, and Strobe are referenced to the Composite Row Drive signal received at the Substrate Common pin of the device.

schematic of inputs and outputs



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Q off-state output voltage, $V_{O(off)}$ . . . . . 225 V
Input voltage . . . . . $V_{CC}+0.3$ V
Substrate common terminal current (see Note 2) . . . . . 1.5 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 1825 mW
Minimum operating free-air temperature . . . . . −55°C
Operating case temperature . . . . . 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to substrate common terminal.
2. Duty cycle is limited by package dissipation.
3. For operation above 25°C free-air temperature, derate linearly at the rate of 14.6 mW/°C.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			10.8	12	15	V
$V_{O(off)}$	Off-state Q output voltage			0		200	V
V_{IH}	High-level input voltage			0.75V_{CC}		$V_{CC}+0.3$	V
V_{IL}	Low-level input voltage			−0.3		0.25V_{CC}	V
$I_{O(on)}$	On-state Q output current	V_{DD} = 80 V, Duty cycle ≤ 1%	V_{CC} = 10.8 V, T_C = 25°C			50	mA
			V_{CC} = 15 V, T_C = 25°C			80	
f_{clock}	Clock frequency, T_A = 25°C					6.25	MHz
t_w	Clock pulse duration, high or low, T_A = 25°C			80			ns
t_{su}	Setup time, data valid before clock↓, T_A = 25°C			20			ns
t_h	Hold time, data valid after clock↓, T_A = 25°C			110			ns
T_A	Operating free-air temperature			−55			°C
T_C	Operating case temperature					125	°C

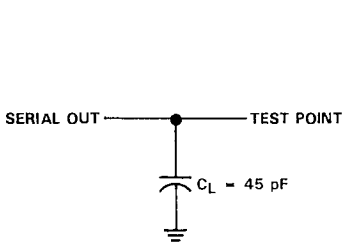
electrical characteristics over recommended operating temperature range, V_{CC} = 12 V, substrate common at 0 V

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Serial outputs	I_O = - μA			V
V_{OL}	Low-level output voltage	Q outputs	I_O = 50 mA		50	V
		Serial output	I_O = 100 μA		1.5	
I_{IH}	High-level input current		V_I = 12 V		5	μA
I_{IL}	Low-level input current		V_I = 0		−5	μA
$I_{O(off)}$	Off-state Q output current		V_O = 200 V		50	μA
I_{CC}	Supply current				500	μA

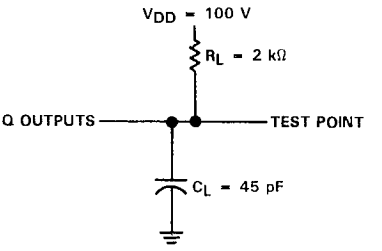
switching characteristics, V_{CC} = 12 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{dLH}	Delay time, clock↓ to serial↓	C_L = 45 pF to common, See Figure 1		200	ns
t_{dHL}	Delay time, clock↓ to serial↑			200	ns
t_{dHL}	Delay time, enable to Q output↓	V_{DD} = 100 V, R_L = 2 kΩ, C_L = 45 pF to common, See Figure 1		500	ns

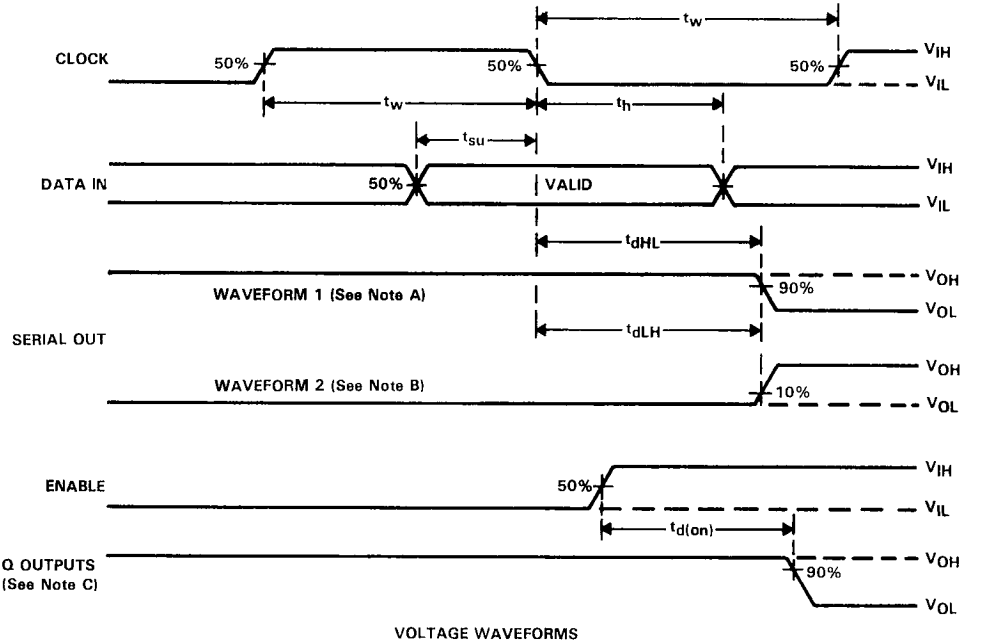
PARAMETER MEASUREMENT INFORMATION



SERIAL OUTPUT LOAD CIRCUIT



Q OUTPUT LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Waveform 1 is for internal conditions such that a low is clocked into R32.
B. Waveform 2 is for internal conditions such that a high is clocked into R32.
C. To measure $t_{d(on)}$, a high is stored in the associated register.

FIGURE 1. SWITCHING CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS

MAXIMUM ON-STATE Q OUTPUT CURRENT
vs
SUPPLY VOLTAGE

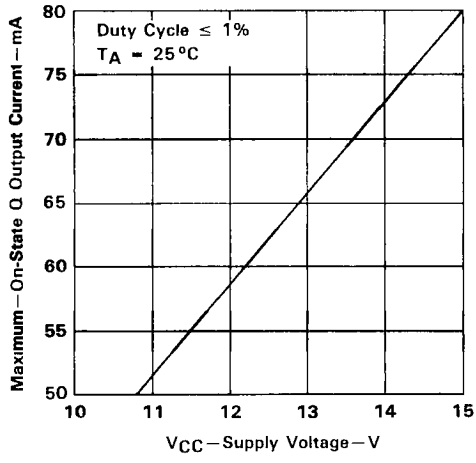


FIGURE 2

TYPICAL CHARACTERISTICS

OUTPUT CHARACTERISTICS SHOWING
SAFE OPERATION AREA (SOA)

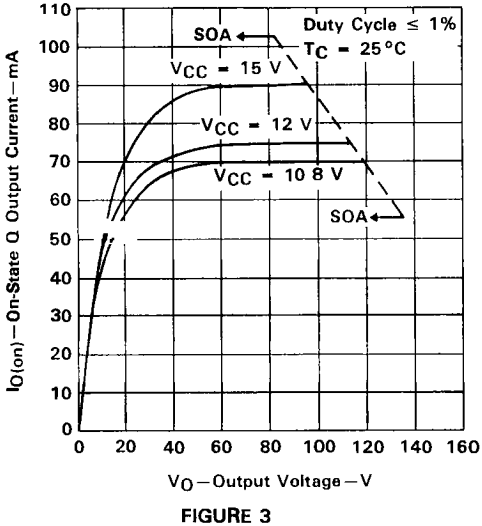


FIGURE 3

OUTPUT SATURATION CURRENT
vs
JUNCTION TEMPERATURE

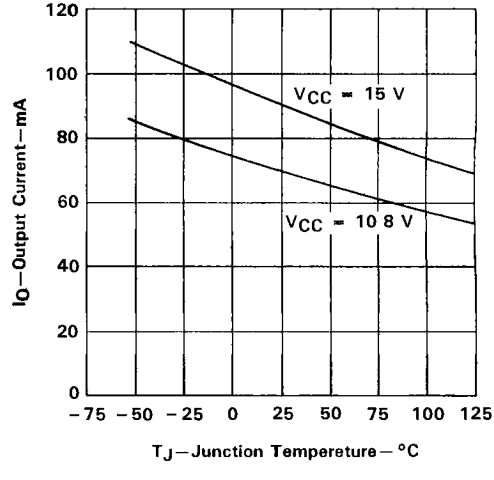


FIGURE 4

D2744, APRIL 1986

- Each Device Drives 32 Electrodes
- 60-V Output Voltage Swing Capability
- 15-mA Output Source and Sink Current Capability
- High-Speed Serially-Shifted Data Input
- Totem-Pole Outputs
- Latches on All Driver Outputs

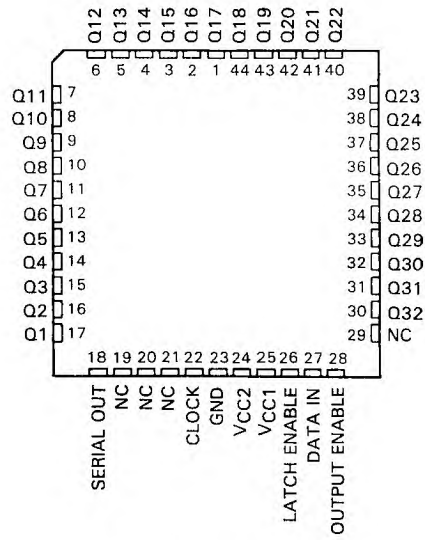
description

The SN55553 and SN55554 are monolithic BIDFET† integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN55554 output sequence has been reversed from the SN55553 for ease in printed circuit board layout.

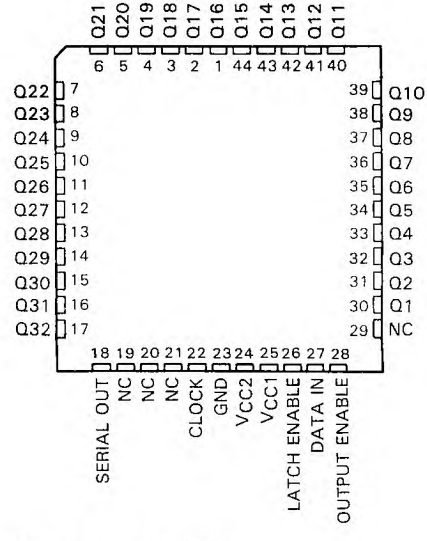
The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of the clock input. When high, the Latch Enable input transfers the shift register contents to the outputs of the 32 latches. When Output Enable is high, all Q outputs are enabled. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the Latch Enable or Output Enable inputs.

The SN55553 and SN55554 are characterized for operation over the full military temperature range of −55°C to 125°C.

SN55553 . . . FD PACKAGE
(TOP VIEW)



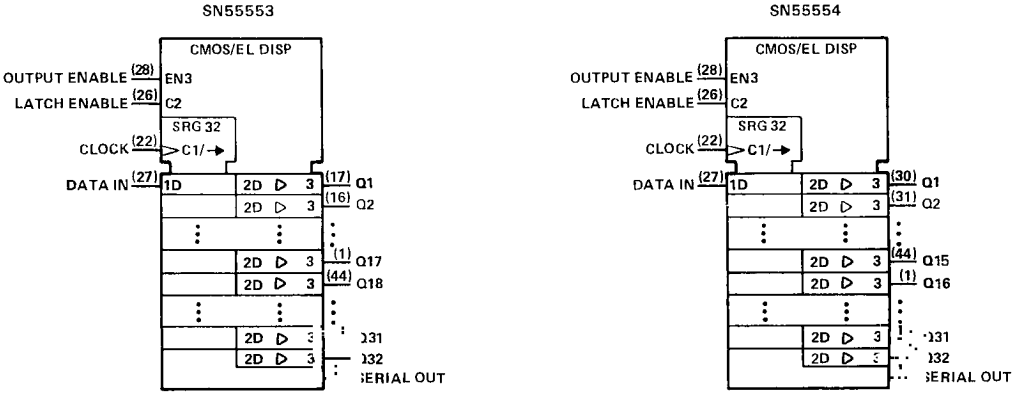
SN55554 . . . FD PACKAGE
(TOP VIEW)



NC—No internal connection

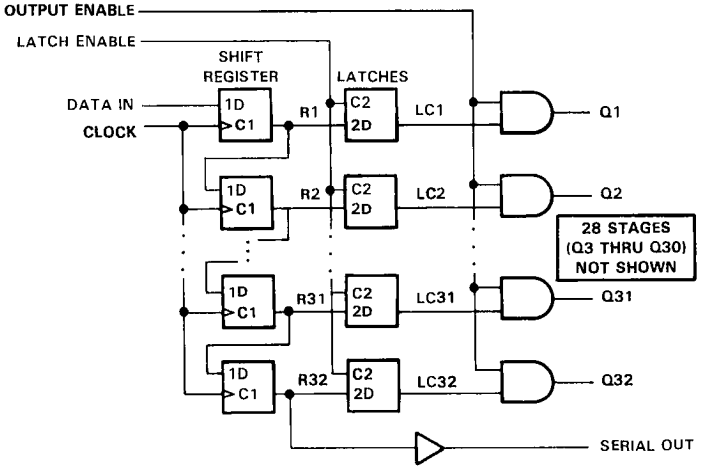
†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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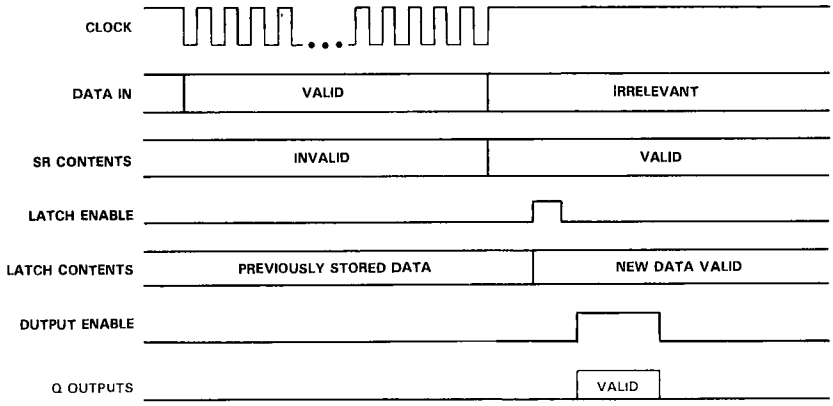
FUNCTION TABLE

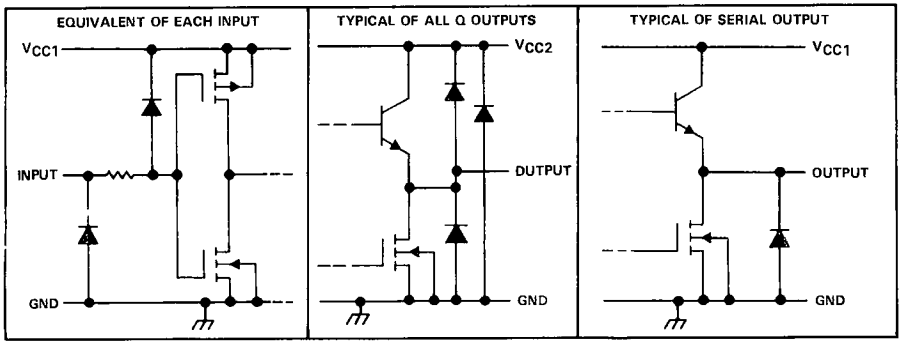
FUNCTION	CONTROL INPUTS			SHIFT REGISTER	LATCHES	OUTPUTS	
	CLOCK	LATCH ENABLE	OUTPUT ENABLE	R1 THRU R32	LC1 THRU LC32	SERIAL	Q1 THRU Q32
LOAD	↑	X	X	Load and shift†	Determined by	R32	Determined by
	No↑	X	X	No change	Latch Enable‡	R32	Output Enable
LATCH	X	L	X	As determined above	Stored data	R32	Determined by
	X	H	X	As determined above	New data	R32	Output Enable
OUTPUT ENABLE	X	X	L	As determined above	Determined by	R32	All L
	X	X	H	As determined above	Latch Enable‡	R32	LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
†R32 and the serial output take on the state of R31, R31 takes on the state of R30,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.
‡New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.

typical operating sequence



schematic of inputs and outputs



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC2} . . . . . 70 V
Input voltage . . . . . V_{CC1} + 0.3 V
Ground current . . . . . 700 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1825 mW
Minimum operating free-air temperature . . . . . −55°C
Operating case temperature . . . . . 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 14.6 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage	10.8	12	13.2	V
V_{CC2}	Supply voltage	0		60	V
V_{IH}	High-level input voltage	0.75V_{CC}		V_{CC}+0.3	V
V_{IL}	Low-level input voltage	−0.3		0.25V_{CC}	
I_{OH}	High-level output current	−15			mA
I_{OL}	Low-level output current	15			mA
I_{OK}	Peak output clamp diode current			±20	mA
f_{clock}	Clock frequency, T_A = 25°C			6.25	MHz
$t_{w(CLK)}$	Clock pulse duration, high or low, T_A = 25°C	80			ns
$t_{w(LE)}$	Latch enable pulse duration, T_A = 25°C	80			
t_{su}	Setup time, data valid before clock↑, T_A = 25°C	20			ns
t_h	Hold time, data valid after clock ↑, T_A = 25°C	110			ns
T_A	Operating free-air temperature	−55			
T_C	Operating case temperature			125	

electrical characteristics over recommended operating temperature range, V_{CC1} = 12 V, V_{CC2} = 60 V

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = −15 mA	55		V
		Serial output	I_O = −100 μA	10		
V_{OL}	Low-level output voltage	Q outputs	I_O = 15 mA		10	V
		Serial output	I_O = [illegible] μA		1.5	
I_{IH}	High-level input current (see Note 3)		V_I = 12 V		5	μA
I_{IL}	Low-level input current (see Note 3)		V_I = 0		−5	μA
I_{CC1}	Supply current, V_{CC1}				7	mA
I_{CC2}	Supply current, V_{CC2}		Outputs high		20	mA
			Outputs low		2	

NOTE 3: I_{IH} and I_{IL} parameter performances are independent of V_{CC2} and need not be 60 V for this test.

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switching characteristics, V_{CC1} = 12 V, V_{CC2} = 60 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{dLH}	Delay time, clock↑ to serial↑	C_L = 45 pF to ground, See Figures 1 and 2		200	ns
t_{dHL}	Delay time, clock↑ to serial↓			200	ns
t_{dLH}	Delay time, LE to Q output↑	C_L = 45 pF to ground, See Figures 1 and 3		1000	ns
t_{dHL}	Delay time, LE to Q output↓			500	ns

PARAMETER MEASUREMENT INFORMATION

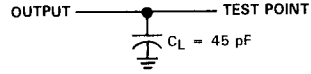


FIGURE 1. OUTPUT LOAD CIRCUIT

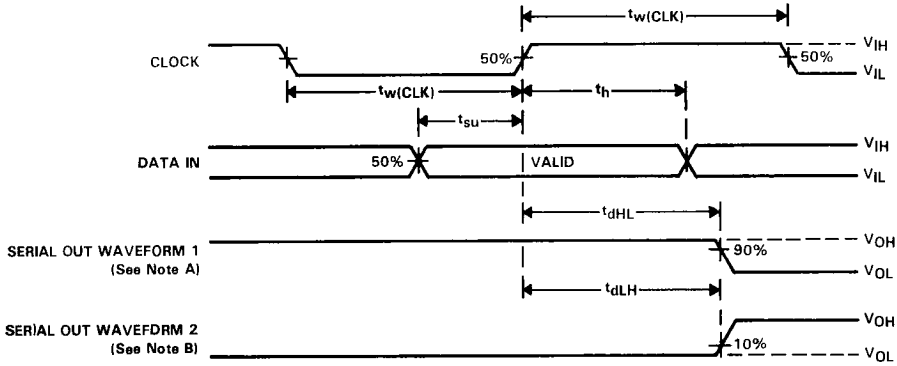


FIGURE 2. VOLTAGE WAVEFORMS FOR SERIAL OUTPUT

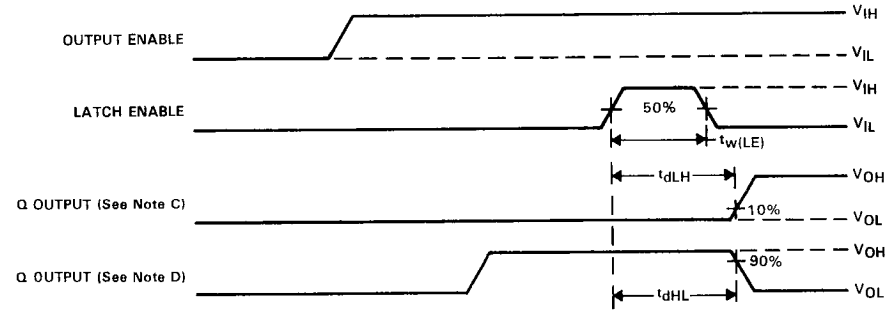


FIGURE 3. VOLTAGE WAVEFORMS FOR Q OUTPUTS

NOTES: A. Waveform 1 is for internal conditions such that a low is clocked into R32.
B. Waveform 2 is for internal conditions such that a high is clocked into R32.
C. To measure t_{dLH}, initially a low is stored in the latch and a high is stored in the shift register.
D. To measure t_{dHL}, initially a high is stored in the latch and a low is stored in the shift register.

D3313, OCTOBER 1989

- Each Device Drives 34 Electrodes
- Selectable Open-Source or Open-Drain Output
- Outputs Rated at 225 V
- Output Current Capability: −90 mA to 150 mA
- CMOS-Compatible Inputs
- Very Low Steady-State Power Consumption

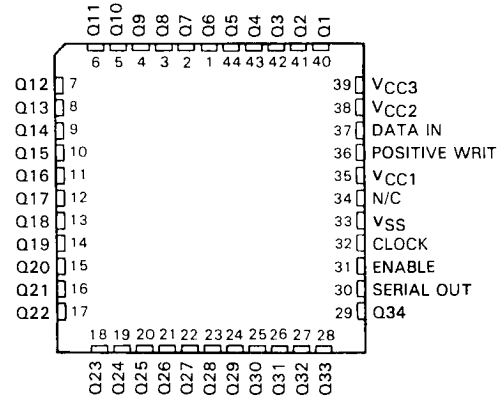
description

The SN55563A and SN55564A are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS compatible. If the Positive Write input is high, the Q outputs act like open-source outputs and output data is not inverted with respect to input data. If the Positive Write input is low, the Q outputs act like open-drain outputs and output data is inverted with respect to input data. The SN55564A output sequence has been reversed from the SN55563A for ease in printed circuit board layout.

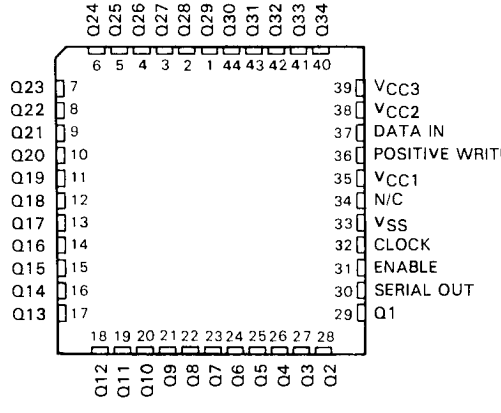
Typically, composite V_{CC2}, V_{CC3}, and V_{SS} signals are externally generated by a high-voltage switching circuit. Serial data is entered into the shift register on the high-to-low transition of the clock input. A high Enable input allows those outputs with a high in their associated register to be turned on, causing the corresponding row to be connected to V_{CC2} when Positive Write is high or to V_{SS} when Positive Write is low. V_{CC3} may be tied to V_{CC2} or held 5 to 15 V above V_{CC2} for better V_{OH} characteristics. The Serial Output from the shift register may be used to cascade additional devices. This output is not affected by the Enable or Positive Write inputs.

The SN55563A and SN55564A are characterized for operation over the full military operating temperature range of −55°C to 125°C.

SN55563A . . . FJ PACKAGE
(TOP VIEW)



SN55564A . . . FJ PACKAGE
(TOP VIEW)



NC—No internal connection

†BIDFET-Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip — Patented Process

LOAD FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTER	OUTPUTS	
	CLOCK	ENABLE	POSITIVE WRITE	R1 THRU R34	SERIAL	Q1 THRU Q34
LOAD	↓	X	X	Load and Shift†	R34	Determined by Enable and Positive Write
	No↓	X	X	No Change	R34	Determined by Enable and Positive Write

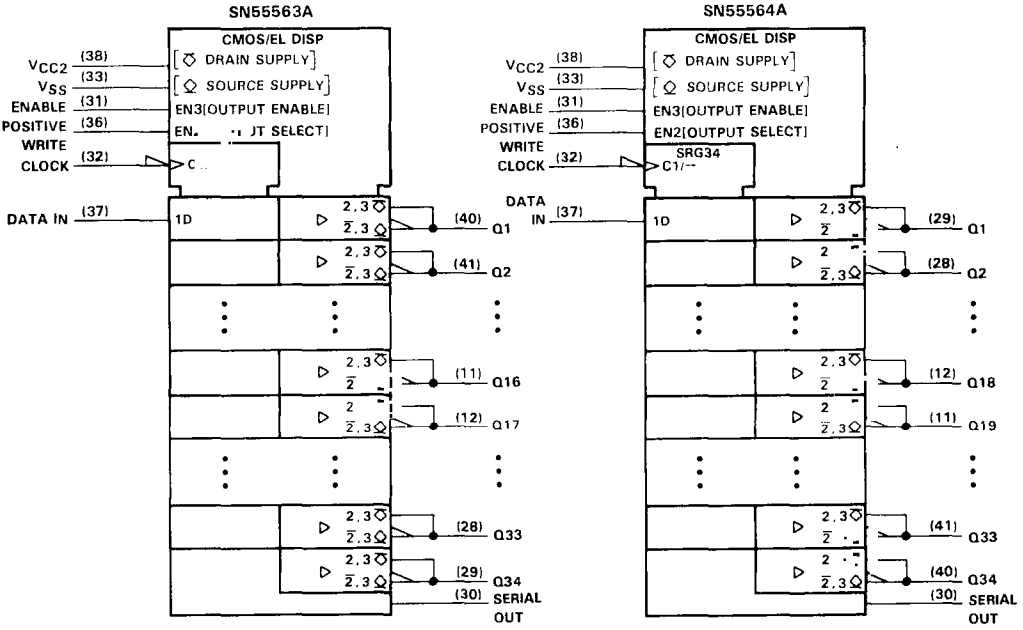
†Register R34 takes on the state of R33, R33 takes on the state of R32, . . . R2 takes on the state of R1, R1 takes on the state of the data input.

OUTPUT CONTROL FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTER CONTENTS Rn FOR R1 THRU R34 (Determined Above)	OUTPUTS	
	CLOCK	ENABLE	POSITIVE WRITE		SERIAL	Q1 THRU Q34
OUTPUT CONTROL	X	L	X	X	R34	High-Impedance
	X	H	H	H	R34	H
	X	H	L	H	R34	L
	X	X	X	L	R34	High-Impedance

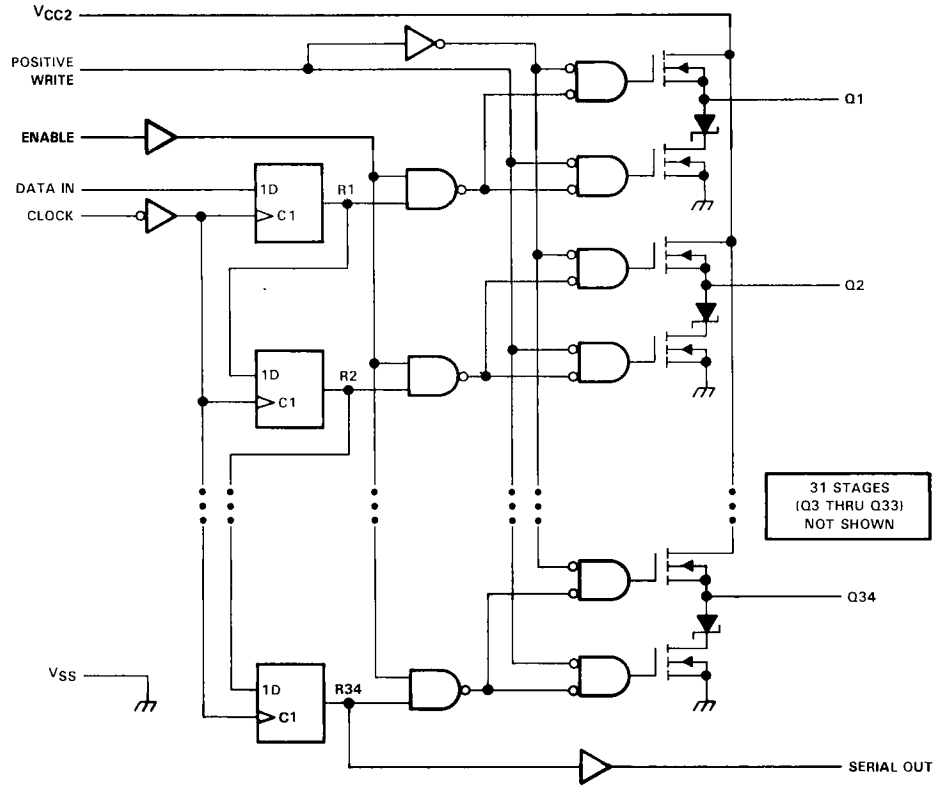
H = high, L = low, X = irrelevant, ↓ = high-to-low transition

logic symbols‡

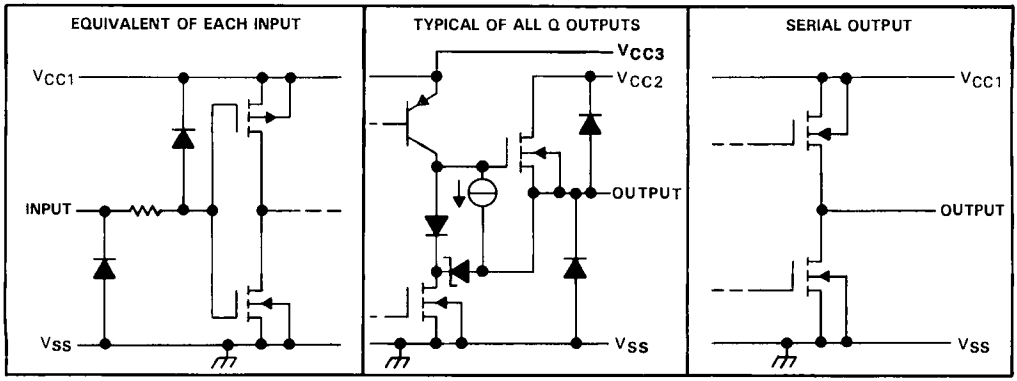


‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

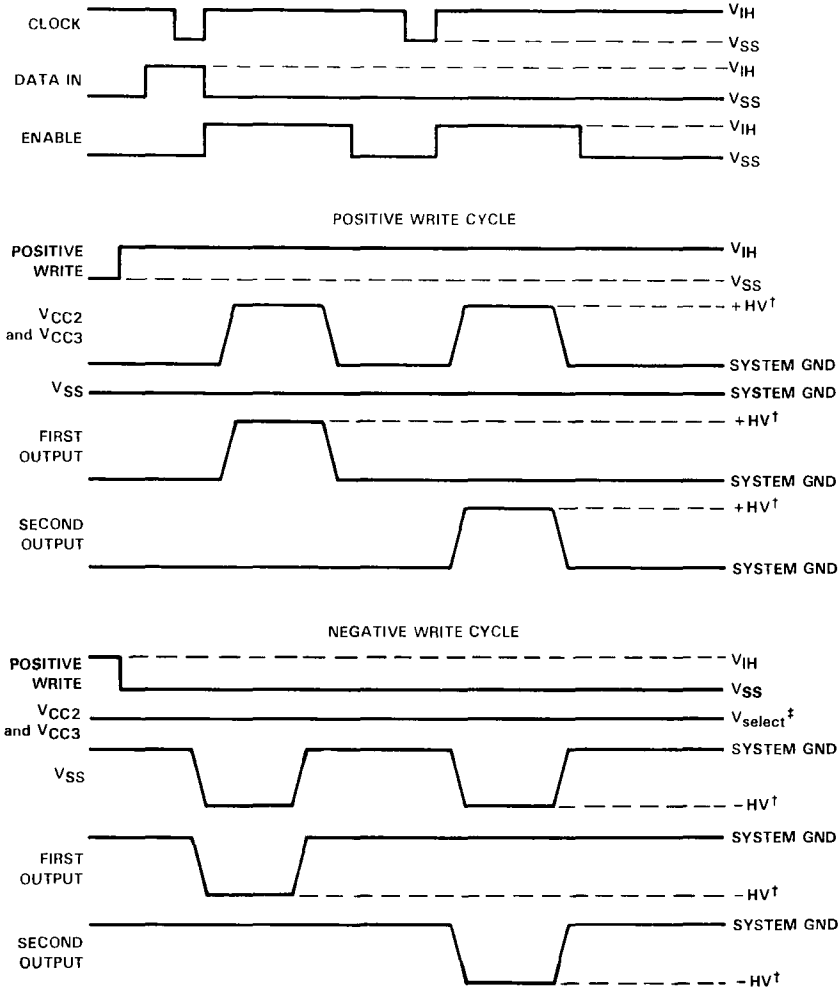
logic diagram (positive logic)



schematics of inputs and outputs



typical operating sequence



†HV = high voltage
‡V_{select} is a voltage level between V_{CC2} of the column driver and V_{SS}.

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absolute maximum ratings over operating free-air temperture range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 230 V
Supply voltage, V_{CC3} . . . . . 230 V
Supply voltage, V_{SS} . . . . . −230 V
Input voltage . . . . . −0.3 V to V_{CC1} + 0.3 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1825 mW
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to V_{SS}.
2. For operation above 25°C free-air temperature, derate 365 mW at 125°C at the rate of 14.6 mW/°C.

recommended operating conditions (see Figure 1 and Figure 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	10.8	12	13.2	V
Supply voltage, V_{CC2}	$V_{CC3}-15$		V_{CC3}	V
Supply voltage, V_{CC3}	0			V
Supply voltage, V_{SS}	0		- .	V
High-level input voltage, V_{IH}	$0.75V_{CC1}$		$V_{CC1}+0.3$	V
Low-level input voltage, V_{IL}†	−0.3		$0.25V_{CC1}$	V
High-level output current, I_{OH}			−90	mA
Low-level output current, I_{OL}			150	mA
Output clamp current, I_{OK}			±150	mA
Clock frequency, f_{clock}			1	MHz
Pulse duration, Clock high or low, t_{wCLK}	125			ns
Setup time, data high or low before clock↓, t_{su1}	100			ns
Setup time, Clock low before V_{CC2}↑ or V_{SS}↓, t_{su2}	300‡			ns
Setup time, Enable high before V_{CC2}↑ or V_{SS}↓, t_{su3}	300‡			ns
Setup time, Positive Write high or low before V_{CC2}↑ or V_{SS}↓, t_{su4}	300‡			ns
Hold time, data high or low after clock↓, t_{h1}	100			ns
Hold time, Clock high after V_{CC2}↓ or V_{SS}↑, t_{h2}	300‡			ns
Hold time, Enable high after V_{CC2}↓ or V_{SS}↑, t_{h3}	0‡			ns
Hold time, Positive Write after V_{CC2}↓ or V_{SS}↑, t_{h4}	0‡			ns
Hold time, Enable low between successive V_{CC2}↑, t_{h5}	12‡			μs
Hold time, Enable low between successive V_{SS}↓, t_{h6}	300‡			ns
Operating free-air temperature, T_A	−55		125	°C

†The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
‡These minimum recommendations are not tested during manufacturing. Performance is dependent on application voltage and temperature and must be validated by the user.

electrical characteristics over recommended operating ranges of V_{CC1} and free-air temperature range, V_{CC2} = 225 V, V_{CC3} = 225 V, V_{SS} = 0 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$I_{O(off)}$	Off-state Q output current		V_O = 225 V		150	μA
			V_O = 0		−150	
V_{OH}	High-level output voltage	Q outputs	I_O = −70 mA, V_{CC1} = 12 V	V_{CC2}−40		V
			I_O = −90 mA, V_{CC1} = 12 V	V_{CC2}−45		
		Serial Out	I_O = −100 μA, V_{CC1} = 12 V	10.5		
V_{OL}	Low-level output voltage	Q outputs	I_O = 150 mA		30	V
		Serial Out	I_O = 100 μA		1	
I_{IH}	High-level input current		V_{IH} = V_{CC1}		100	μA
I_{IL}	Low-level input current		V_{IL} = 0		−10	μA
I_{CC1}	Supply current from V_{CC1}		One Q output high		4	mA
			All Q outputs low or high impedance		2	
I_{CC3}	Supply current from V_{CC3}‡		One Q output high, V_{CC1} = 12 V		10	mA
			All Q outputs low or high impedance, V_{CC1} = 12 V		200	μA

switching characteristics over recommended operating range of V_{CC1}, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level serial output from clock	C_L = 50 pF to V_{SS}, See Figures 3 and 4		400	ns
t_{PHL}	Propagation delay time, high-to-low level serial output from clock			400	ns

‡I_{CC3} is measured with V_{CC2} and V_{CC3} shorted together.

PARAMETER MEASUREMENT INFORMATION

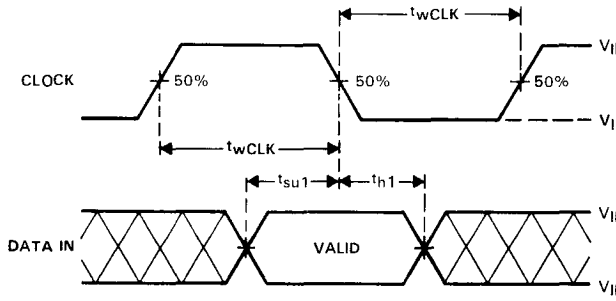

FIGURE 1. INPUT TIMING VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
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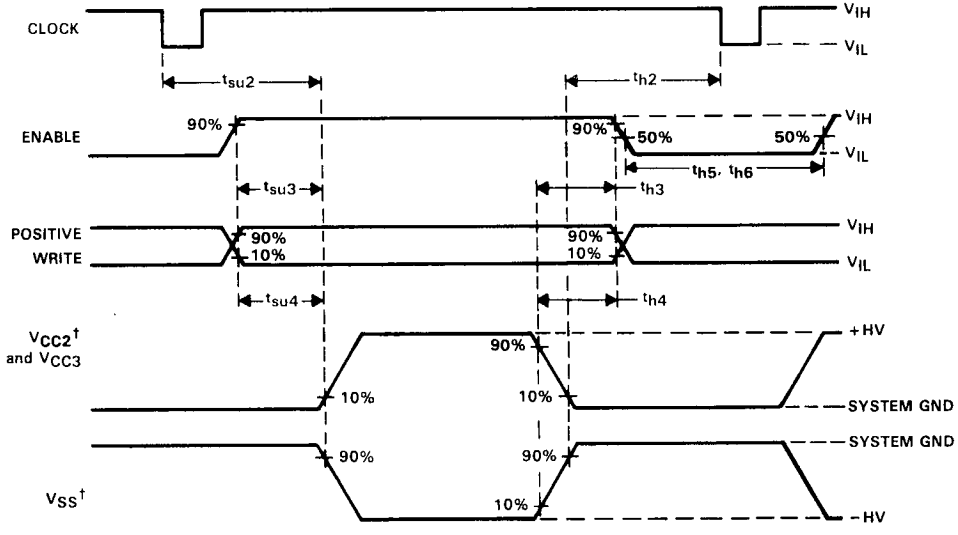
PARAMETER MEASUREMENT INFORMATION



†Timing waveforms are with respect to V_{CC2} or V_{SS}, as appropriate.

FIGURE 2. CONTROL INPUT TIMING VOLTAGE WAVEFORMS

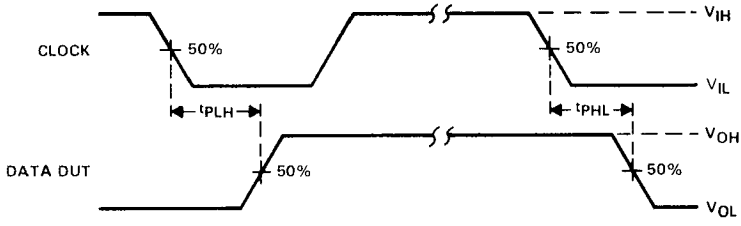
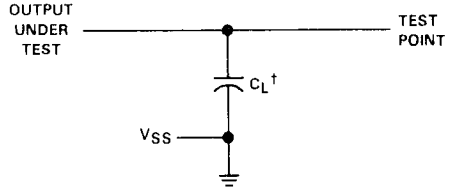


FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY TIMES, CLOCK TO DATA OUT



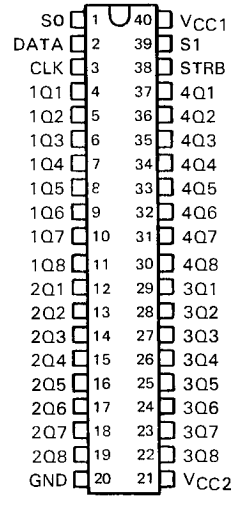
†C_L includes probe and jig capacitance.

FIGURE 4. LOAD CIRCUIT

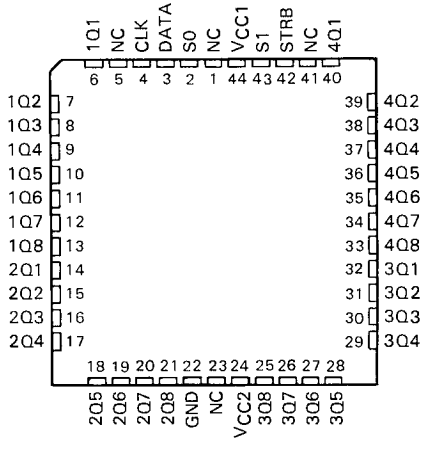
D2471, DECEMBER 1985—RE\ JULY 1989

- Controls 32 Electrodes
- 100-V Totem-Pole Outputs
- Low Stand-by Power Consumption
- All Outputs Contain Sink and Source Clamp Diodes
- 15-mA Steady-State Output Current
- Rugged DMOS Outputs
- CMOS Inputs
- Direct Replacement for SN75500A

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

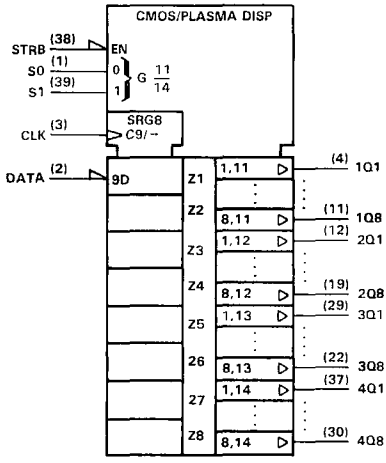
The SN65500E and SN75500E are monolithic BIDFET† integrated circuits designed to perform the line select operation of a matrix-addressable display. The device inputs are diode-clamped CMOS inputs.

The outputs of these drivers are normally low and can be selectively switched high when the strobe input is low. Selection of the outputs is achieved through the data, S0, and S1 inputs. The 8-bit data stored internally in the serial register is inverted and sent to one of four output sections by the 2-line to 4-line decoder. All other outputs remain low. Internal circuits provide a high-current pulse to the level-shifting circuit during positive output transitions. When the output transition is complete, the low steady-state current reduces the circuit's standby power consumption. All outputs contain clamp diodes to the V_{CC2} and GND supply inputs.

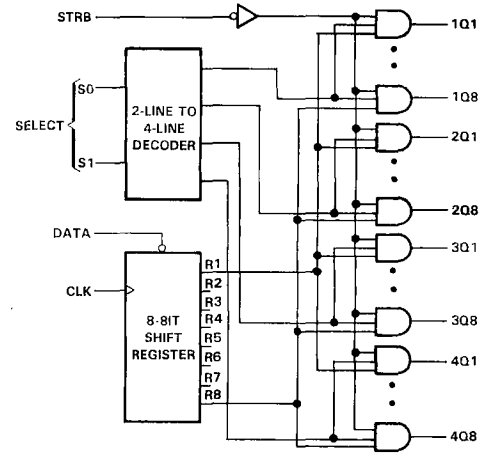
The SN65500E is characterized for operation from −40°C to 85°C. The SN75500E is characterized for operation from 0°C to 70°C.

†BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

logic symbol†



functional block diagram (positive logic)



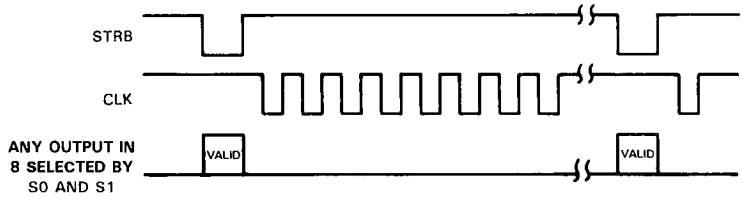
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

FUNCTION TABLE

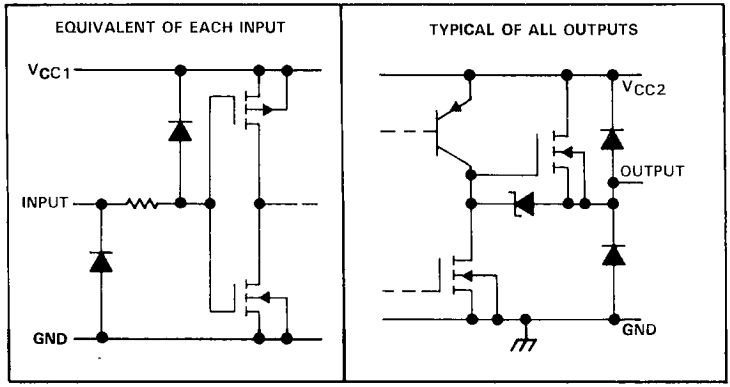
FUNCTION	INPUTS					OUTPUTS						
	DATA	CLK	SELECT S1	SELECT S0	STRB	SHIFT REGISTER R1	SHIFT REGISTER R2	SHIFT REGISTER R3 ... R8	1Q1 ... 1Q8	2Q1 ... 2Q8	3Q1 ... 3Q8	4Q1 ... 4Q8
LOAD	H	↑	X	X	H	L	$R1_n$	$R2_n$ ... $R7_n$	L ... L	L ... L	L ... L	L ... L
	L	↑	X	X	H	H	$R1_n$	$R2_n$ ... $R7_n$	L ... L	L ... L	L ... L	L ... L
STROBE	X	X	X	X	H	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	L ... L	L ... L	L ... L
	X	H	L	L	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	R1 ... R8	L ... L	L ... L	L ... L
	X	H	L	H	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	R1 ... R8	L ... L	L ... L
	X	H	H	L	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	L ... L	R1 ... R8	L ... L
	X	H	H	H	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	L ... L	L ... L	R1 ... R8

H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
R1 . . . R8 = levels currently at internal outputs of shift registers one through eight, respectively.
$R1_n$ . . . $R8_n$ = levels at shift-register outouts R1 through R8, respectively, before the most recent ↑ transition of the clock.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 100 V
Input voltage . . . . . V_{CC1} + 0.3 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65500E . . . . . −40°C to 85°C
SN75500E . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C
Case temperature for 10 seconds: FN package . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	mW	14.2 mW/°C	1136 mW	923 mW
N	1275 mW	10.2 mW/°C	816 mW	663 mW

recommended operating conditions

		SN65500E			SN75500E			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC1}		10.8	12	13.2	10.8	12	13.2	V
Supply voltage, V_{CC2}		0		100	0		100	V
High-level input voltage, V_{IH}, as a percentage of V_{CC1}		75%			75%			
Low-level input voltage, V_{IL}, as a percentage of V_{CC1}				25%			25%	
High-level output clamp current				20			20	mA
Low-level output clamp current				−20			−20	mA
Clock frequency, f_{clock} (see Figure 2)		0		8	0		8	MHz
Duration of high or low clock pulse, t_w		62			62			ns
Setup time, t_{su}	Data inputs before clock↑	20			20			ns
	Select inputs before strobe↓	50			50			
Hold time, t_h	Data inputs after clock↑ (see Note 2)	50			50			ns
	Strobe input high after clock↑	50			50			
	Select inputs after strobe↑	50			50			
Operating free-air temperature, T_A		−40		85	0		70	°C

NOTE 2: For operation above 25 °C junction temperature, refer to Figure 2.

electrical characteristics over recommended operating free-air temperature range

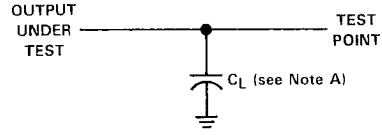
PARAMETER		TEST CONDITIONS		SN65500E			SN75500E			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	Input clamp voltage	V_{CC1} = 12 V,	I_I = −12 mA		−1	−1.5		−1	−1.5	V
V_{OH}	High-level output voltage	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	94	97.5		95	97.5		V
			I_{OH} = −10 mA	92	94.5		93	94.5		
			I_{OH} = −15 mA	90	93.5		91	93.5		
V_{OL}	Low-level output voltage	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2		0.85	2	V
			I_{OL} = 10 mA		2	4		2	4	
			I_{OL} = 15 mA		2.75	5		2.75	5	
V_{OK}	Output clamp voltage	V_{CC2} = 0	I_O = 20 mA		1	2.5		1	2.5	V
			I_O = −20 mA		−1.2	−2.5		−1.2	−2.5	
I_{IH}	High-level input current	V_{CC1} = 13.2 V,	V_I = V_{IH} min			1			1	μA
I_{IL}	Low-level input current	V_{CC1} = 13.2 V,	V_I = V_{IL} max			−1			−1	μA
I_{CC1}	Supply current	V_{CC1} = 13.2 V,	V_{CC2} = 100 V		0.05	1		0.05	1	mA
I_{CC2}	Supply current	V_{CC2} = 100 V			1	5		1	3	mA

†All typical values are at V_{CC1} = 12 V, T_A = 25 °C.

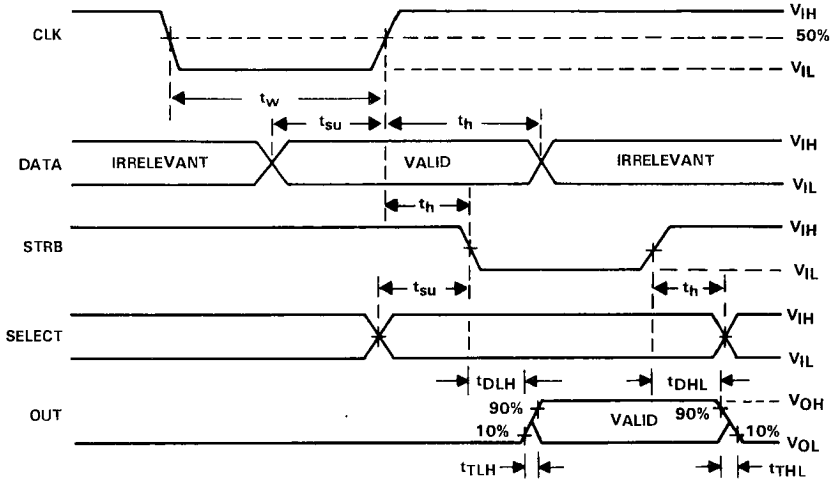
switching characteristics, V_{CC1} = 12 V, V_{CC2} = 100 V, T_A = 25 °C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 30 pF, See Figure 1		250	ns
t_{DLH}	Delay time, low-to-high-level output from strobe input				ns
t_{THL}	Transition time, high-to-low-level output				ns
t_{TLH}	Transition time, low-to-high-level output			300	ns

PARAMETER MEASUREMENT INFORMATION



LOAD TEST CIRCUIT



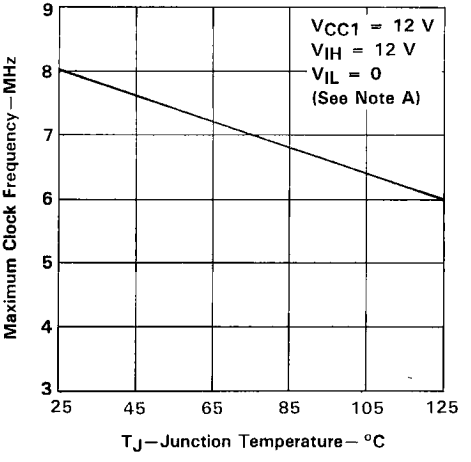
VOLTAGE WAVEFORMS

NOTE A. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

MAXIMUM CLOCK FREQUENCY
vs
VIRTUAL JUNCTION TEMPERATURE



NOTE A: This curve assumes a symmetrical clock pulse.

FIGURE 2

THERMAL INFORMATION

junction temperature formula

$$T_J = T_A + P_D R_{\theta JA}$$
$$T_J = T_C + P_D R_{\theta JC}$$

where

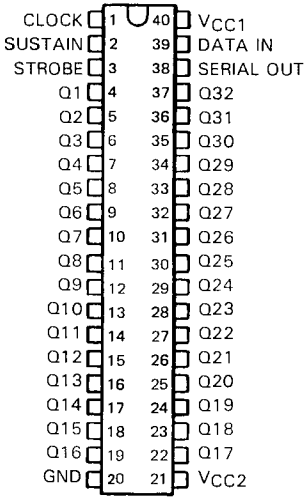
T_J = virtual junction temperature
T_A = free-air temperature
P_D = average device power dissipation
R_θ = thermal resistance (junction-to-air, $R_{\theta JA}$, or junction-to-case, $R_{\theta JC}$)

PACKAGE TYPE	$R_{\theta JA}$	$R_{\theta JC}$
FN 44-pin plastic	70°C/W	22°C/W
N 40-pin plastic	97°C/W	27°C/W

D2472, MARCH 1983—REVISED OCTOBER 1989

- **Controls 32 Electrodes**
- **100-V Totem-Pole Outputs**
- **Low Standby Power Consumption**
- **All Outputs Contain Sink and Source Clamp Diodes**
- **15-mA Steady-State Output Current**
- **Rugged DMOS Outputs**
- **CMOS Inputs**
- **Direct Replacement for SN75501C**

N PACKAGE
(TOP VIEW)



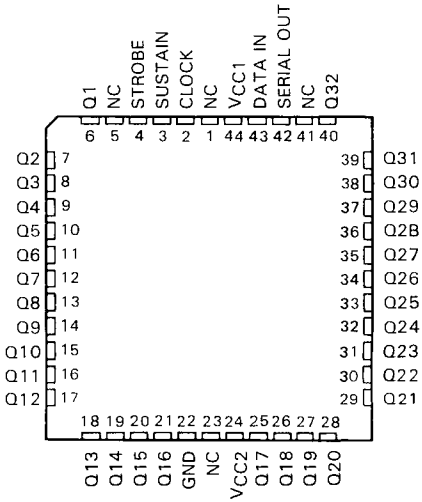
description

The SN65501E and SN75501E are monolithic BIDFET† integrated circuits designed to provide the serial-to-parallel conversion and level translation of data in a matrix-addressable display. The device inputs are diode-clamped CMOS inputs.

The Q outputs of these drivers are normally high and can be switched either selectively or together. Any output whose associated register bit (in the internal 32-bit serial register) contains a low will switch low when STROBE is low if SUSTAIN is high. All other outputs remain high. When SUSTAIN is low, all outputs switch low independently of the data or strobe inputs. This feature can be used to generate a portion of the sustain pulse required in the operation of an ac plasma display. The internal level-shift circuits provide additional drive during the times that the outputs switch high to facilitate fast rise times while maintaining low standby power consumption. All outputs contain clamp diodes to the V_{CC2} and GND supply inputs.

The SN65501E is characterized for operation over the temperature range of −40°C to 85°C. The SN75501E is characterized for operation over the temperature range of 0°C to 70°C.

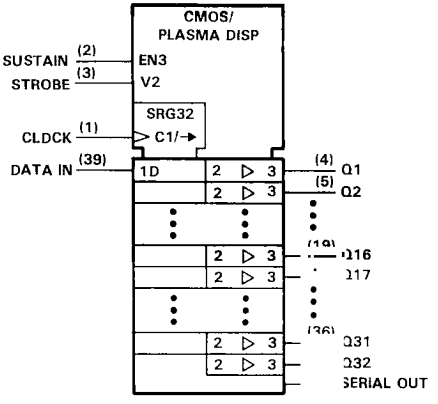
FN PACKAGE
(TOP VIEW)



NC No internal connection

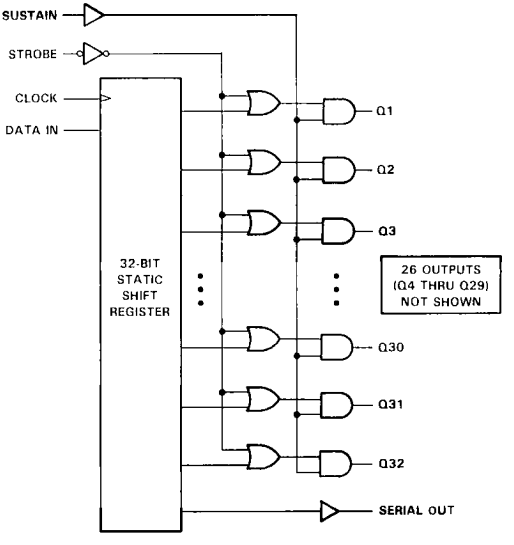
† BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

functional block diagram (positive logic)

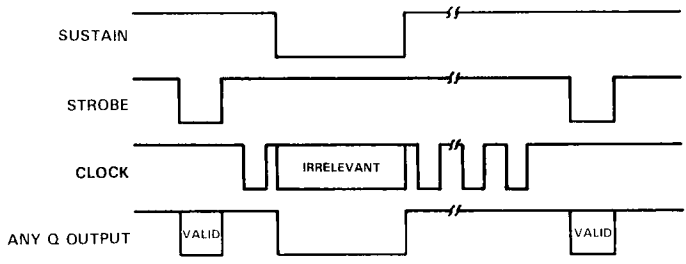


FUNCTION TABLE

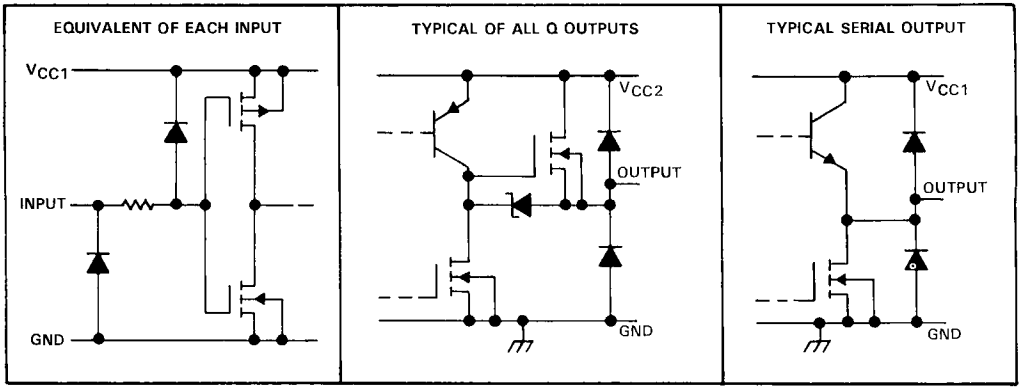
FUNCTION	INPUTS				OUTPUTS						
	DATA	CLOCK	STROBE	SUSTAIN	SHIFT REGISTER R1	SHIFT REGISTER R2	SHIFT REGISTER R3 . . . R32	SERIAL DATA	Q1	Q2	Q3 . . . Q32
LOAD	H	↑	H	H	H	$R1_n$	$R2_n$ . . . $R31_n$	$R32_n$	H	H	H . . . H
	L	↑	H	H	L	$R1_n$	$R2_n$ . . . $R31_n$	. . .	H	H	H . . . H
STROBE	X	X	H	H	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	. . .	H	H	H . . . H
	X	H	L	H	$R1_n$	$R2_n$	$R3_n$	. . .	R1	R2	R3 . . . R32
SUSTAIN	X	X	X	L	$R1_n$	$R2_n$	$R3_n$ . . .	.	L	L	L . . . L

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
R1 . . . R32 = levels currently at internal outputs of shift registers one through thirty-two, respectively.
$R1_n$ . . . $R32_n$ = levels at shift-register outputs R1 thro gh R32 respectively, before the most recent ↑ transition at the CLOCK input.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 100 V
Input voltage . . . . . V_{CC1} to 0.3 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65501E . . . . . −40°C to 85°C
SN75501E . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1775 mW	14.2 mW/°C	1136 mW	923 mW
N	1275 mW	10.2 mW/°C	816 mW	663 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	13.2	V
Supply voltage, V_{CC2}		0		100	V
High-level input voltage, V_{IH}		0.75 V_{CC1}			V
Low-level input voltage, V_{IL}				0.25 V_{CC1}	V
High-level Q output clamp current, I_{OKH}				20	mA
Low-level Q output clamp current, I_{OKL}				−20	mA
Clock frequency, f_{clock}, at or below, 25°C junction temperature (see Note 2)		0		8	MHz
Duration of high or low clock pulse, t_w		62			ns
Setup time, t_{su}	Data inputs before ↑	20			ns
	Data inputs after ↑	50			
Hold time, t_h	[illegible] high after [illegible]	[illegible]			ns
	[illegible] high after [illegible]	[illegible]			
Operating free-air temperature, T_A	[illegible]	−[illegible]		85	°C
	SN75501E	0		70	

NOTE 2: See Figure 3 for maximum clock frequency when devices are operated in cascade or for operation above T_J = 25°C.

electrical characteristics over recommended operating free-air temperature range

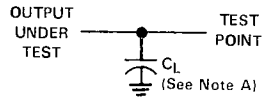
PARAMETER			TEST CONDITIONS		SN65501E			SN75501E			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	Input clamp voltage		V_{CC1} = 12 V,	I_I = 12 mA		−1	−1.5		−1	−1.5	V
V_{OH}	High-level output voltage	Q outputs	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	94	97.5		95	97.5		V
				I_{OH} = −10 mA	92	94.5		93	94.5		
				I_{OH} = −15 mA	90	93.5		91	93.5		
		SERIAL OUT	V_{CC1} = 10.8 V,	I_{OH} = −100 μA	9	10		9	10		
V_{OL}	Low-level output voltage	Q outputs	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2		0.85	2	V
				I_{OL} = 10 mA		2	4		2	4	
				I_{OL} = 15 mA		2.75	5		2.75	5	
		SERIAL OUT	V_{CC1} = 10.8 V,	I_{OL} = 100 μA		0.1	1		0.1	1	
V_{OK}	Output clamp voltage	Q output	V_{CC2} = 0	I_{OK} = 20 mA		1	2.5		1	2.5	V
				I_{OK} = −20 mA		−1.2	−2.5		−1.2	−2.5	
I_{IH}	High-level input current		V_{CC1} = 13.2 V, V_{CC2} = 100 V	V_{IH} = V_{IH}min,			1			1	μA
I_{IL}	Low-level input current		V_{CC1} = 13.2 V, V_{CC2} = 100 V	V_{IL} = V_{IL}max,			−1			−1	μA
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 13.2 V, V_{CC2} = 100 V			0.05	1		0.05	1	mA
I_{CC2}	Supply current from V_{CC2}		V_{CC2} = 100 V			1	5		1	3	mA

† Typical values are at V_{CC1} = 12 V, T_A = 25°C.

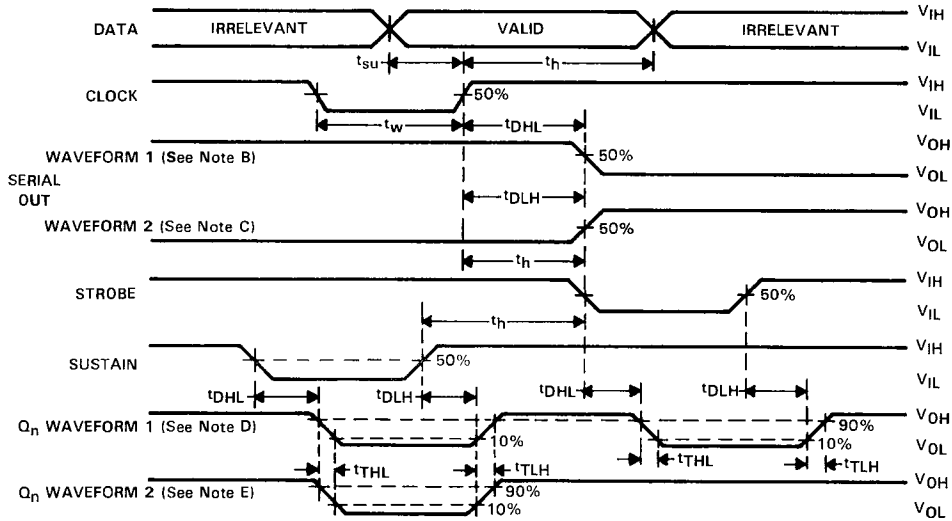
switching characteristics, V_{CC1} = 12 V, V_{CC2} = 100 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level outputs	STROBE to Q outputs	C_L = 30 pF			.	ns
		SUSTAIN to Q outputs	C_L = 30 pF			.	
		CLOCK to SERIAL OUT	C_L = 20 pF			147	
t_{DLH}	Delay time, low-to-high-level outputs	STROBE to Q outputs	C_L = 30 pF			450	ns
		SUSTAIN to Q outputs	C_L = 30 pF			450	
		CLOCK to SERIAL OUT	C_L = 20 pF			147	
t_{THL}	Transition time, high-to-low-level Q output		C_L = 30 pF			200	ns
t_{TLH}	Transition time, low-to-high-level Q output		C_L = 30 pF			300	ns

PARAMETER MEASUREMENT INFORMATION



LOAD TEST CIRCUIT



NOTES: A. C_L includes probe and jig capacitance.
B. Serial out waveform for internal conditions such that a low is registered in R32.
C. Serial out waveform for internal conditions such that a high is registered in R32.
D. Q_n output with a low stored in associated register R_n.
E. Q_n output with a high stored in associated register R_n.

VOLTAGE WAVEFORMS

FIGURE 1. SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

MAXIMUM CLOCK FREQUENCY
vs
JUNCTION TEMPERATURE

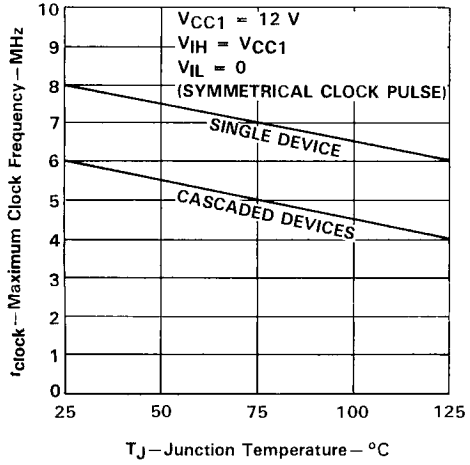


FIGURE 2

INPUT VOLTAGE LOGIC LEVEL LIMITS
vs
V_{CC1} SUPPLY VOLTAGE

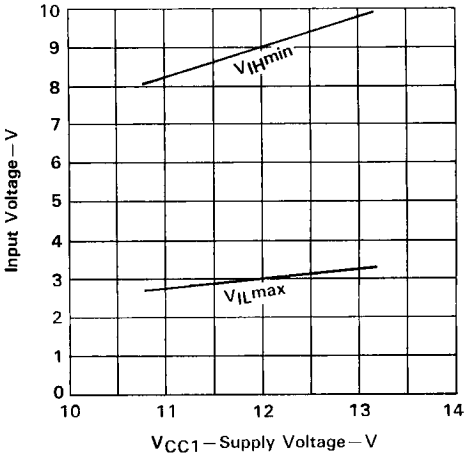


FIGURE 3

THERMAL CHARACTERISTICS

junction temperature formula

$$T_J = T_A + P_D R_\theta$$

where

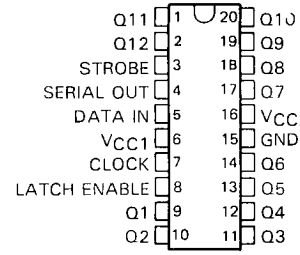
T_J = virtual junction temperature
T_A = free-air temperature
P_D = average device power dissipation
R_θ = thermal resistance (junction-to-air, $R_{\theta JA}$, or junction-to-case, $R_{\theta JC}$)

PACKAGE	[illegible]	$R_{\theta JC}$
FN	7 [illegible]	22°C/W
N	100°C/W	27°C/W

D2654, DECEMBER 1985—REVISED OCTOBER 1989

- Each Device Drives 12 Lines
- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- TTL-Compatible Inputs
- Latches on All Driver Outputs

DW DR N PACKAGE
(TDP VIEW)



description

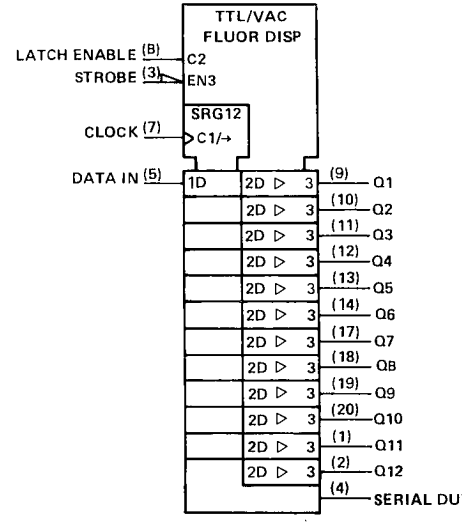
The SN65512B and SN75512B are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display.

All device inputs are diode-clamped p-n-p inputs and will assume a high logic level when open-circuited. The nominal input threshold is 1.5 V. Outputs are totem-pole structures formed by an n-p-n emitter follower and double-diffused MOS (DMOS) transistors.

The device consists of a 12-bit shift register, 12 latches, and 12 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 12 latches. The active-low STROBE input enables all Q outputs. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by LATCH ENABLE or STROBE.

The SN65512B is characterized for operation from −40°C to 85°C. The SN75512B is characterized for operation from 0°C to 70°C.

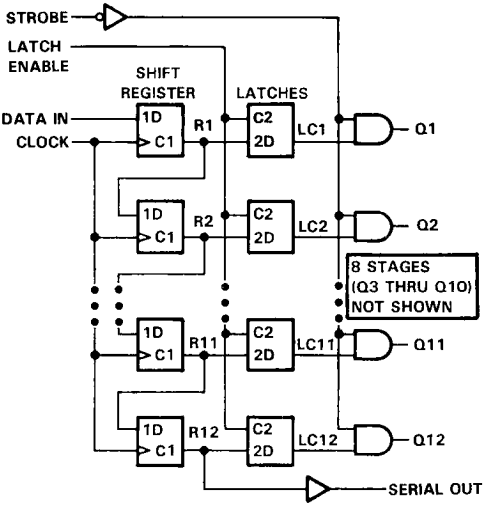
logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

† BIDFET —Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

logic diagram (positive logic)

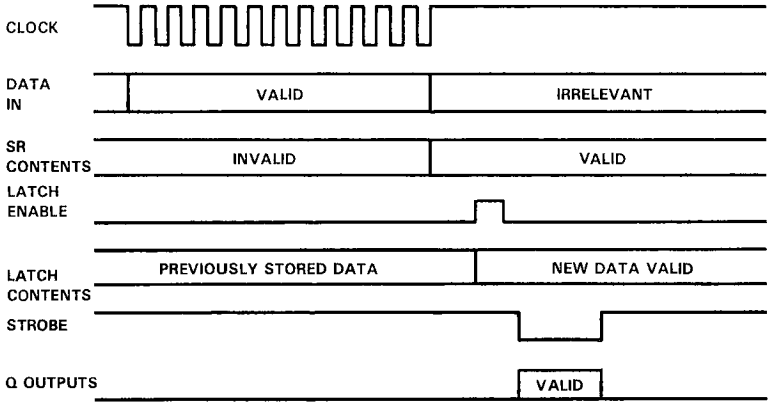


FUNCTION TABLE

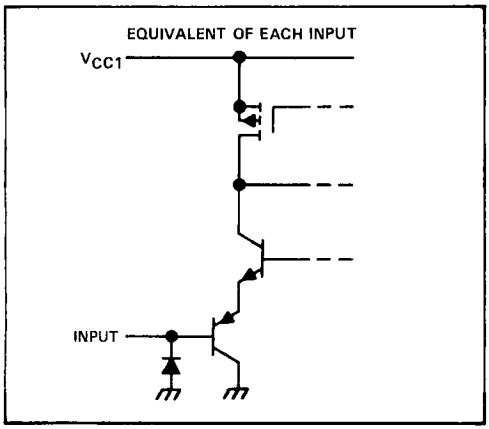
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R12	LATCHES LC1 THRU LC12	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE			SERIAL	Q1 THRU Q12
LOAD	↑	X	X	Load and shift†	Determined by LATCH ENABLE‡		Determined by SERIAL
	Not↑	X	X	No change	Determined by LATCH ENABLE‡	R12	Determined by STROBE
LATCH	X	L	X	As determined above	Stored data	R12	Determined by STROBE
	X	H	X		New data	R12	Determined by STROBE
STROBE	X	X	H	As determined ebove	Determined by LATCH ENABLE‡	R12	All L
	X	X	L		Determined by LATCH ENABLE‡	R12	LC1 thru LC12, respectively

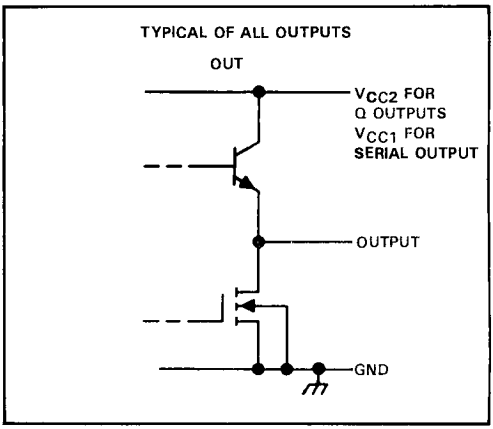
H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
† R12 takes on the state of R11, R11 takes on the state of R10, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.
‡ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 70 V
Input voltage . . . . . V_{CC1}
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65512B . . . . . −40°C to 85°C
SN75512B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		SN65512B		SN75512B		UNIT
		MIN	MAX	MIN	MAX	
Supply voltage, V_{CC1}		5	15	5	15	V
Supply voltage, V_{CC2}		0	60	0	60	V
High-level input voltage, V_{IH}		2		2		V
Low-level input voltage, V_{IL}			0.8		0.8	V
High-level output current, I_{OH}			−25		−25	mA
Low-level output current, I_{OL}	V_{CC1} = 10 V		5		5	mA
Clock frequency, f_{clock}	V_{CC1} = 15 V, T_A = 25°C	0	4	0	4	MHz
	V_{CC1} = 5 V, T_A = 25°C	0	1	0	1	
Pulse duration, CLOCK high or low, t_w	V_{CC1} = 15 V, T_A = 25°C	100		100		ns
	V_{CC1} = 5 V, T_A = 25°C	500		500		
Setup time, DATA IN before CLOCK↑, t_{su} (see Figure 1)	V_{CC1} = 15 V, T_A = 25°C	100		100		ns
	V_{CC1} = 5 V, T_A = 25°C	250		250		
Hold time, DATA IN after CLOCK↑, t_h (see Figure 1)	V_{CC1} = 15 V, T_A = 25°C	50		50		ns
	V_{CC1} = 5 V, T_A = 25°C	250		250		
Operating free-air temperature, T_A		−40	85	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	Q outputs	I_{OH} = −25 mA		57.5	58		V
		Serial output	I_{OH} = −200 μA, V_{CC1} = 10 V		9	9.5		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 5 mA, V_{CC1} = 10 V			2.6	5	V
		Serial output	I_{OL} = 200 μA, V_{CC1} = 10 V			0.05	0.2	
I_{IH}	High-level input current		V_{CC1} = 15 V, V_I = 5 V			0.01	1	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V, V_I = 0.8 V			−25	−150	μA
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 15 V	V_I = 5 V		80	500	μA
				V_I = 0.8 V		2	6	mA
I_{CC2}	Supply current from V_{CC2}		V_{CC1} = 15 V	All [illegible]ts high		10	100	μA
				S[illegible]t 2 V		0.8	3	mA

†All typical values are at V_{CC1} = 10 V, T_A = 25°C.

switching characteristics, V_{CC1} = 10 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output	C_L = 30 pF, See Figure 2		300	ns
t_{DLH}	Delay time, low-to-high-level output			300	ns
t_{THL}	Transition time, high-to-low-level output			500	ns
t_{TLH}	Transition time, low-to-high-level output			500	ns

PARAMETER MEASUREMENT INFORMATION

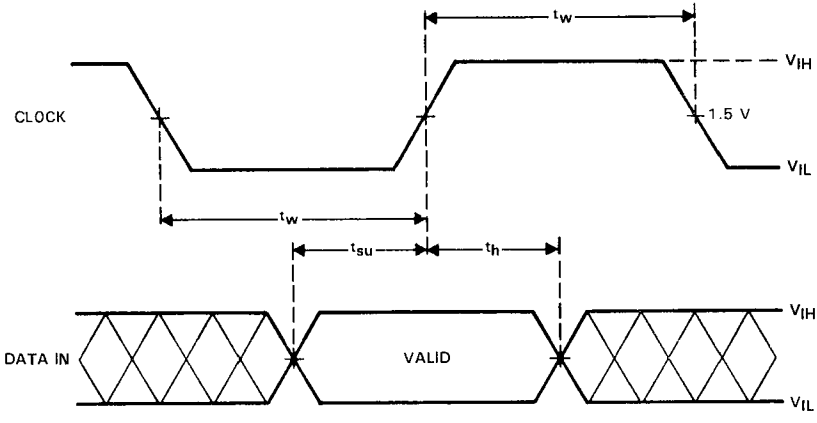


FIGURE 1. INPUT TIMING VOLTAGE WAVEFORMS

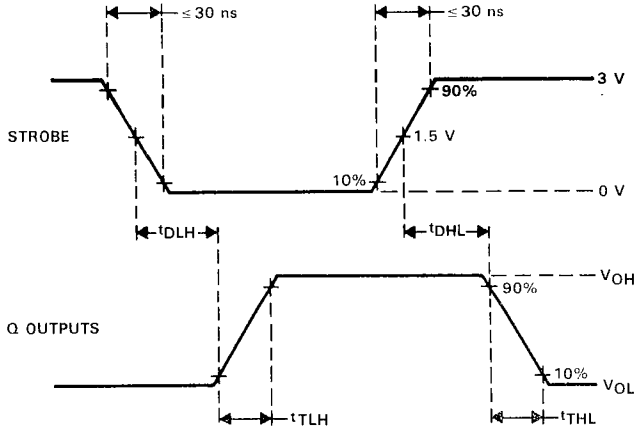


FIGURE 2. SWITCHING-TIME VOLTAGE WAVEFORMS

D2720, MARCH 1983—REVISED MAY 1990

- Each Device Drives 32 Lines
- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially Shifted Data Input
- Latches on All Driver Outputs

description

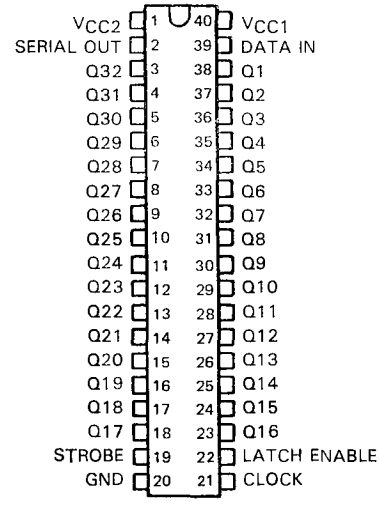
The SN65518 and SN75518 are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display.

The devices each consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. While LATCH ENABLE is high, parallel data is transferred to the output buffers through a 32-bit latch. Data present in the latch during the high-to-low transition of LATCH ENABLE is latched. When STROBE is low, all Q outputs are enabled. When STROBE is high, all Q outputs are low.

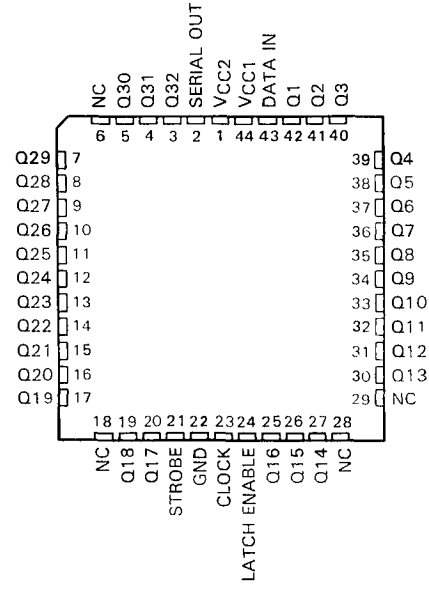
Serial data output from the shift register may be used to cascade additional devices. This output is not affected by LATCH ENABLE or STROBE.

The SN65518 is characterized for operation from −40°C to 85°C and the SN75518 is characterized for operation from 0°C to 70°C.

N PACKAGE
(TOP VIEW)



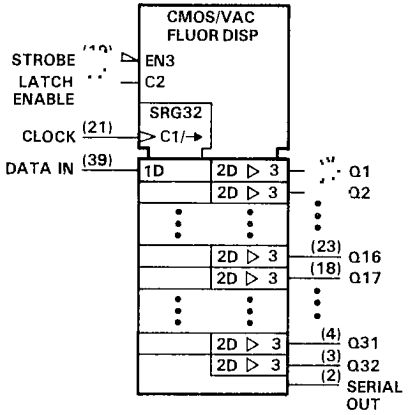
FN PACKAGE
(TOP VIEW)



†BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip—patented process.

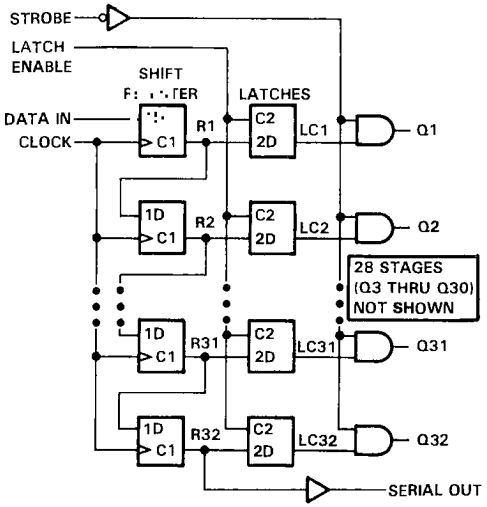
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)

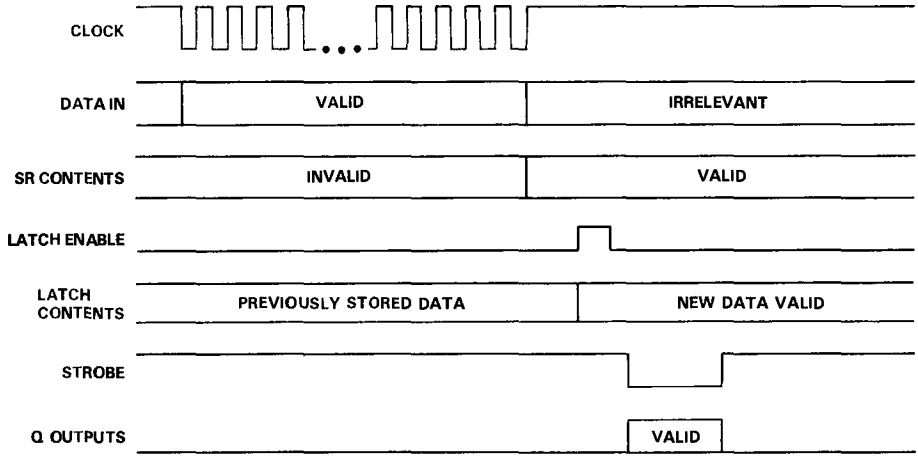


FUNCTION TABLE

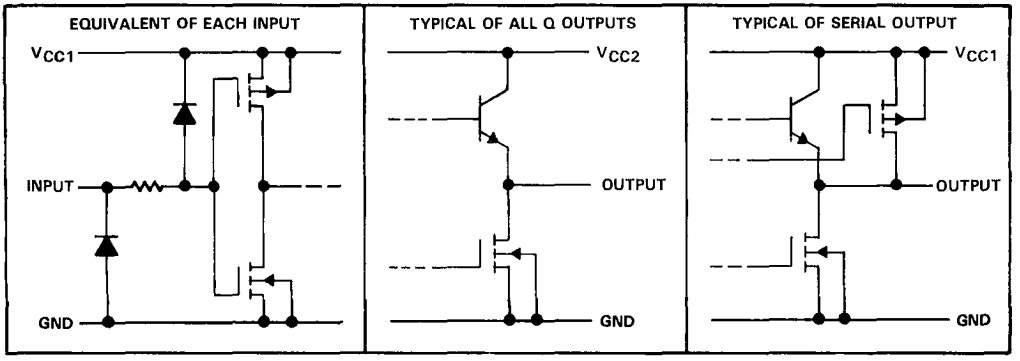
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS	LATCHES	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE	R1 THRU R32	LC1 THRU LC32	SERIAL	Q1 THRU Q32
LOAD	↑	X	X	Load and shift†	Determined by	R32	Determined by STROBE
	No↑	X	X	No change	LATCH ENABLE‡		
LATCH	X	L	X	As determined	Stored data	R32	Determined by STROBE
	X	H	X	above	New Data		
STROBE	X	X	H	As determined	Determined by	R32	All L
	X	X	L	above	LATCH ENABLE‡		LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
†R32 and the serial output take on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.
‡New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 70 V
Input voltage, V_I . . . . . V_{CC1}
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65518 . . . . . −40°C to 85°C
SN75518 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1700 mW	13.6 mW/°C	1088 mW	884 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW

recommended operating conditions, T_A = 25°C (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{CC1}		4.5	15	V
Supply voltage, V_{CC2}		0	60	V
High-level input voltage, V_{IH} (see Figure 1)	V_{CC1} = 4.5 V	3.5		V
	V_{CC1} = 15 V	12		
Low-level input voltage, V_{IL} (see Figure 1)		−0.3	0.8	V
High-level output current, I_{OH}			−25	mA
Low-level output current, I_{OL}			2	mA
Clock frequency, f_{clock} (see Figure 2)	V_{CC1} = 10 V to 15 V	0	5	MHz
	V_{CC1} = 4.5 V	0	1	
Pulse duration, CLOCK high, $t_{w(CKH)}$	V_{CC1} = 10 V to 15 V	100		ns
	V_{CC1} = 4.5 V	500		
Pulse duration, CLOCK low, $t_{w(CKL)}$	V_{CC1} = 10 V to 15 V	100		ns
	V_{CC1} = 4.5 V	500		
Setup time, DATA IN before CLOCK↑, t_{su}	V_{CC1} = 10 V to 15 V	75		ns
	V_{CC1} = 4.5 V	150		
Hold time, DATA IN after CLOCK↑, t_h	V_{CC1} = 10 V to 15 V	75		ns
	V_{CC1} = 4.5 V	150		
Operating free-air temperature, T_A	S[illegible]8	−40	85	°C
	[illegible]18	0	70	

electrical characteristics over recommended ranges of operating free-air temperature and V_{CC1} (unless otherwise noted), V_{CC2} = 60 V

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	Q outputs	I_{OH} = −25 mA	57.5	58		V
		SERIAL OUT	V_{CC1} = 5 V, I_{OH} = −20 μA	4.5	4.9	5	
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 mA			5	V
		SERIAL OUT	I_{OL} = 20 μA		0.06	0.8	
I_{IH}	High-level input current		V_{CC1} = 15 V, V_I = 15 V		0.1	1	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V, V_I = 0 V		−0.1	−1	μA
I_{CC1}	Supply current		V_{CC1} = 4.5 V		1.8	4	mA
			V_{CC1} = 15 V		2	5	
I_{CC2}	Supply current	SN65518	Outputs high, T_A = −40°C			12	mA
		SN65518, SN75518	Outputs high, T_A = 0°C to MAX		7	10	
			Outputs low		0.01	0.5	

†All typical values are at T_A = 25°C.

switching characteristics, V_{CC2} = 60 V, C_L = 50 pF, T_A = 25°C (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	UNIT
t_d	Delay time, CLOCK to DATA OUT		V_{CC1} = 4.5 V	C_L = 15 pF, See Figure 4		ns
			V_{CC1} = 15 V		150	
t_{DHL}	Delay time, high-to-low-level Q output	from LATCH ENABLE	V_{CC1} = 4.5 V	See Figure 5	1.5	μs
		from STROBE		See Figure 6	1	
		from LATCH ENABLE	V_{CC1} = 15 V	See Figure 5	0.5	
		from STROBE		See Figure 6	0.5	
t_{DLH}	Delay time, low-to-high-level Q output	from LATCH ENABLE	V_{CC1} = 4.5 V	See Figure 5	1.5	μs
		from STROBE		See Figure 6	1	
		from LATCH ENABLE	V_{CC1} = 15 V	See Figure 5	0.25	
		from STROBE		See Figure 6	0.25	
t_{THL}	Transition time, high-to-low-level Q output		V_{CC1} = 4.5 V	See Figure 6	3	μs
			V_{CC1} = 15 V		1.5	
t_{TLH}	Transition time, low-to-high-level Q output		V_{CC1} = 4.5 V	See Figure 6	2.5	μs
			V_{CC1} = 15 V		0.75	

RECOMMENDED OPERATING CONDITIONS

INPUT VOLTAGE LOGIC-LEVEL LIMITS
vs
SUPPLY VOLTAGE V_{CC1}

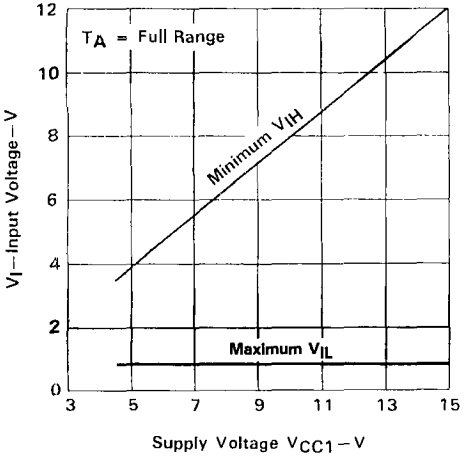


FIGURE 1

MAXIMUM INPUT DATA RATE
vs
SUPPLY VOLTAGE V_{CC1}

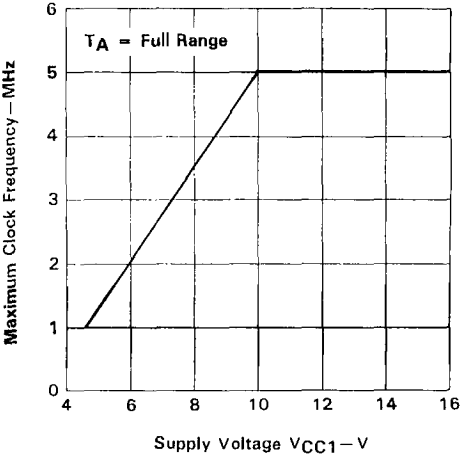


FIGURE 2

PARAMETER MEASUREMENT INFORMATION†

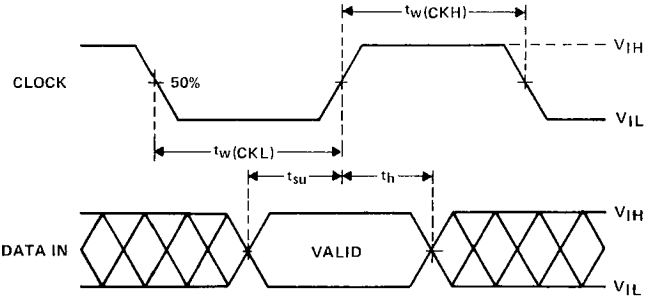


FIGURE 3. INPUT TIMING VOLTAGE WAVEFORMS

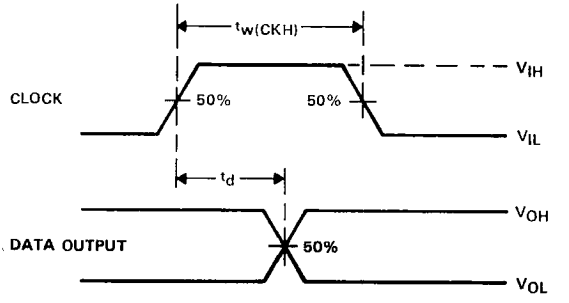


FIGURE 4. DATA OUTPUT SWITCHING TIMES

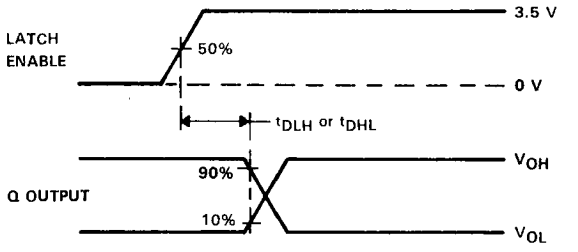


FIGURE 5. Q OUTPUT SWITCHING TIMES

†For testing purposes, all input pulses have maximum rise and fall times of 30 ns.

PARAMETER MEASUREMENT INFORMATION†

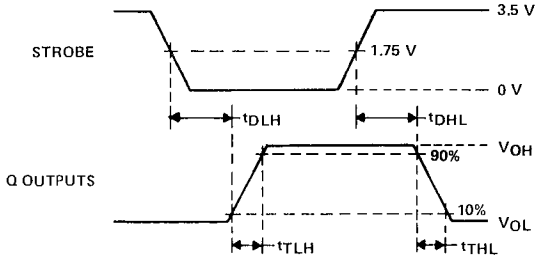


FIGURE 6. SWITCHING-TIME VOLTAGE WAVEFORMS

†For testing purposes, all input pulses have maximum rise and fall times of 30 ns.

D2743, MARCH 1983—REVISED OCTOBER 1989

- Each Device Drives 32 Electrodes
- High-Voltage Open-Drain DMOS Outputs
- 50-mA Output Current Capability
- CMOS-Compatible Inputs
- Very Low Steady-State Power Consumption

description

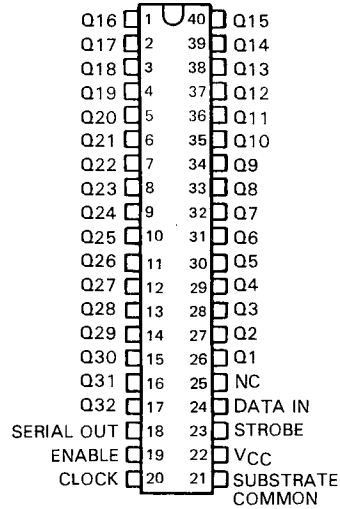
The SN65551, SN65552, SN75551, and SN75552 are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS-compatible and all outputs are high-voltage open-drain DMOS transistors. The SN75552 output sequence is reversed from the SN75551 for ease in printed circuit board layout.

The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to the SUBSTRATE COMMON terminal. Serial data is entered into the shift register on the high-to-low transition of CLOCK. A high at the ENABLE input allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When STROBE is low, all output transistors are turned on. The Serial Data output (SERIAL OUT) from the shift register may be used to cascade additional devices. This output is not affected by the ENABLE or STROBE inputs.

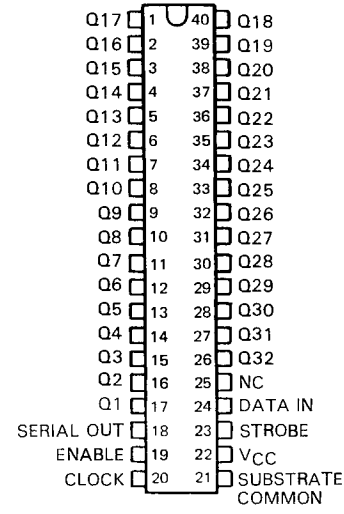
The SN65551 and SN65552 are characterized for operation from −40°C to 85°C. The SN75551 and SN75552 are characterized for operation from 0°C to 70°C.

N
DUAL-IN-LINE-PACKAGES
(TOP VIEW)

SN65551, SN75551



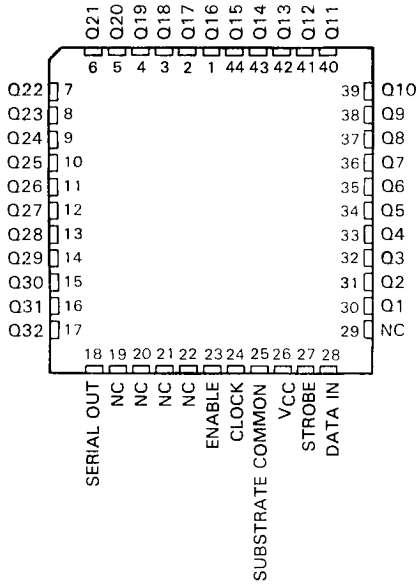
SN65552, SN75552



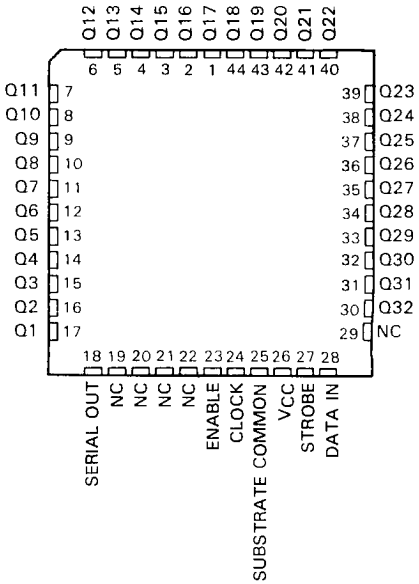
NC—No internal connection

† BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

SN65551, SN75551 . . . FN PACKAGE
(TOP VIEW)



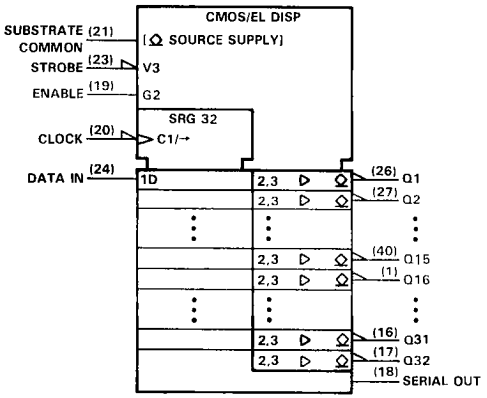
SN65552, SN75552 . . . FN PACKAGE
(TOP VIEW)



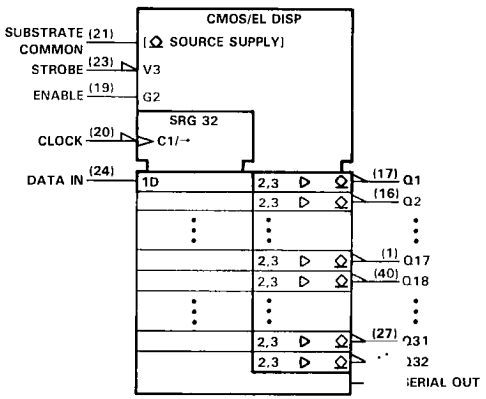
NC—No internal connection

logic symbols†

SN65551, SN75551

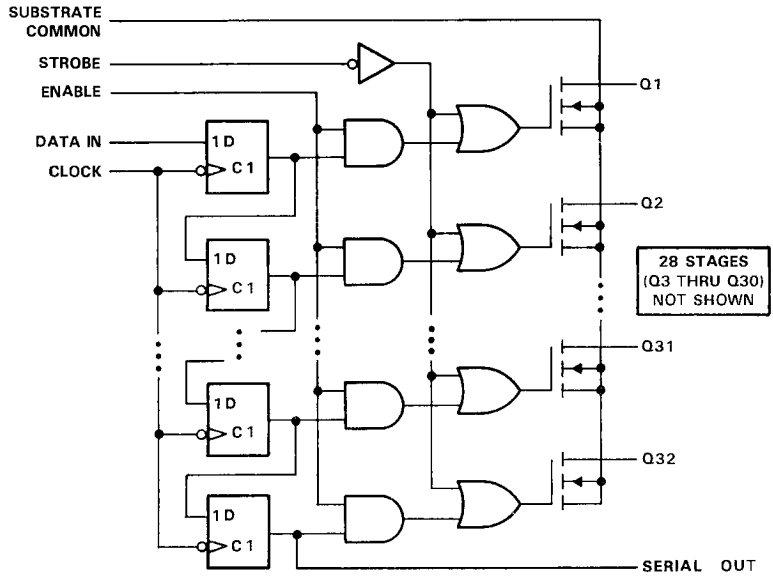


SN65552, SN75552



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. The symbol Ω here indicates an n-channel open-drain output.
Pin numbers shown are for the N package.

logic diagram (positive logic)

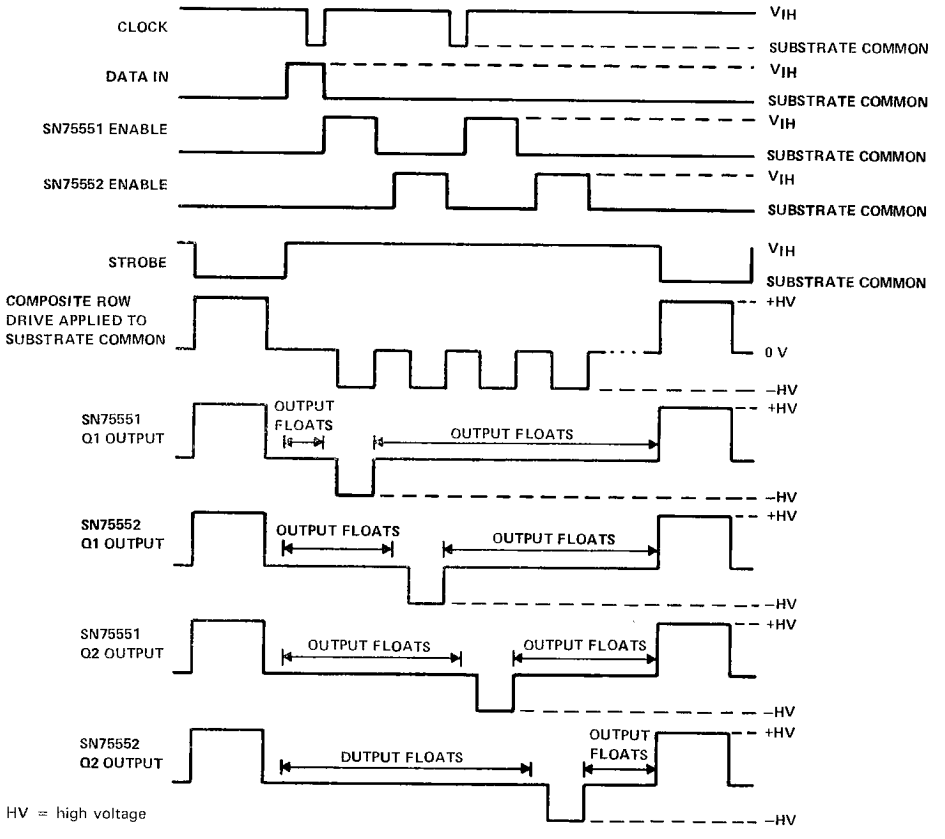


FUNCTION TABLE

FUNCTION5	CONTROL INPUTS			SHIFT REGISTERS	OUTPUTS	
	CLOCK	ENABLE	STROBE	R1 THRU R32	SERIAL	Q1 THRU Q32
LOAD	↓	X	X	Load and Shift†	R32	Determined by ENABLE and STROBE
	No ↓	X	X	No Change	R32	Determined by ENABLE and STROBE
ENABLE	X	L	H	As determined above	R32	All Q outputs off
	X	H	H	As determined above		Determined by R1 through R32
STROBE	X	X	L	As determined above	.	All Q outputs on

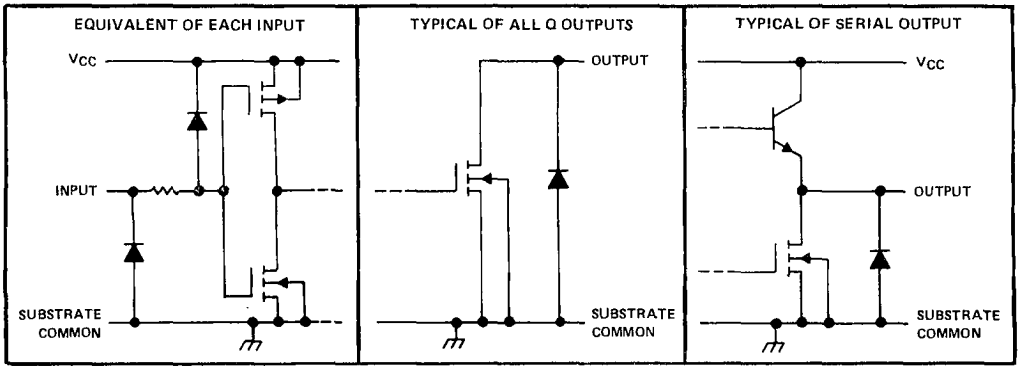
H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition.
†Register R32 takes on the state of R31, R31 takes on the state of R30,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



NOTE: During operation CLOCK, DATA IN, ENABLE, and STROBE are referenced to the Composite Row Drive signal received at the SUBSTRATE COMMON pin of the device.

schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Off-state Q output voltage, $V_{O(off)}$ . . . . . 225 V
Input voltage . . . . . V_{CC} + 0.3 V
Substrate common terminal current (see Note 2) . . . . . 1.5 A
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65551, SN65552 . . . . . −40°C to 85°C
SN75551, SN75552 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to SUBSTRATE COMMON terminal.
2. Duty cycle is limited by package dissipation.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	mW	13.6 mW/°C	1088 mW	884 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		10.8	12	15	V
V_{IH}	High-level input voltage (see Figure 1)	V_{CC} = 10.8 V	8.1		11.1	V
		V_{CC} = 15 V	11.25		15.3	
V_{IL}	Low-level input voltage (see Figure 1)	V_{CC} = 10.8 V	−0.3		2.7	V
		V_{CC} = 15 V	−0.3		3.75	
$V_{O(off)}$	Off-state Q output voltage		0		200	V
$I_{O(on)}$	On-state output current, duty cycle ≤ 1%, (see Figures 2, 3, and 4)	V_{CC} = 10.8 V, T_A = 25°C			50	mA
		V_{CC} = 15 V, T_A = 25°C			80	
I_{OK}	Output clamp current				−45	mA
f_{clock}	Clock frequency		0		4	MHz
t_w	Pulse duration, CLOCK high or low		125			ns
t_{su}	Setup time, DATA IN before CLOCK (see Figure 5)		50			ns
t_h	Hold time, DATA IN after CLOCK (see Figure 5)		100			ns
T_A	Operating free-air temperature		−40		85	°C
			0		70	

electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$I_{O(off)}$	Off-state Q output current		V_O = 200 V		10	μA
V_{OH}	High-level output voltage	Serial outputs	I_O = −100 μA	V_{CC}−1.5		V
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 50 mA, See Figure 3		30	V
		Serial output	I_{OL} = 100 μA		1	
I_{IH}	High-level input current		V_I @ V_{CC}		1	μA
I_{IL}	Low-level input current		V_I = 0		−1	μA
I_{CC}	Supply current from V_{CC}				250	μA

switching characteristics, V_{CC} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level SERIAL OUTPUT from CLOCK	C_L = 20 pF to ground, See Figure 6		200	ns
t_{PLH}	Propagation delay time, low-to-high level SERIAL OUTPUT from CLOCK			200	ns
$t_{d(on)}$	Turn-on delay time, Q outputs from ENABLE	I_{OL} = 50 mA, STROBE at V_{CC}, R_L = 1.4 kΩ to 100 V, See Figure 7		500	ns

RECOMMENDED OPERATING CONDITIONS

INPUT VOLTAGE LOGIC-LEVEL LIMITS
vs
SUPPLY VOLTAGE

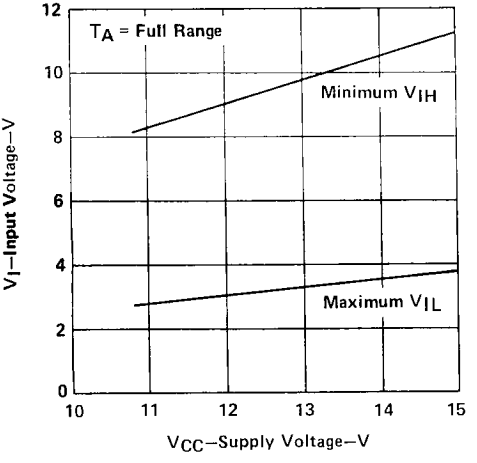


FIGURE 1

MAXIMUM ON-STATE Q OUTPUT CURRENT
vs
SUPPLY VOLTAGE

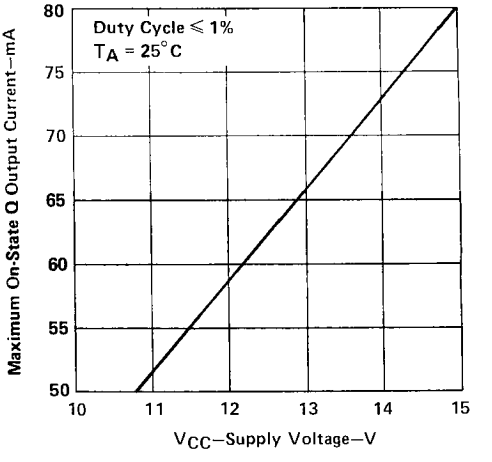
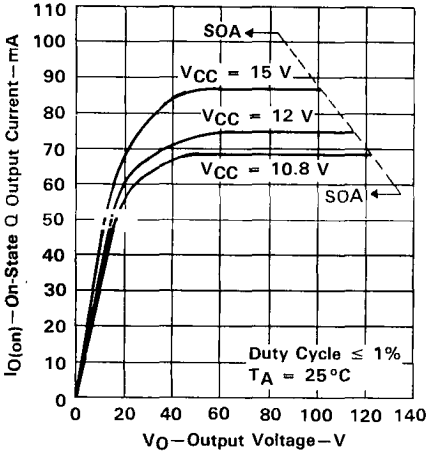


FIGURE 2

TYPICAL CHARACTERISTICS

ON-STATE Q OUTPUT CURRENT
vs
OUTPUT VOLTAGE



SOA = Safe Operating Area

FIGURE 3

OUTPUT SATURATION CURRENT
vs
FREE-AIR TEMPERATURE†

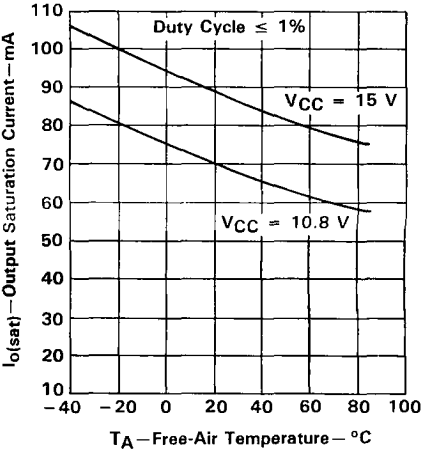


FIGURE 4

† Data for temperatures below 0°C and above 70°C apply only for SN65551 and SN65552.

PARAMETER MEASUREMENT INFORMATION

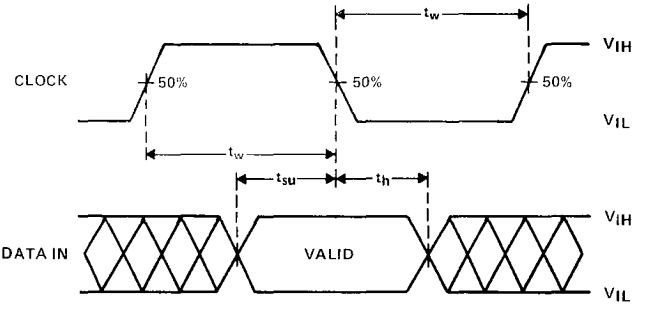


FIGURE 5. INPUT TIMING VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

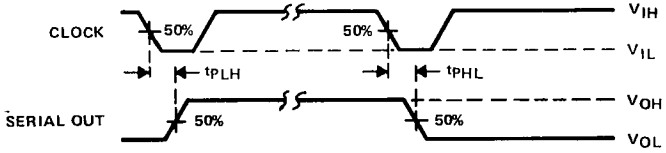


FIGURE 6. VOLTAGE WAVEFORMS, SERIAL OUTPUT

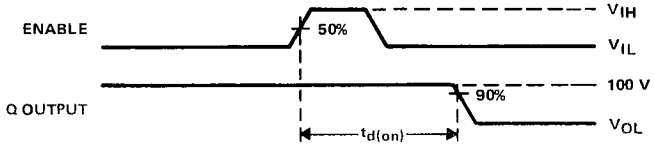


FIGURE 7. VOLTAGE WAVEFORMS, Q OUTPUT

D2744, MARCH 1983—REVISED DECEMBER 1989

- Each Device Drives 32 Electrodes
- 60-V Output Voltage Swing Capability
- 15-mA Output Source and Sink Current Capability
- High-Speed Serially-Shifted Data Input
- Totem-Pole Outputs
- Latches on All Driver Outputs

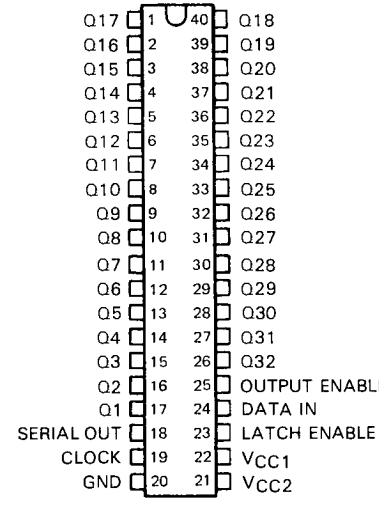
description

The SN65553, SN65554, SN75553, and SN75554 are monolithic BIDFET† integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN65554 and SN75554 output sequence is reversed from the SN65553 and SN75553 for ease in printed circuit board layout.

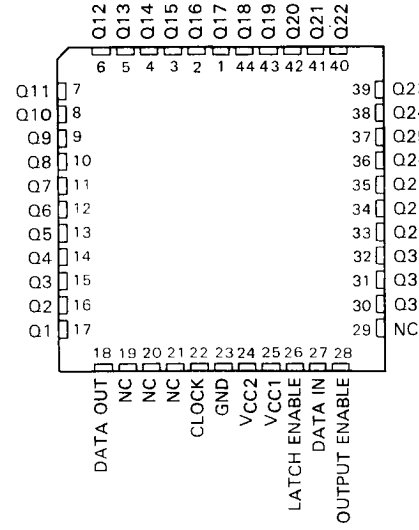
The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 32 latches. When OUTPUT ENABLE is high, all Q outputs are enabled. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by LATCH ENABLE or OUTPUT ENABLE.

The SN65553 and SN65554 are characterized for operation from −40°C to 85°C. The SN75553 and SN75554 are characterized for operation from 0°C to 70°C.

N PACKAGE
(TOP VIEW)
SN65553, SN75553



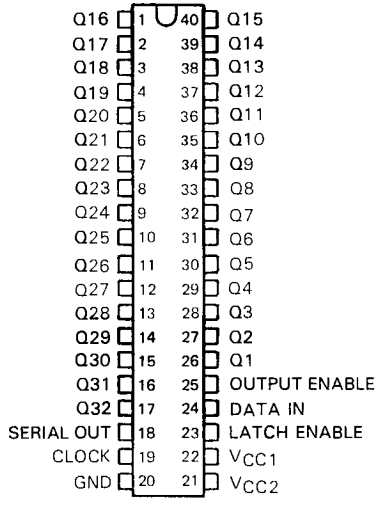
FN PACKAGE
(TOP VIEW)
SN65553, SN75553



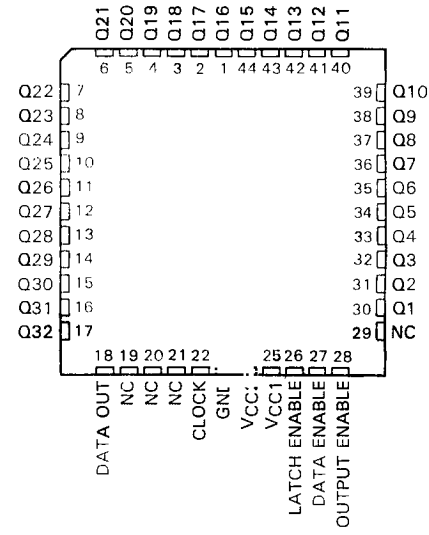
NC—No internal connection

†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

N PACKAGE
(TOP VIEW)
SN65554, SN75554



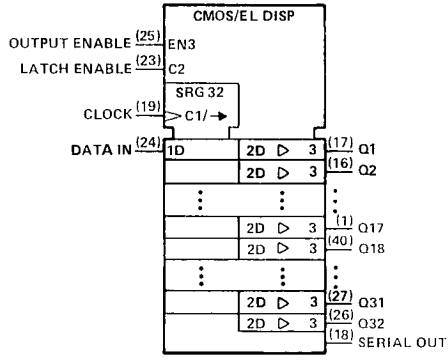
FN PACKAGE
(TOP VIEW)
SN65554, SN75554



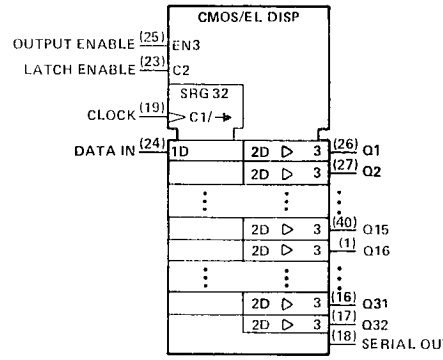
NC – No internal connection

logic symbols†

SN65553, SN75553

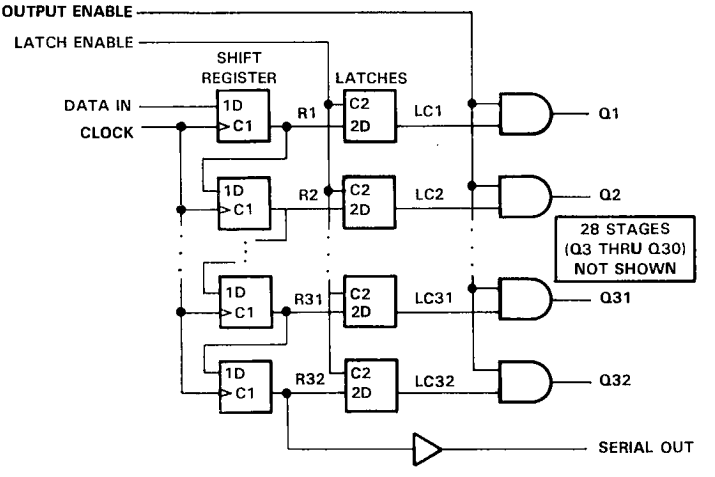


SN65554, SN75554



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12
Pin numbers shown are for N packages.

logic diagram (positive logic)

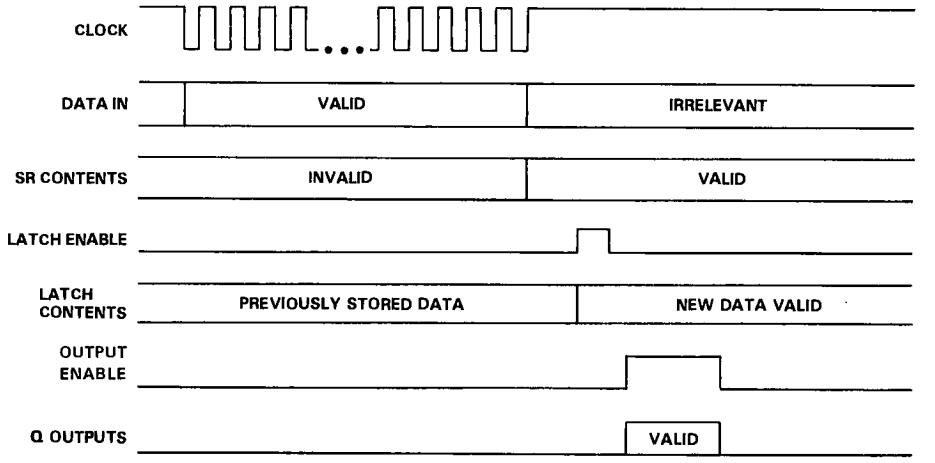


FUNCTION TABLE

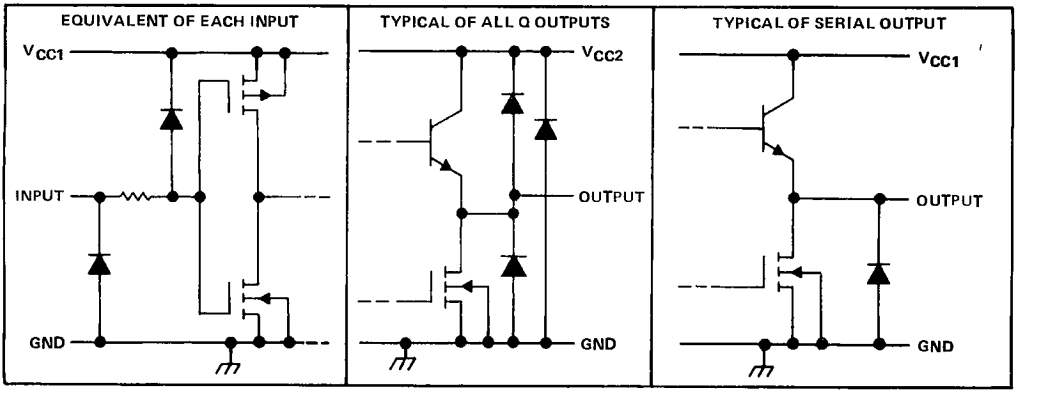
FUNCTION	CONTROL INPUTS			SHIFT REGISTER	LATCHES	OUTPUTS	
	CLOCK	LATCH ENABLE	OUTPUT ENABLE	R1 THRU R32	LC1 THRU LC32	SERIAL	Q1 THRU Q22
LOAD	↑	X	X	Load and shift†	Determined by	R32	Determined by
	Not↑	X	X	No change	LATCH ENABLE‡	R32	OUTPUT ENABLE
LATCH	X	L	X	As determined	Stored data	R32	Determined by
	X	H	X	above	New data	.	OUTPUT ENABLE
OUTPUT ENABLE	X	X	L	As determined	Determined by	.	All L
	X	X	H	above	LATCH ENABLE‡	R32	LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
†R32 and the serial output take on the state of R31, R31 takes on the state of R30, . . .R2 takes on the state of R1, and R1 takes on the state of the data input.
‡New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematic of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC2} . . . . . 70 V
Input voltage . . . . . V_{CC1} + 0.3 V
Ground current . . . . . 700 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65553, SN65554 . . . . . −40°C to 85°C
SN75553, SN75554 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1700 mW	13.6 mW/°C	mW	884 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	15	V
Supply voltage, V_{CC2}		0		60	V
High-level input voltage, V_{IH} (see Figure 1)	V_{CC1} = 10.8 V	8.1		11.1	V
	V_{CC1} = 15 V	11.25		15.3	
Low-level input voltage, V_{IL} (see Figure 1)	V_{CC1} = 10.8 V	−0.3		2.7	V
	V_{CC1} = 15 V	−0.3		3.75	
High-level output current, I_{OH}		−15			mA
Low-level output current, I_{OL}		15			mA
Output clamp current, I_{OK}				20	mA
Clock frequency, f_{clock}		0		6.25	MHz
Pulse duration, [illegible] high or low, $t_{w(CLK)}$ (see Figure 2)		80			ns
Pulse duration, [illegible] $t_{w(LE)}$ (see Figure 4)		80			ns
Data setup time before CL[illegible], t_{su} (see Figure 2)		20			ns
Data hold time after CLOCK ↑, t_h (see Figure 2)		80			ns
Operating free-air temperature, T_A	[illegible]553 [illegible]554	−40		85	°C
	[illegible] SN75554	0		70	

electrical characteristics over recommended ranges of V_{CC1} and operating free-air temperature, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = −15 mA	57		V
		SERIAL OUT	I_O = −100 μA	V_{CC1}−1.5		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 15 mA		8	V
		SERIAL OUT	I_{OL} = 100 μA		1	
I_{IH}	High-level input current		$V_I = V_{CC1}$		1	μA
I_{IL}	Low-level input current		V_I = 0		−1	μA
I_{CC1}	Supply current from V_{CC1}				5	mA
I_{CC2}	Supply current from V_{CC2}	[illegible]553 [illegible]554			12	mA
		[illegible] SN75554			10	

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level SERIAL OUT from CLOCK	C_L = 20 pF to ground, See Figure 3		140	ns
t_{PLH}	Propagation delay time, low-to-high-level SERIAL OUT from CLOCK			140	ns
t_{DHL}	Delay time, high-to-low-level Q output from LATCH ENABLE	C_L = 20 pF to ground, See Figure 4		500	ns
t_{DLH}	Delay time, low-to-high-level Q output from LATCH ENABLE	C_L = 20 pF to ground, See Figure 4		1	μs

RECOMMENDED OPERATION CONDITIONS

INPUT VOLTAGE LOGIC-LEVEL LIMITS
vs
SUPPLY VOLTAGE V_{CC1}

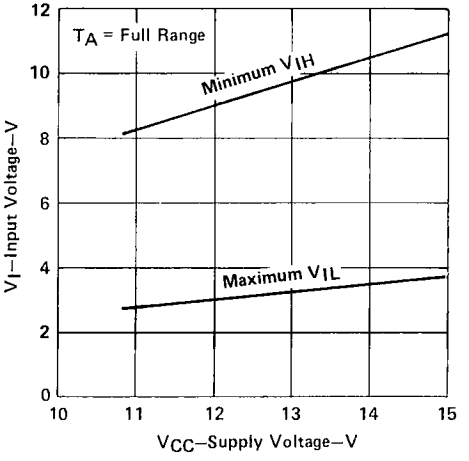


FIGURE 1

PARAMETER MEASUREMENT INFORMATION

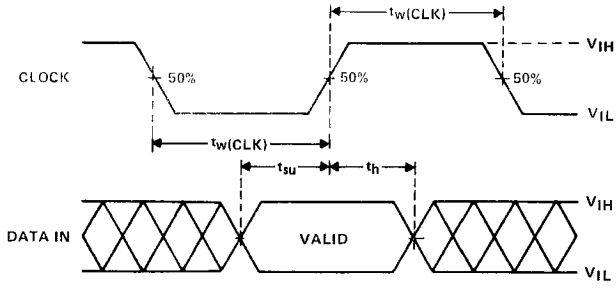


FIGURE 2. INPUT TIMING VOLTAGE WAVEFORMS

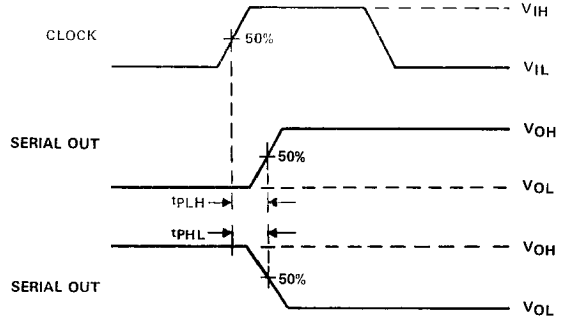


FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY CLOCK TO SERIAL OUTPUT

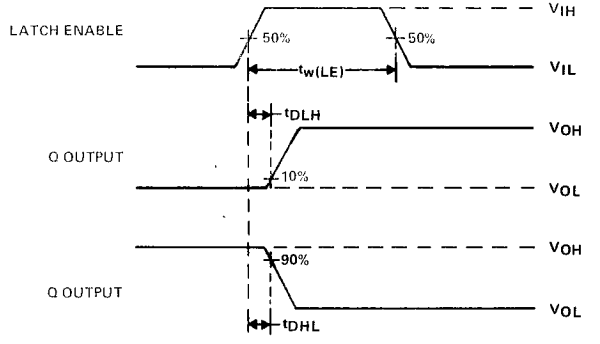


FIGURE 4. VOLTAGE WAVEFORMS FOR DELAY TIMES, LATCH ENABLE TO Q OUTPUTS

D2744, APRIL 1985—REVISED JULY 1990

- Each Device Drives 32 Electrodes
- 90-V Output Voltage Swing Capability Using Ramped Supply
- 15-mA Output Source and Sink Current Capability
- High-Speed Serially-Shifted Data Input
- Totem-Pole Outputs
- Latches on All Driver Outputs

description

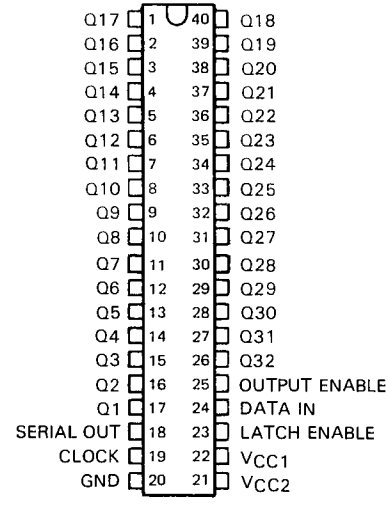
The SN65555, SN75555, SN65556, and SN75556 are monolithic BIDFET† integrated circuits designed to drive the column electrodes of an electro-luminescent display. The SN65556 and SN75556 output sequence is reversed from the SN65555 and SN75555 for ease in printed circuit board layout.

The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 32 latches. When OUTPUT ENABLE is high, all Q outputs are enabled. Data must be loaded into the latches and OUTPUT ENABLE must be high before supply voltage V_{CC2} is ramped up.

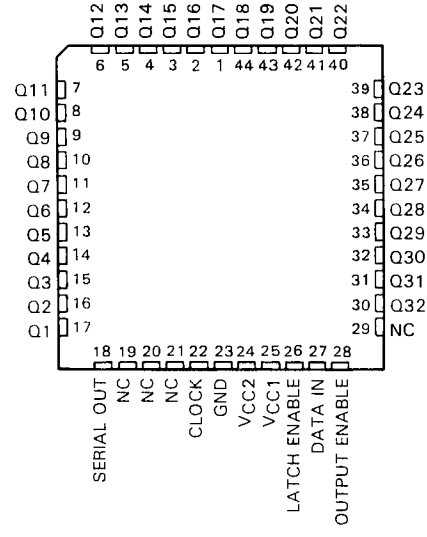
Serial data output from the shift register may be used to cascade shift registers. This output is not affected by LATCH ENABLE or OUTPUT ENABLE.

The SN65555 and SN65556 are characterized for operation from −40°C to 85°C. The SN75555 and SN75556 are characterized for operation from 0°C to 70°C.

SN65555, SN75555
N PACKAGE
(TOP VIEW)



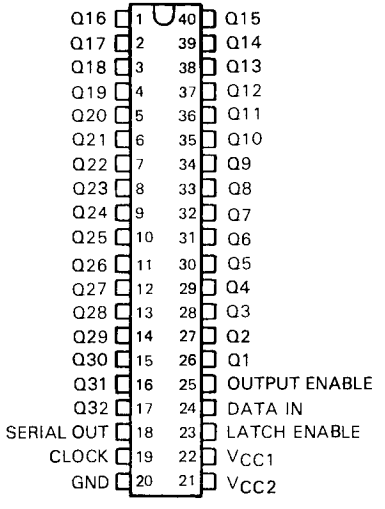
SN65555, SN75555
FN PACKAGE
(TOP VIEW)



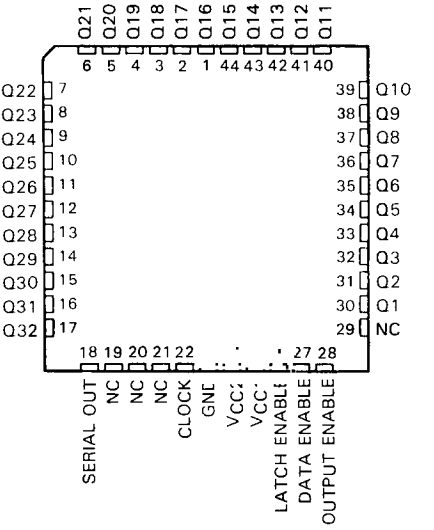
NC—No internal connection

†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

SN65556, SN75556
N PACKAGE
(TOP VIEW)



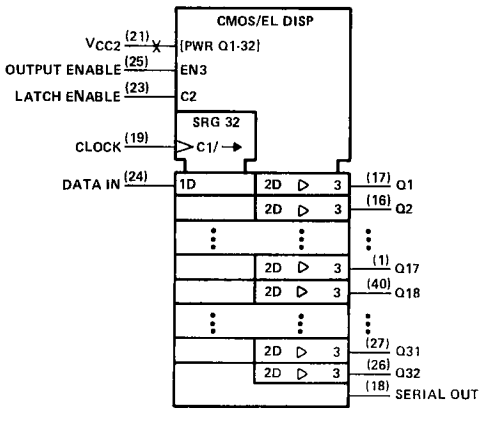
SN65556, SN75556
FN PACKAGE
(TOP VIEW)



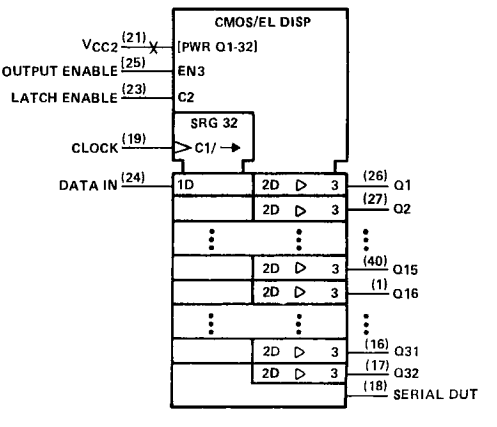
NC—No internal connection

logic symbols†

SN65555, SN75555

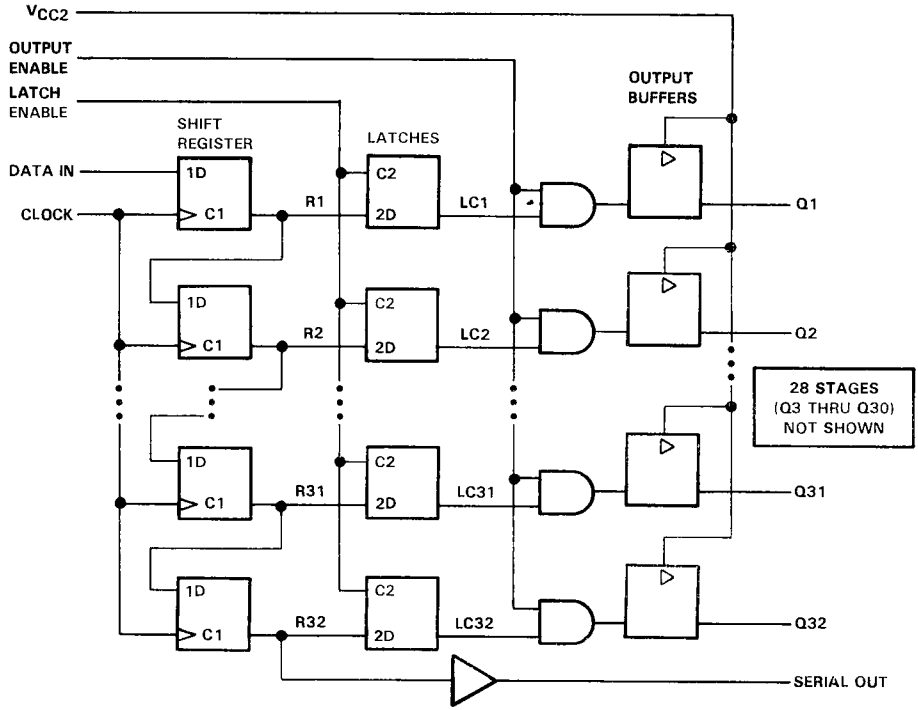


SN65556, SN75556



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbars shown are for N packages.

logic diagram (positive logic)

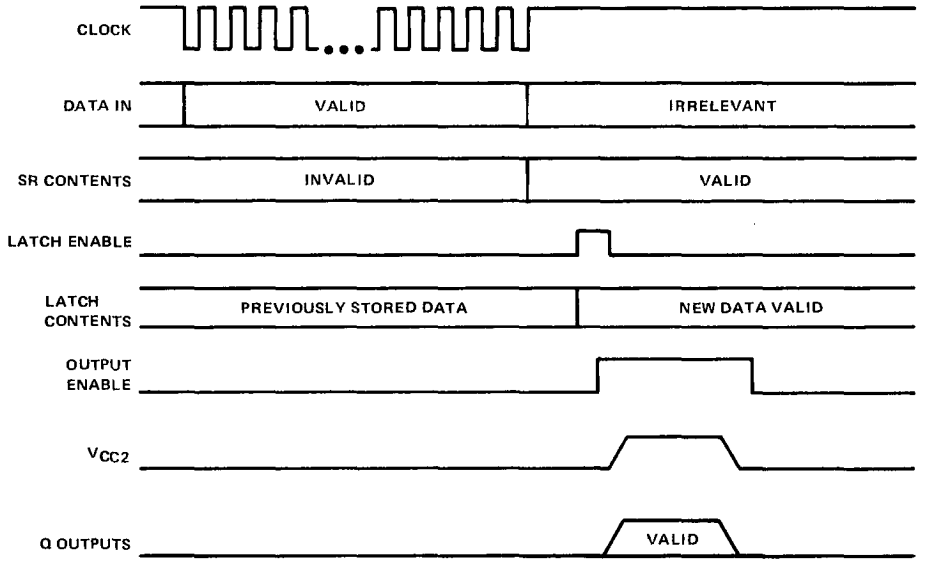


FUNCTION TABLE

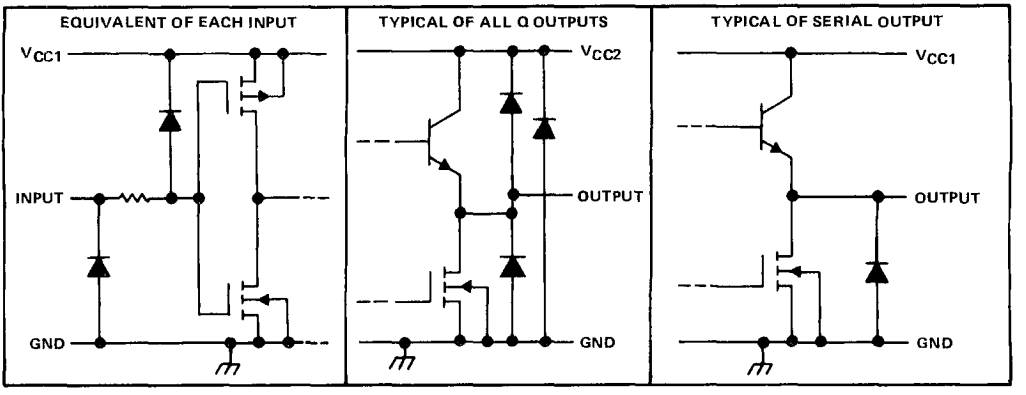
FUNCTION	CONTROL INPUTS			SHIFT REGISTER	LATCHES	OUTPUTS	
	CLOCK	LATCH ENABLE	OUTPUT ENABLE	R1 THRU R32	LC1 THRU LC32	SERIAL	Q1 THRU Q32
LOAD	↑	X	X	Load and shift†	Determined by LATCH ENABLE‡	R32	Determined by OUTPUT ENABLE
	Not↑	X	X	No change			
LATCH	X	L	X	As determined above	Stored data	R32	Determined by OUTPUT ENABLE
	X	H	X		New data		
OUTPUT ENABLE	X	X	L	As determined above	Determined by LATCH ENABLE‡	R32	All L
	X	X	H			R32	LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
†R32 and the serial output take on the state of R31, R31 takes on the state of R30,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.
‡New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematic of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC2} (see Note 2) . . . . . 90 V
Input voltage . . . . . V_{CC1} + 0.3 V
Ground current . . . . . 700 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65555, SN65556 . . . . . −40°C to 85°C
SN75555, SN75556 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. These devices have been designed to be used in applications in which the high-voltage supply, V_{CC2}, is switched to ground before changing the state of the outputs.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1700 mW	13.6 mW/°C	1088 mW	884 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage		10.8	12	15	V
V_{CC2}	Supply voltage		0		80	V
V_{IH}	High-level input voltage (see Figure 1)	V_{CC1} = 10.8 V	8.1		11.1	V
		V_{CC1} = 15 V	11.25		15.3	
V_{IL}	Low-level input voltage (see Figure 1)	V_{CC1} = 10.8 V	−0.3†		2.7	V
		V_{CC1} = 15 V	−0.3†		3.75	
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current				15	mA
I_{OK}	Output clamp current				20	mA
f_{clock}	Clock frequency		0		6.25	MHz
$t_{w(CLK)}$	Pulse duration, CLOCK or low (see Figure 2)		80			ns
$t_{w(LE)}$	Pulse duration, LATCH ENABLE		80			ns
t_{su}	Setup time	DATA IN before CLOCK↑ (see Figure 2)	20			ns
		OUTPUT ENABLE ↓ before V_{CC2}↑ (see Figure 4)	500			
t_h	Hold time	DATA IN after CLOCK ↑ (see Figure 2)	80			ns
		OUTPUT ENABLE after V_{CC2}↑ (see Figure 4)	100			
dv/dt	Rate of rise for V_{CC2}				80	V/μs
T_A	Operating free-air temperature	SN65555, SN65556	−40		85	°C
		SN75555, SN75556	0		70	

†The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 12 V, V_{CC2} = 80 V

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = −15 mA	77		V
		SERIAL OUT	I_O = −100 μA	10.5		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 15 mA		8	V
		SERIAL OUT	I_{OL} = 100 μA		1	
I_{IH}	High-level input current		V_I = 12 V		1	μA
I_{IL}	Low-level input current		V_I = 0		−1	μA
I_{CC1}	Supply current from V_{CC1}				2	mA
I_{CC2}	Supply current from V_{CC2}				5	mA

switching characteristics, V_{CC1} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level SERIAL OUT from CLOCK	C_L = 20 pF to ground, V_{CC2} = 0, See Figure 3		140	ns
t_{PLH}	Propagation delay time, low-to-high-level SERIAL OUT from CLOCK			140	ns
t_d	Delay time, V_{CC2} to Q outputs	dv/dt = 80 V/μs, See Figure 4		100	ns

RECOMMENDED OPERATION CONDITIONS

INPUT VOLTAGE LOGIC-LEVEL LIMITS
vs
SUPPLY VOLTAGE V_{CC1}

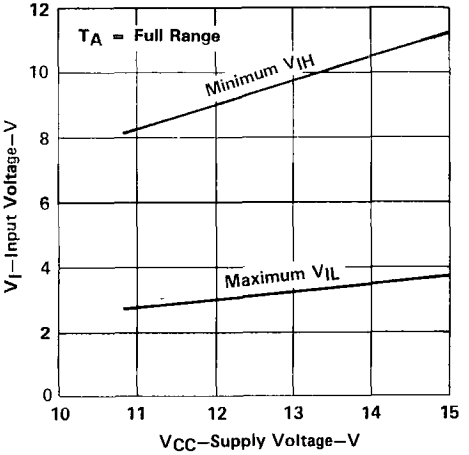


FIGURE 1

PARAMETER MEASUREMENT INFORMATION

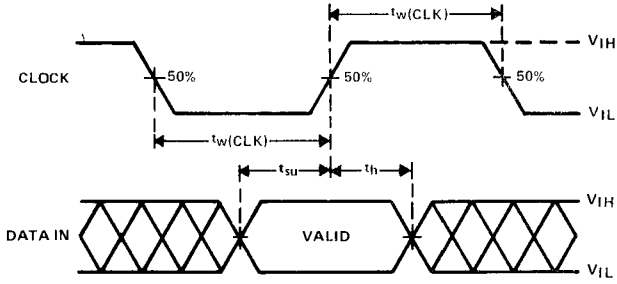


FIGURE 2. INPUT TIMING VOLTAGE WAVEFORMS

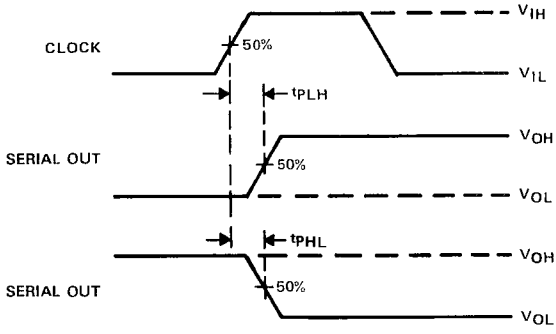


FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY CLOCK TO SERIAL OUTPUT

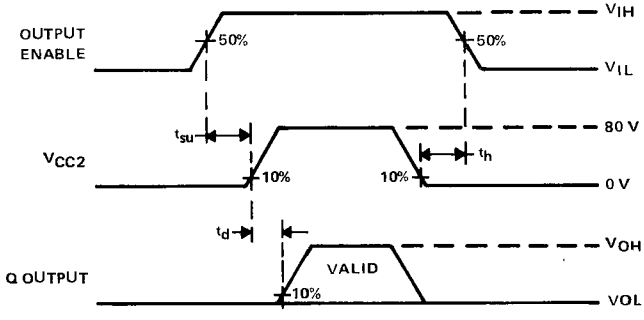
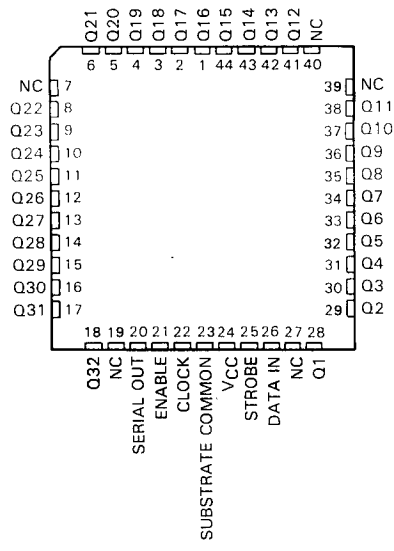


FIGURE 4. VOLTAGE WAVEFORMS FOR DELAY TIMES, V_{CC2} TO Q OUTPUTS

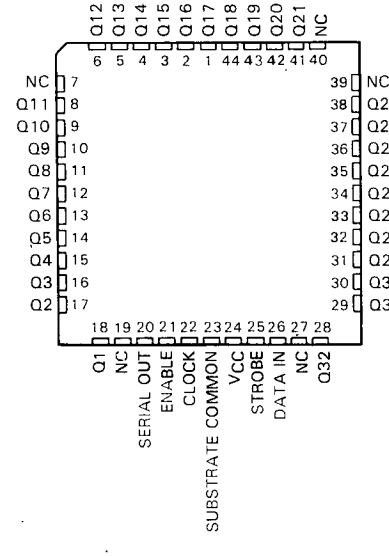
D2999, DECEMBER 1985—REVISED OCTOBER 1989

- Each Device Drives 32 Electrodes
- High-Voltage Open-Collector N-P-N Outputs Using Ramped Supply
- 300-mA Output Current Capability
- CMOS-Compatible Inputs
- Very Low Steady-State Power Consumption

SN65557, SN75557 . . . FN PACKAGE
(TOP VIEW)



SN65558, SN75558 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

These devices are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS-compatible and all outputs are high-voltage open-collector n-p-n transistors. The SN65558 and SN75558 output sequences are reversed from the SN65557 and SN75557 for ease in printed circuit board layout.

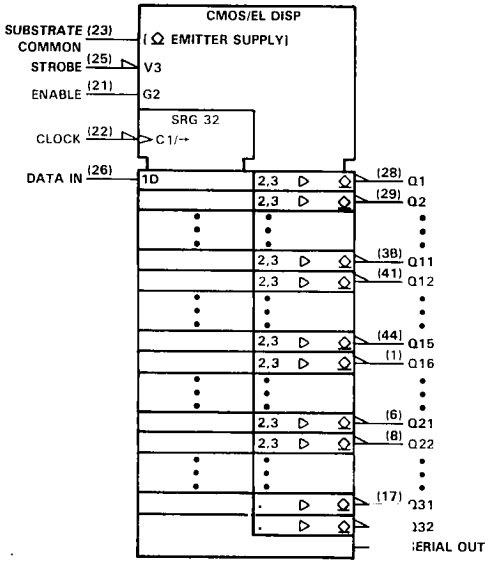
The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to the SUBSTRATE COMMON terminal. Serial data is entered into the shift register on the high-to-low transition of the clock input. A high ENABLE allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When STROBE is low, all output transistors are turned on. The Serial Data output (SERIAL OUT) from the shift register may be used to cascade additional devices. This output is not affected by the ENABLE or STRDBE inputs.

The SN65557 and SN65558 are characterized for operation from −40°C to 85°C. The SN75557 and SN75558 are characterized for operation from 0°C to 70°C.

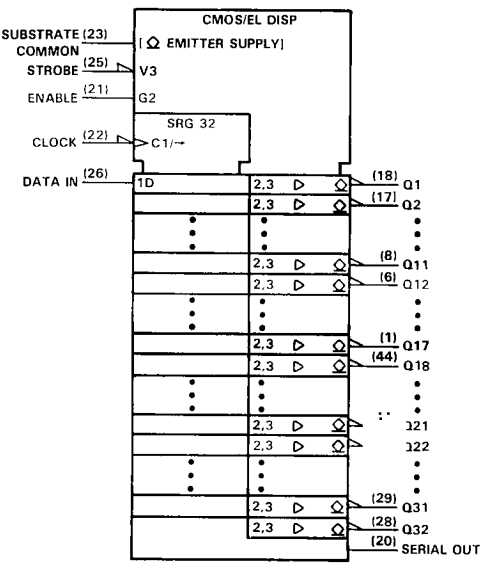
† BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip patented process

logic symbols†

SN65557, SN75557

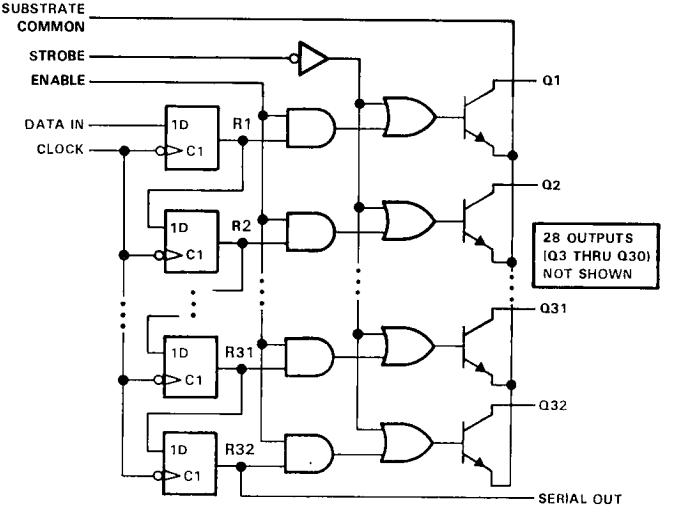


SN65558, SN75558



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

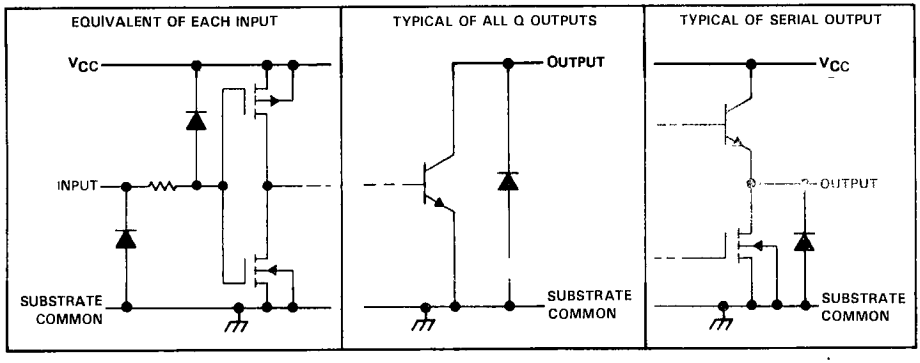


FUNCTION TABLE

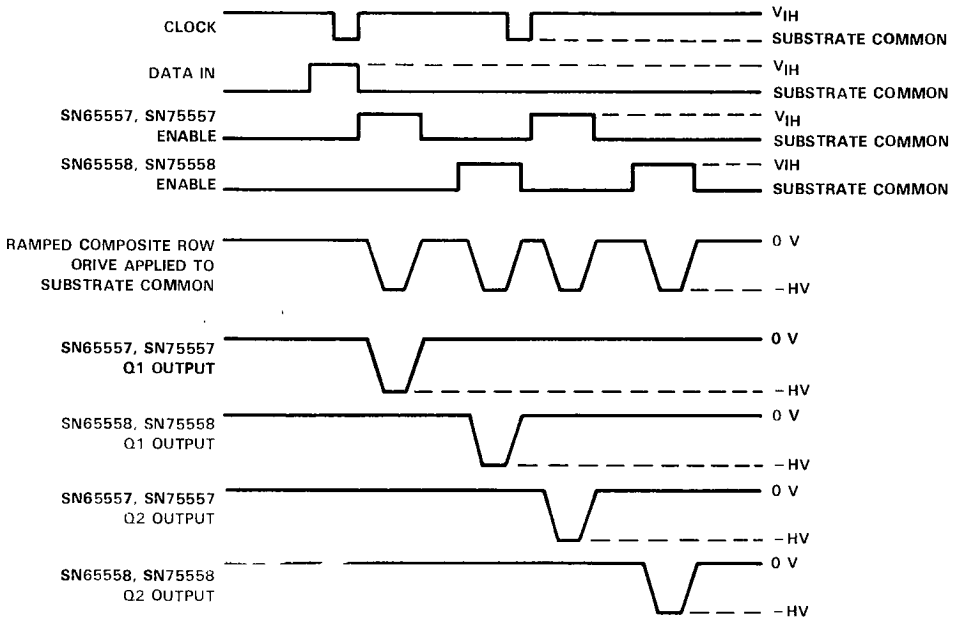
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS	OUTPUTS	
	CLOCK	ENABLE	STROBE	R1 THRU R32	SERIAL	Q1 THRU Q32
LOAD	↓	X	X	Load and Shift†	.	Determined by ENABLE and STROBE
	No ↓	X	X	No Change	R32	Determined by ENABLE and STROBE
ENABLE	X	L	H	As determined above	R32	All Q outputs off
	X	H	H	As determined above	R32	Determined by R1 through R32
$\overline{S}$ . . .	X	X	L	As determined above	R32	All Q outputs on

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition.
†Register R32 takes on the state of R31, R31 takes on the state of R30, . . .R2 takes on the state of R1, and R1 takes on the state of the data input.

schematics of inputs and outputs



typical operating sequence



HV = High voltage

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Off-state output voltage, $V_{O(off)}$ (see Note 2) . . . . . 110 V
Input voltage . . . . . V_{CC}+0.3 V
Substrate common terminal current (see Note 3) . . . . . 750 mA
Continuous total power dissipation at (or below)
25°C free-air temperature (see Note 4) . . . . . 1700 mW
Operating free-air temperature range: SN65557, SN65558 . . . . . −40°C to 85°C
SN75557, SN75558 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to SUBSTRATE COMMON terminal.
2. Data must be clocked into the shift register and Q outputs enabled prior to ramping SUBSTRATE COMMON to −HV (see typical operating sequence).
3. Duty cycle is limited by package dissipation.
4. For operation above 25°C free-air temperature, derate linearly to 1088 mW at 70°C, and 884 mW at 85°C at the rate of 13.6 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			10.8	12	15	V
High-level input voltage, V_{IH} (see Figure 1)		V_{CC} = 10.8 V	8.1		11.1	V
		V_{CC} = 15 V	11.25		15.3	
Low-level input voltage, V_{IL} (see Figure 1)		V_{CC} = 10.8 V	−0.3		2.7	V
		V_{CC} = 15 V	−0.3		3.75	
Off-state Q output voltage, $V_{O(off)}$			−0.3		100	V
On-state Q output current, $I_{O(on)}$, duty cycle ≤ 1%, V_{CC} = 15 V						mA
Rate of rise for SUBSTRATE COMMON, dV/dt (see Figure 4)						V/μs
Clock frequency, f_{clock}			0		4	MHz
Pulse duration, CLOCK high or low, t_w			125			ns
Setup time, t_{su}	DATA IN before CLOCK↓ (see Figure 2)		50			ns
	ENABLE before SUBSTRATE COMMON ↓ (see Figure 4)					
Hold time, t_h, DATA IN after CLOCK↓ (see Figure 2)						ns
Operating free-air temperature, T_A		SN65557, SN65558	−40		85	°C
		SN75557, SN75558	0		70	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 12 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN65557 SN65558		SN75557 SN75558		UNIT
				MIN	MAX	MIN	MAX	
$I_{O(off)}$	Off-state Q output current		V_O = [illegible] V		20		10	μA
V_{OH}	High-level output voltage	Serial outputs	I_O = [illegible] μA	10.5		10.5		V
V_{VOL}	Low-level output voltage	Q outputs	I_{OL} = 300 mA		20		10	V
		Serial output	I_{OL} = 100 μA		1		1	
I_{IH}	High-level input current		V_I = 12 V		1		1	μA
I_{IL}	Low-level input current		V_I = 0		−1		−1	μA
I_{CC}	Supply current from V_{CC}				[illegible]		250	μA

switching characteristics, V_{CC} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level SERIAL OUTPUT from CLOCK	C_L = 20 pF to SUBSTRATE COMMON (see Figure 3)		200	ns
t_{PLH}	Propagation delay time, low-to-high-level SERIAL OUTPUT from CLOCK			200	ns
$t_{d(on)}$	Turn-on delay time, Q outputs from ENABLE	dV/dt = 100 V/μs, STROBE at V_{CC}, R_L = 2 kΩ to 60 V (see Figure 4)		500	ns

RECOMMENDED OPERATING CONDITIONS

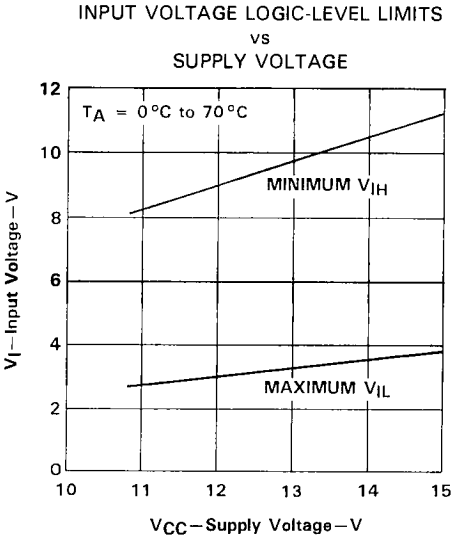


FIGURE 1

TEXAS INSTRUMENTS
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PARAMETER MEASUREMENT INFORMATION

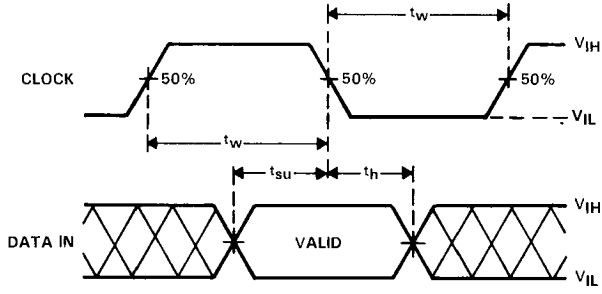

FIGURE 2. INPUT TIMING VOLTAGE WAVEFORMS

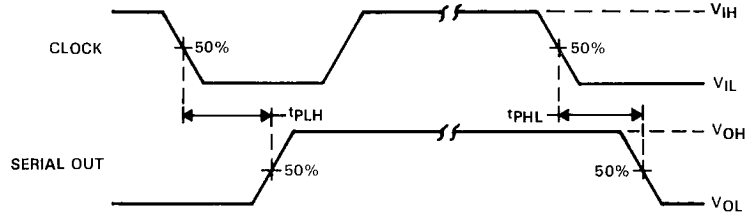

FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY TIMES, CLOCK TO DATA OUT

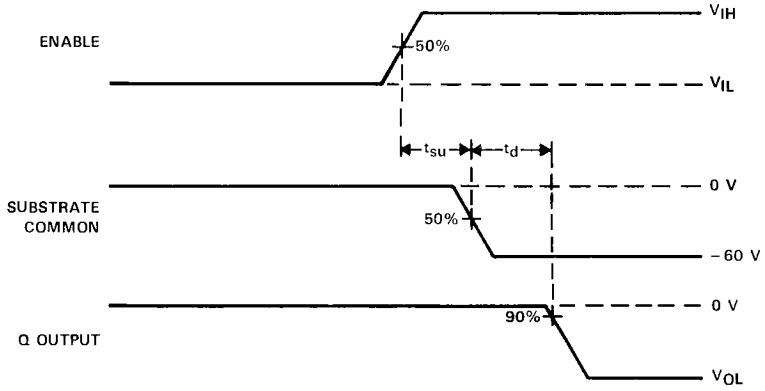

FIGURE 4. VOLTAGE WAVEFORMS FOR TURN ON DELAY TIME, SUBSTRATE COMMON TO Q OUTPUT

TYPICAL CHARACTERISTICS

ON-STATE Q OUTPUT CURRENT
vs
ON-STATE Q OUTPUT VOLTAGE

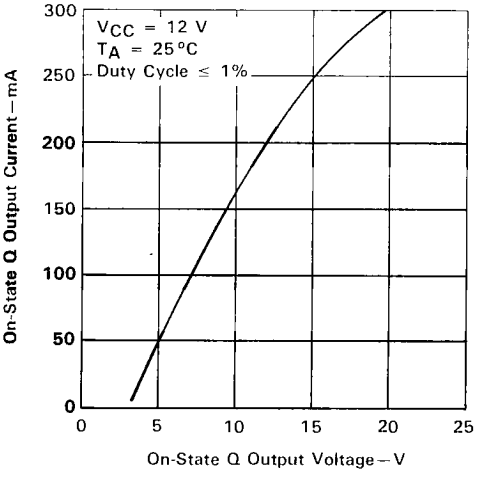

FIGURE 5

TEXAS INSTRUMENTS
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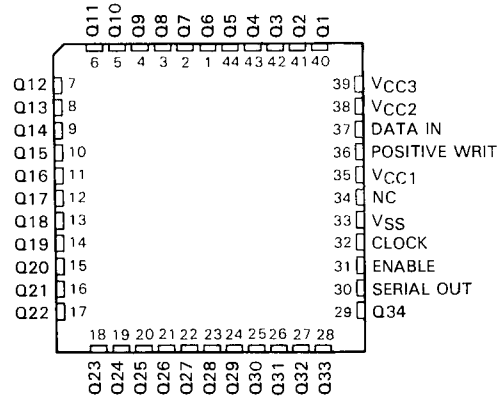
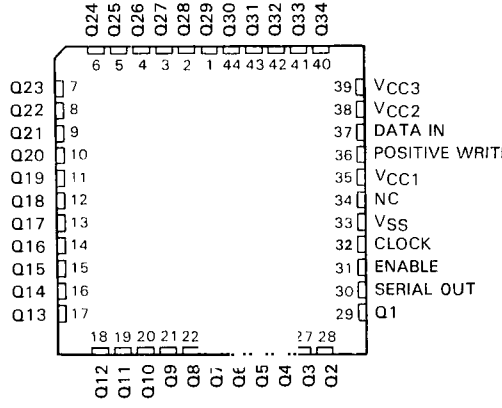
D3223, MAY 1986–REVISED DECEMBER 1989

- Each Device Drives 34 Electrodes
- Selectable Open-Source or Open-Drain Output
- Outputs Rated at 240 V
- Output Current Capability:
  - −150 mA to 100 mA (SN65')
  - −150 mA to 120 mA (SN75')
- CMOS-Compatible Inputs
- Very Low Steady-State Power Consumption

SN65563A, SN75563A . . . FN PACKAGE
(TOP VIEW)



SN65564A, SN75564A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN65563A, SN65564A, SN75563A, and SN75564A are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS compatible. If POSITIVE WRITE is high, the Q outputs act like open-source outputs and output data is not inverted with respect to input data. If POSITIVE WRITE is low, the Q outputs act like open-drain outputs and output data is inverted with respect to input data. The SN65564A and SN75564A output sequences are reversed from the SN65563A and SN75563A for ease in printed circuit board layout.

Typically, composite V_{CC2}, V_{CC3}, and ground signals are externally generated by a high-voltage switching circuit. Serial data is entered into the shift register on the high-to-low transition of CLOCK. A high at the ENABLE input allows those outputs with a high in their associated register to be turned on, causing the corresponding row to be connected to V_{CC2} when POSITIVE WRITE is high or to ground when POSITIVE WRITE is low. V_{CC3} may be tied to V_{CC2} or held 5 V to 15 V above V_{CC2} for better V_{OH} characteristics. SERIAL OUTPUT from the shift register may be used to cascade additional devices. This output is not affected by the ENABLE or POSITIVE WRITE inputs.

The SN65563A and SN65564A are characterized for operation over the full automotive operating temperature range of −40°C to 85°C. The SN75563A and SN75564A are characterized for operation from 0°C to 70°C.

†BIDFET-Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip — Patented Process

LOAD FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTER	OUTPUTS	
	CLOCK	ENABLE	POSITIVE WRITE	R1 THRU R34	SERIAL	Q1 THRU Q34
LOAD	↓	X	X	Load and Shift†	R34	Determined by ENABLE and POSITIVE WRITE
	No↓	X	X	No Change	R34	Determined by ENABLE and POSITIVE WRITE

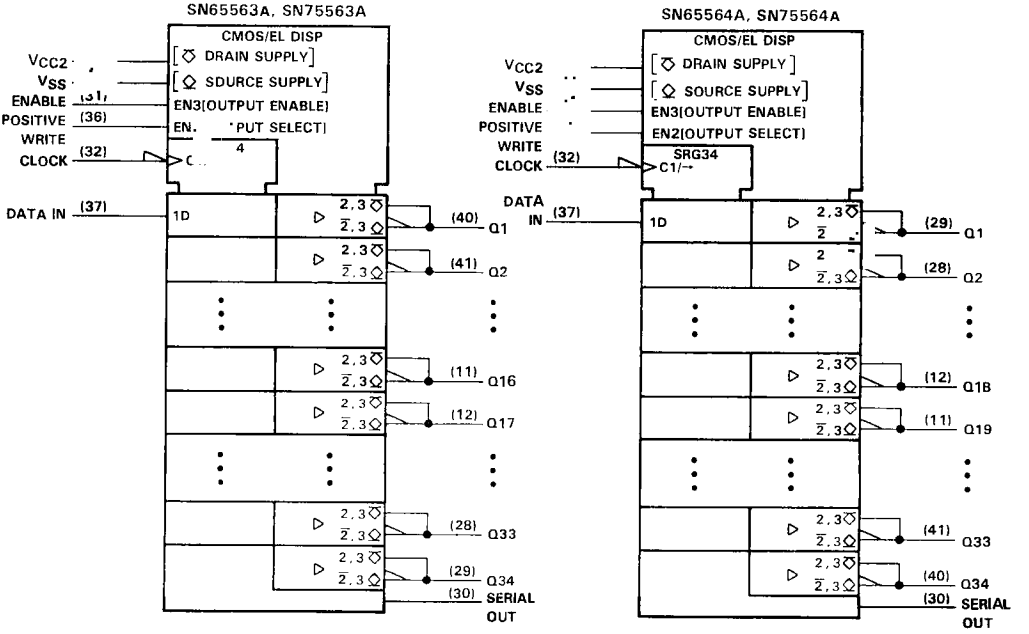
†Register R34 takes on the state of R33, R33 takes on the state of R32, . . . R2 takes on the state of R1, R1 takes on the state of the data input.

OUTPUT CONTROL FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTER CONTENTS Rn FOR R1 THRU R34 (Determined Above)	OUTPUTS	
	CLOCK	ENABLE	POSITIVE WRITE		SERIAL	Q1 THRU Q34
OUTPUT CONTROL	X	L	X	X	R34	High-Impedance
	X	H	H	H	R34	H
	X	H	L	H	R34	L
	X	X	X	L	R34	High-Impedance

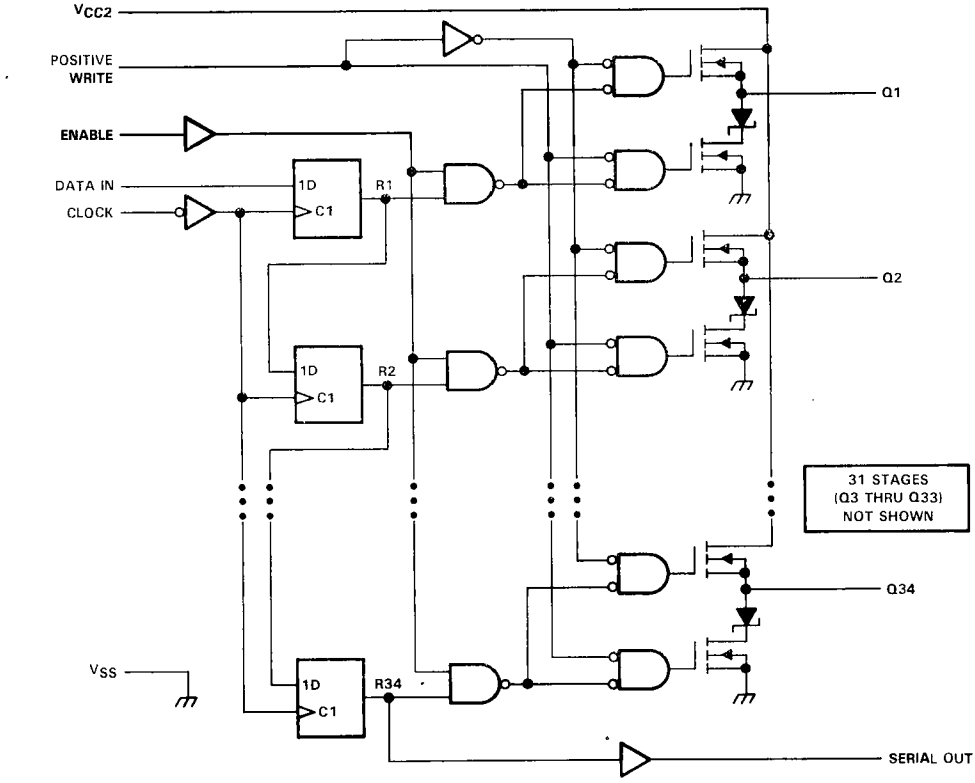
H = high, L = low, X = irrelevant, ↓ = high-to-low transition

schematics of inputs and outputs

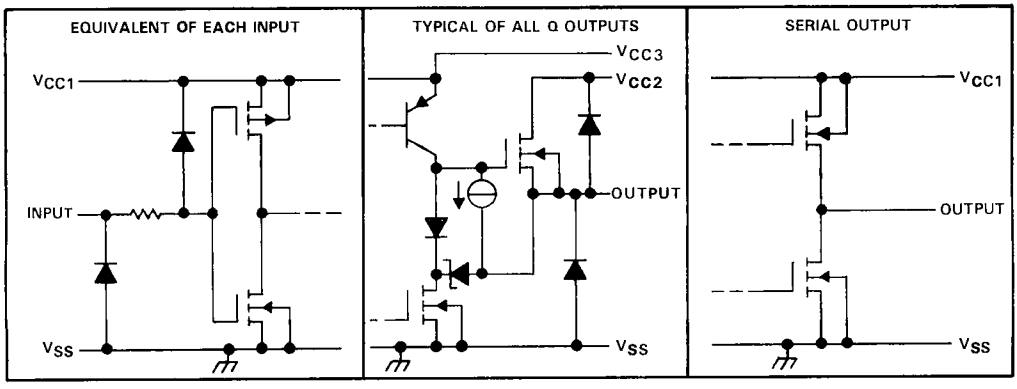


‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

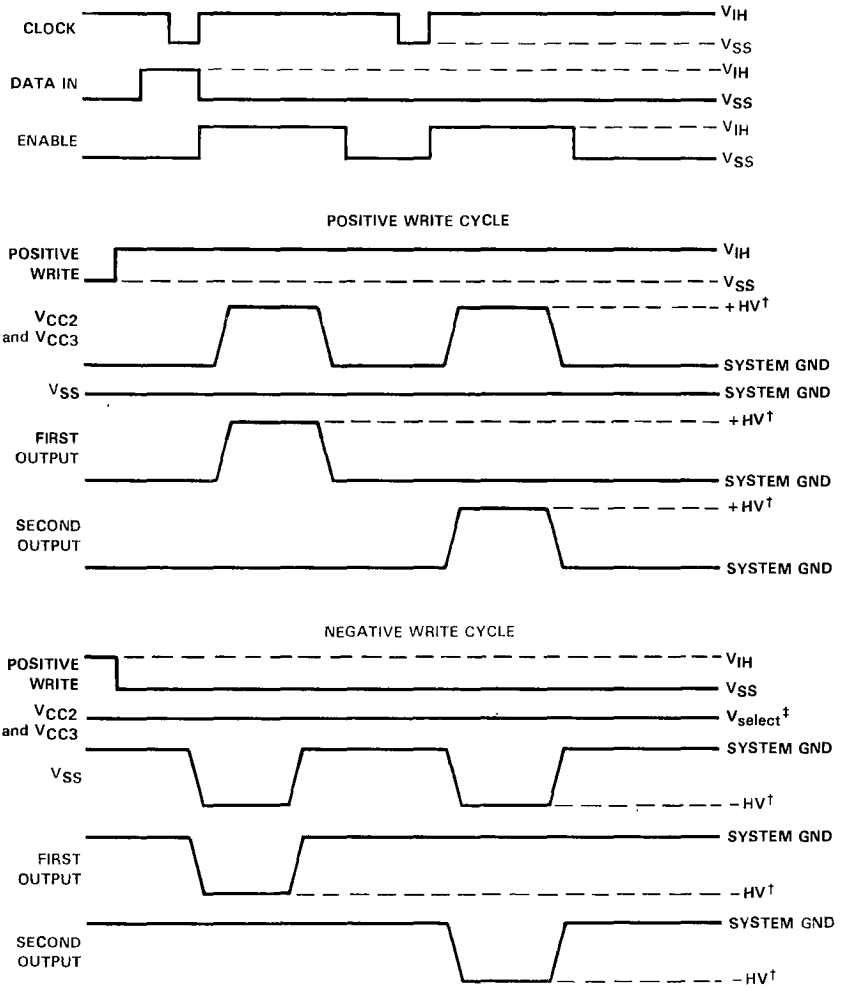
logic diagram (positive logic)



schematics of inputs and outputs



typical operating sequence



†HV = high voltage
‡During the negative write cycle, the V_{CC2} and V_{CC3} supplies are in a high-impedance state.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperture range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 240 V
Supply voltage, V_{CC3} . . . . . 240 V
Supply voltage, V_{SS} . . . . . −240 V
Input voltage . . . . . −0.3 V to V_{CC1} + 0.3 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1700 mW
Operating free-air temperature range: SN65563A, SN65564A . . . . . −40°C to 85°C
SN75563A, SN75564A . . . . . 0°C to 70°C
Storage temperature range . . . . . −40°C to 125°C
Case temperature for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to V_{SS}.
2. For operation above 25°C free-air temperature, derate to 1088 mW at 70°C or 884 mW at 85°C at the rate of 13.6 mW/°C.

recommended operating conditions (see Note 1, Figure 1, and Figure 2)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		7.5	12	13.2	V
Supply voltage, V_{CC2}		$V_{CC3}-15$		V_{CC3}	V
Supply voltage, V_{CC3}		0		235	V
Supply voltage, V_{SS}		0		−235	V
High-level input voltage, V_{IH}		0.[illegible]21		$V_{CC1}+0.3$	V
Low-level input voltage, V_{IL}†		−0.3		$0.25V_{CC1}$	V
High-level output current, I_{OH}	[illegible]64A			−	mA
	[illegible]64A			−	
Low-level output current, I_{OL}				150	mA
Output clamp current, I_{OK}				±150	mA
Clock frequency, f_{clock}				4	MHz
Pulse duration, CLOCK high or low, t_{wCLK}		[illegible]			ns
Setup time, DATA IN high or low before CLOCK↓, t_{su1}		[illegible]			ns
Setup time, CLOCK low before V_{CC2}↑ or V_{SS}↓, t_{su2}		300			ns
Setup time, [illegible] high before V_{CC2}↑ or V_{SS}↓, t_{su3}		300			ns
Setup time, [illegible] WRITE high or low before V_{CC2}↑ or V_{SS}↓, t_{su4}		300			ns
Hold time, DATA IN high or low after CLOCK↓, t_{h1}		100			ns
Hold time, CLOCK high after V_{CC2}↓ or V_{SS}↑, t_{h2}		300			ns
Hold time, ENABLE high after V_{CC2}↓ or V_{SS}↑, t_{h3}		0			ns
Hold time, POSITIVE WRITE after V_{CC2}↓ or [illegible] t_{h4}		0			ns
Hold time, ENABLE low between successive [illegible] t_{h5}	[illegible]64A	12			μs
	SN75[illegible]64A	10			
Hold time, E[illegible] low between successive [illegible] t_{h6}		300			ns
Operating free-air temperature, T_A	SN65[illegible], SN65564A	−40		85	°C
	SN75563A, SN75564A	0		70	

†The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating ranges of V_{CC1} and free-air temperature range, V_{CC2} = 235 V, V_{CC3} = 235 V, V_{SS} = 0 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$I_{O(off)}$	Off-state Q output current		V_O = 235 V		50	μA
			V_O = 0		−50	
V_{OH}	High-level output voltage	Q outputs	I_O = −70 mA	V_{CC2} − 30		V
		SERIAL OUT	I_O = −100 μA, V_{CC1} = 12 V	10.5		
V_{OL}	Low-level output voltage	Q outputs	I_O = 150 mA		30	V
		SERIAL OUT	I_O = 100 μA		1	
I_{IH}	High-level input current		V_{IH} = V_{CC1}		100	μA
I_{IL}	Low-level input current		V_{IL} = 0		−100	μA
I_{CC1}	Supply current from V_{CC1}		One Q output high		4	mA
			All Q outputs low or high impedance		2	
I_{CC3}	Supply current from V_{CC3}		One Q output high		10	mA
			All Q outputs low or high impedance		200	μA

switching characteristics operating range of V_{CC1}, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level serial output from clock	C_L = 50 pF to V_{SS}, See Figures 3 and 4		400	ns
t_{PHL}	Propagation delay time, high-to-low level serial output from clock			400	ns

PARAMETER MEASUREMENT INFORMATION

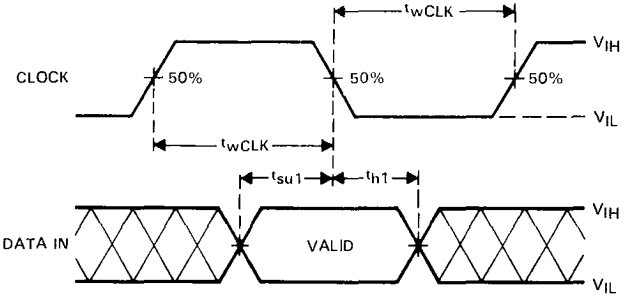

FIGURE 1. INPUT TIMING VOLTAGE WAVEFORMS

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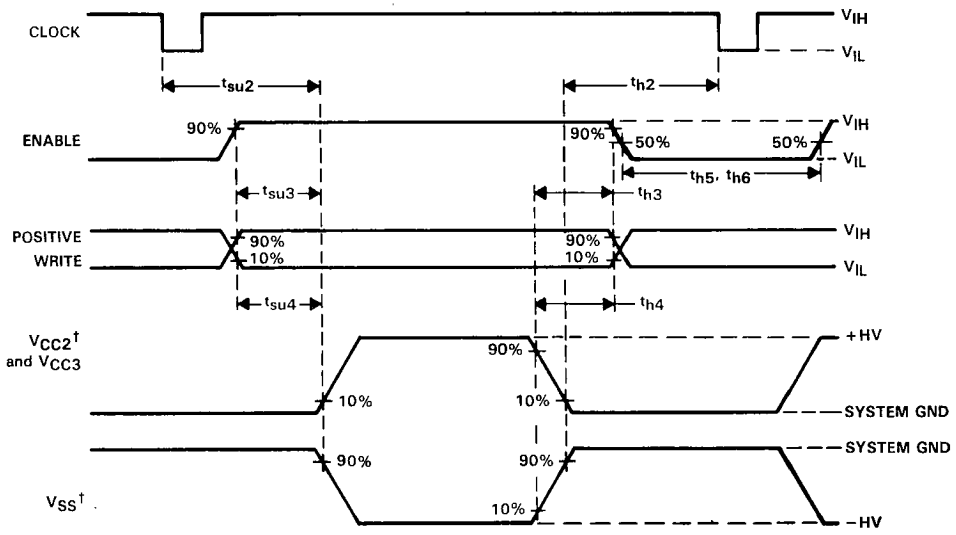
PARAMETER MEASUREMENT INFORMATION



†Timing waveforms are with respect to V_{CC2} or V_{SS}, as appropriate.

FIGURE 2. CONTROL INPUT TIMING VOLTAGE WAVEFORMS

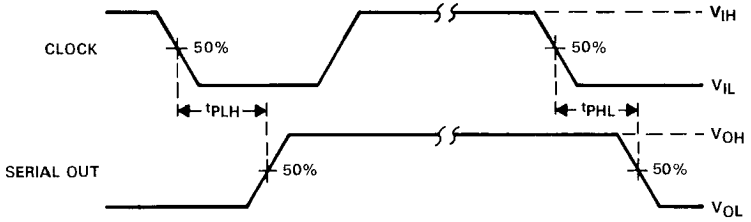


FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY TIMES, CLOCK TO DATA OUT

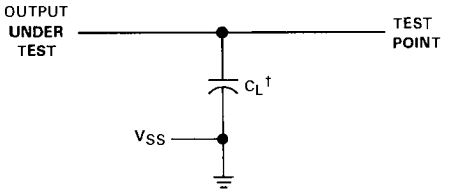


FIGURE 4. LOAD CIRCUIT

†C_L includes probe and jig capacitance.

D3005, DECEMBER 1986—REVISED JULY 1989

- Each Device Drives 32 Lines
- 180-V Open-Drain Parallel Outputs
- 220-mA Parallel Output Sink Current Capability
- CMOS-Compatible Inputs
- Strobe Input Provided
- Serial Data Output for Cascade Operation
- Inputs Have Built-in Electrostatic Discharge Protection

description

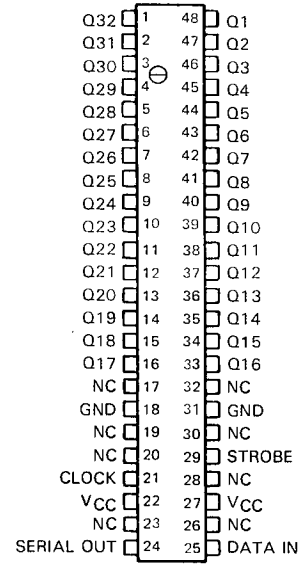
The SN751506 and the SN751516 are monolithic integrated circuits designed to drive the scan lines of a dc plasma panel display. The SN751516 pin sequence is reversed from the SN751506 for ease in printed circuit board layout.

Each device consists of a 32-bit shift register and 32 OR gates. Serial data is entered into the shift register on the high-to-low transition of the clock input. When STROBE is low, all Q outputs are in the off-state. Outputs are open-drain JFET transistors with a breakdown voltage in excess of 180 V. The outputs have a 220-mA sink current capability in the on state. Only one Q output should be allowed to be in the on state at a time.

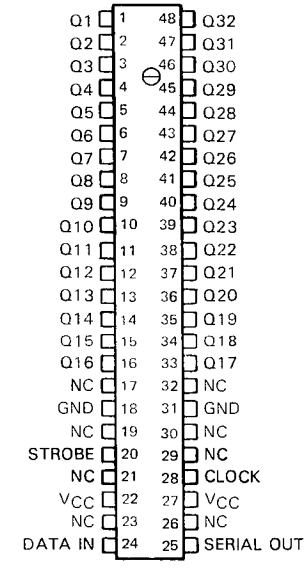
Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the strobe input. All inputs are CMOS compatible with ESD protection built in.

The SN751506 and SN751516 are characterized for operation from 0°C to 70°C.

SN751506 . . . FT PACKAGE
(TOP VIEW)

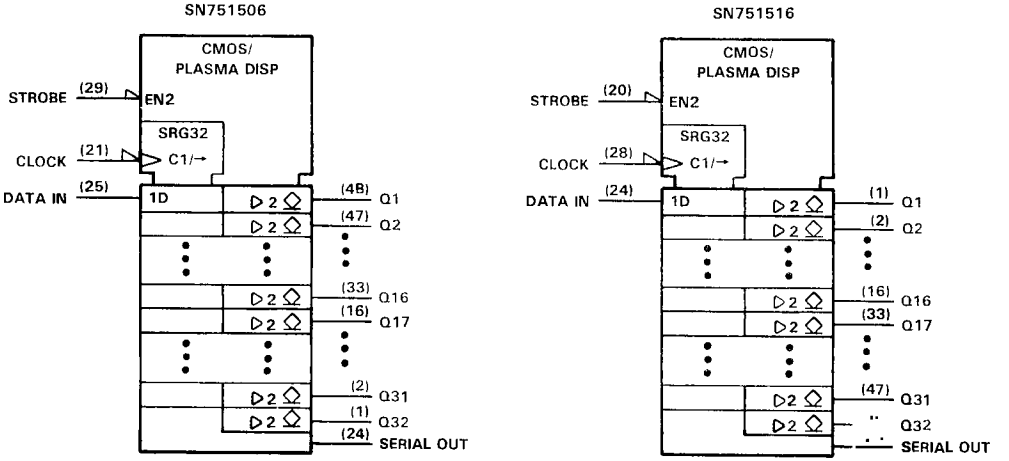


SN751516 . . . FT PACKAGE
(TOP VIEW)



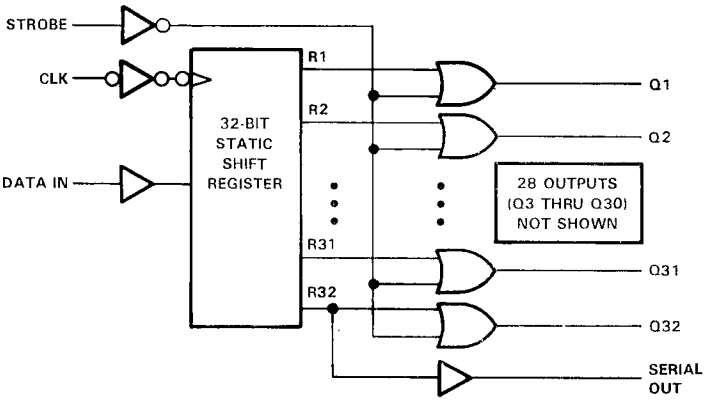
NC—No internal connection

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

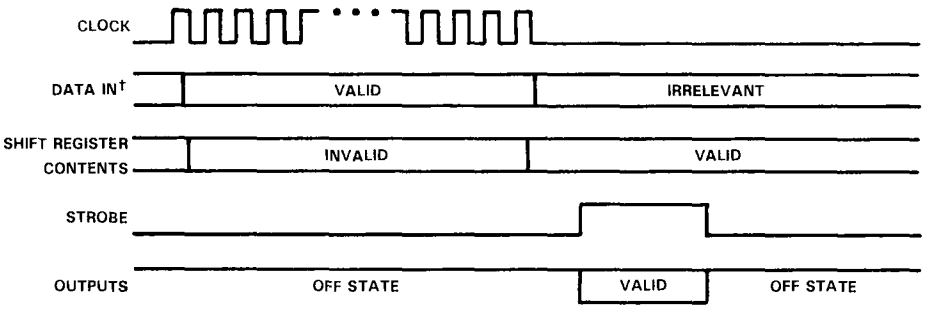


FUNCTION TABLE

FUNCTION	CONTROL INPUTS		SHIFT REGISTERS	OUTPUTS	
	CLOCK	STROBE	R1 THRU R32	SERIAL	Q1 THRU Q32
LOAD	↓	X	Load and shift‡	R32	Determined by STROBE
	No↓	X	No change	R32	
STROBE	X	L	As determined above	R32	All high impedance
	X	H		R32	R1 thru R32

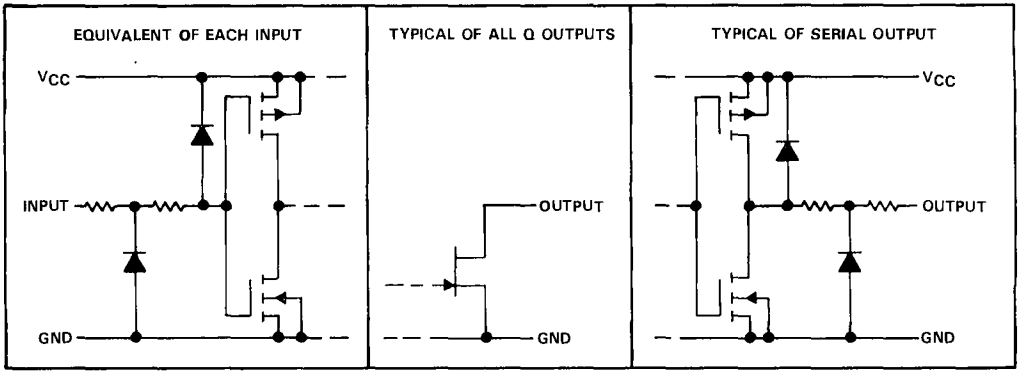
H = high level, L = low level, X = irrelevant, ↓ = high to low transition.
‡ R32 takes on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



†Only 1 bit in 32 should be low in the input data.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.4 V to 7 V
On-state Q output voltage, V_O . . . . . −0.4 V to 125 V
Off-state Q output voltage, V_O . . . . . −0.4 V to 180 V
Input voltage . . . . . −0.4 V to V_{CC} +0.4 V
Serial output voltage . . . . . −0.4 V to V_{CC} +0.4 V
Q output on-state time duration (see Note 2) . . . . . 100 μs
Q output duty cycle (see Note 2) 1/200
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 1025 mW
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to GND.
2. Only one Q output should be on at a time.
3. For operation above 25°C free-air temperature, derate linearly to 656 mW at 70°C at the rate of 8.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4	5	6	V
Peak on-state Q output voltage, $V_{O(on)}$				110	V
High-level input voltage, V_{IH}	V_{CC} = 4 V	3.2			V
	V_{CC} = 6 V	4.8			
Low-level input voltage, V_{IL}	V_{CC} = 4 V			0.8	V
	V_{CC} = 6 V			1.2	
Output current, I_O (T_A = 25°C)					mA
Clock frequency, f_{clock}					kHz
Pulse duration, CLOCK high or low, t_{wCLK}		1.5†			μs
Pulse duration, DATA, t_{wD}		5			μs
Pulse duration, STROBE, t_{wSTRB}		2			μs
Setup time, DATA IN before ↓, t_{su}		1			μs
Hold time, DATA IN after CL		1.2			μs
Operating free-air temperature, T_A		0		70	°C

† The minimum clock period is 5 μs.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	SERIAL OUT	I_{OH} = −0.1 mA	4.5			V
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 180 mA		6	10	V
		SERIAL OUT	I_{OL} = 0.1 mA			0.5	
$I_{O(off)}$	Off-state output current	Q outputs	V_{OH} = 110 V			1	μA
I_{OL}	Low-level output current	Q outputs	V_{OL} = 16 V	220			mA
I_{IH}	High-level input current		$V_I = V_{CC}$			1	μA
I_{IL}	Low-level input current		V_I = 0			−1	μA
C_i	Input capacitance					15	pF
I_{CC}	Supply current		All Q outputs off			1	mA
			One Q output on		20	40	

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, CLOCK to SERIAL OUT	C_L = 15 pF		0.2	0.5	μs
t_{PHL}	Delay time, high-to-low-level Q output from STROBE or CLOCK inputs	C_L = 150 pF, R_L = 470 Ω, See Figures 2 and 3		0.2‡	0.6	μs
t_{PLH}	Delay time, low-to-high-level Q output from STROBE or CLOCK inputs			0.35‡	1	μs
t_{THL}	Transition time, high-to-low-level Q output			0.1	0.3	μs
t_{TLH}	Transition time, low-to-high-level Q output			0.35	1	μs

‡ Typical values are for clock inputs. Typical from strobe inputs will be less.

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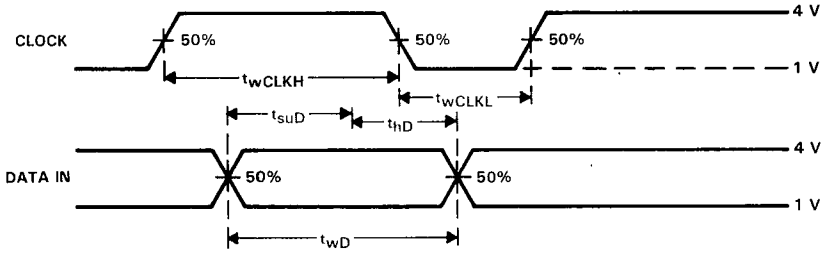


FIGURE 1. INPUT TIMING VOLTAGE WAVEFORMS

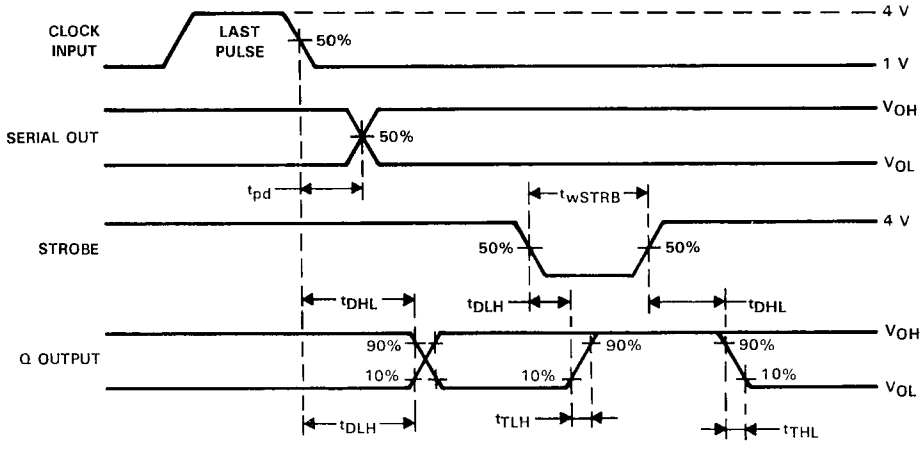
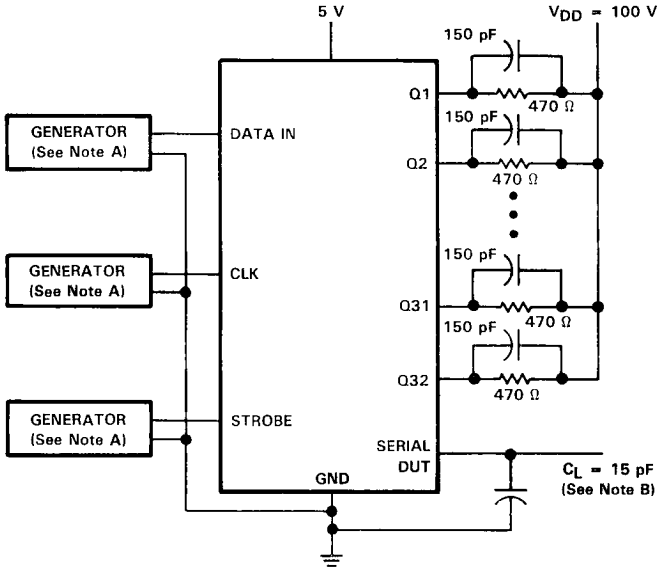


FIGURE 2. SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by generators having the following characteristics: t_w = 1.25 μs, PRR ≤ 200 kHz, t_r ≤ 30 ns, t_f ≤ 30 ns, Z_o = 50 Ω.

B. C_L includes probe and jig capacitance.

FIGURE 3. TEST CIRCUIT

TYPICAL CHARACTERISTICS

LOW-LEVEL Q OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

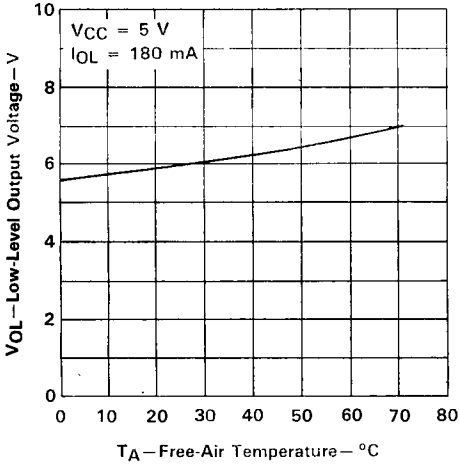


FIGURE 4

LOW-LEVEL Q OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

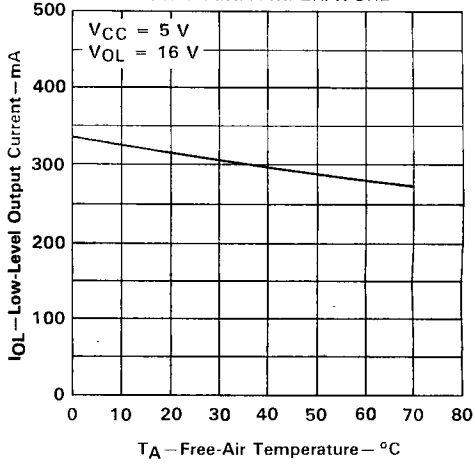


FIGURE 5

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

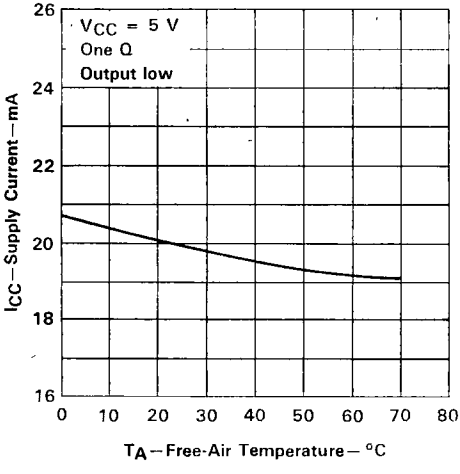


FIGURE 6

PROPAGATION DELAY TIME,
CLOCK TO SERIAL OUTPUT
vs
FREE-AIR TEMPERATURE

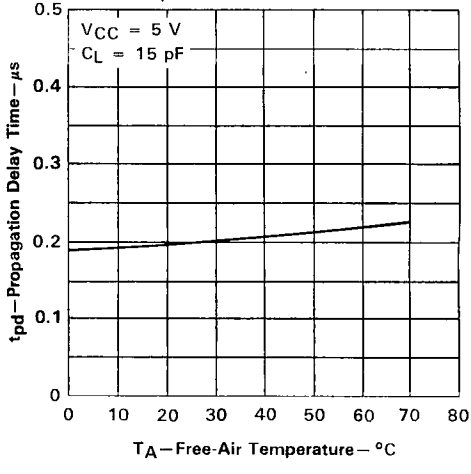


FIGURE 7

TYPICAL CHARACTERISTICS

DELAY TIME,
HIGH-TO-LOW-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

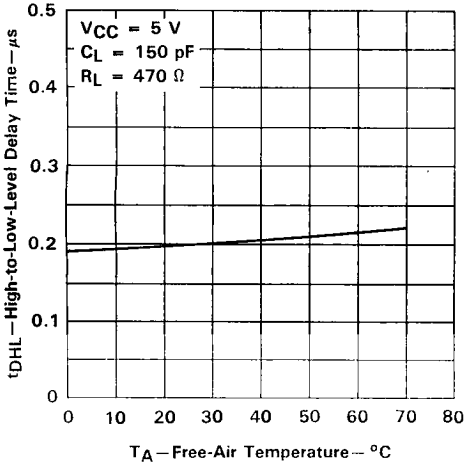


FIGURE 8

DELAY TIME,
LOW-TO-HIGH-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

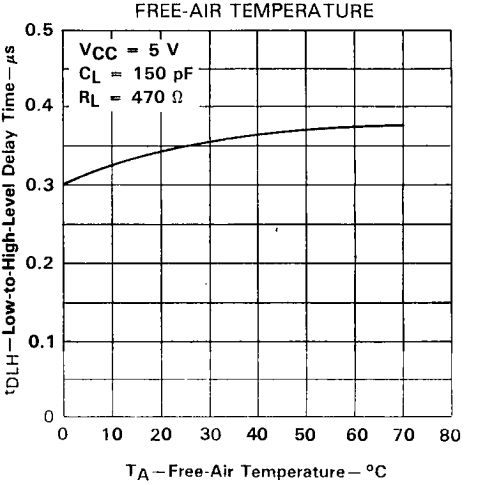


FIGURE 9

TRANSITION TIME,
HIGH-TO-LOW-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

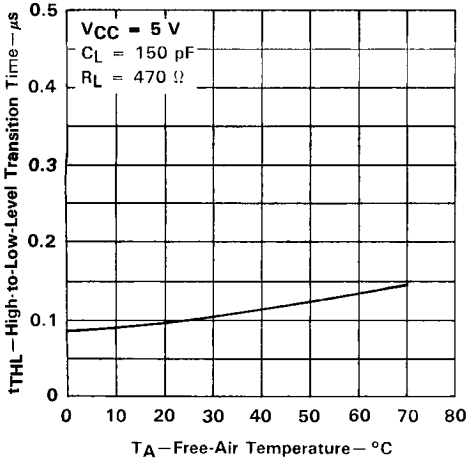


FIGURE 10

TRANSITION TIME,
LOW-TO-HIGH-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

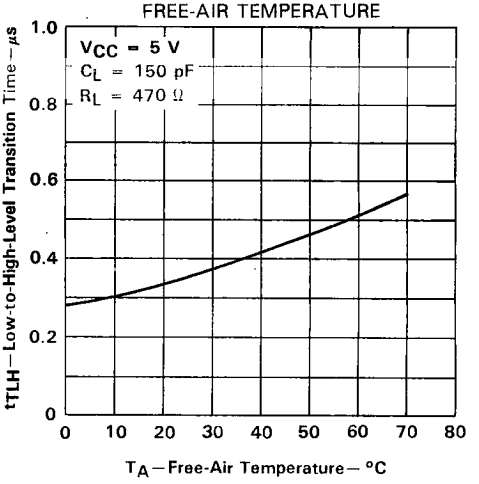
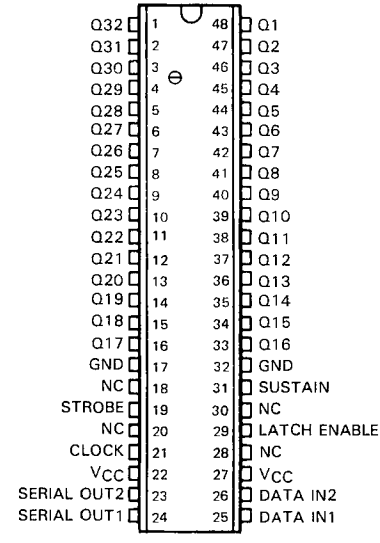


FIGURE 11

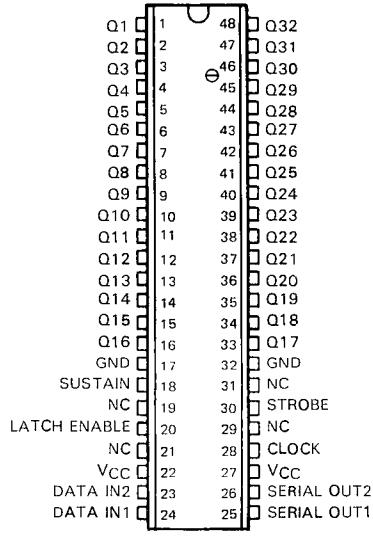
D2984, JANUARY 1987—REVISED NOV **

- Each Device Drives 32 Lines
- −120-V P-N-P Open-Collector Parallel Outputs
- High-Speed Serially Shifted Data Inputs
- CMOS-Compatible Inputs
- Strobe and Sustain Inputs Provided
- Serial Data Output for Cascade Operation

SN751508 . . . FT PACKAGE
(TOP VIEW)



SN751518 . . . FT PACKAGE
(TOP VIEW)



NC—No internal connection

description

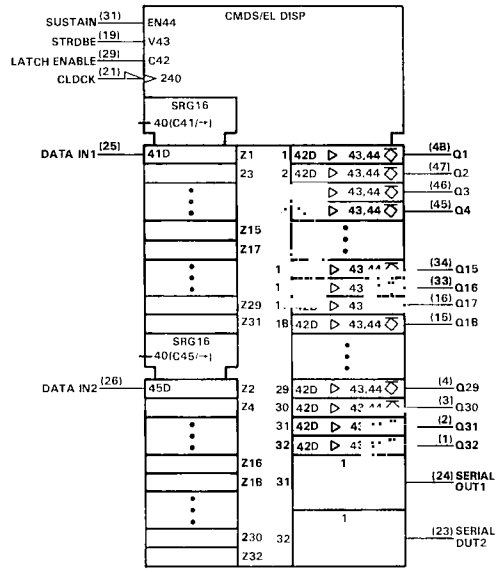
The SN751508 and SN751518 are monolithic integrated circuits designed to drive the data lines of a dc plasma panel display. The SN751518 pin sequence is reversed from the SN751508 for ease in printed circuit board layout.

Each device consists of two 16-bit shift registers, 32 latches, 32 OR gates, and 32 P-N-P open-collector output AND gates. Typically, a 32-bit data string is split into two 16-bit data strings externally and then entered in parallel into the shift registers on the high-to-low transition of the clock signal. A high LATCH ENABLE transfers the data from the shift registers to the inputs of 32 OR gates through the latches. Data present in the latch during the high-to-low transition of LATCH ENABLE is stored. When STROBE is high, the latch is masked and a high will be placed on the data input of the output AND gates. When STROBE is low, and SUSTAIN is high, data from the latches is reflected at the outputs. When low, SUSTAIN will force all outputs to their off state. Drivers may be cascaded via the serial data outputs of the static shift registers. These outputs are not affected by LATCH ENABLE, STROBE, or SUSTAIN.

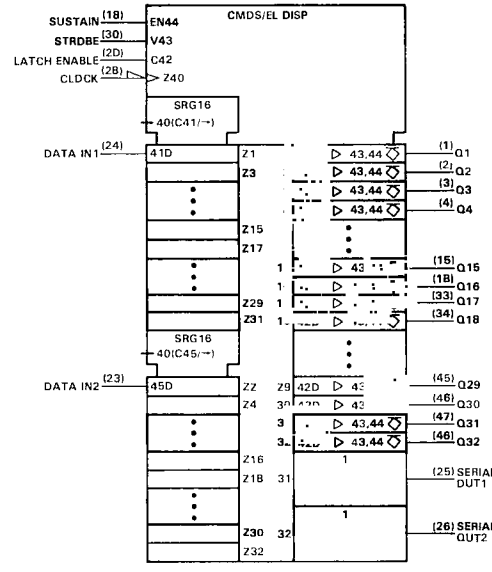
The SN751508 and the SN751518 are characterized from 0°C to 70°C.

logic symbols†

SN751508

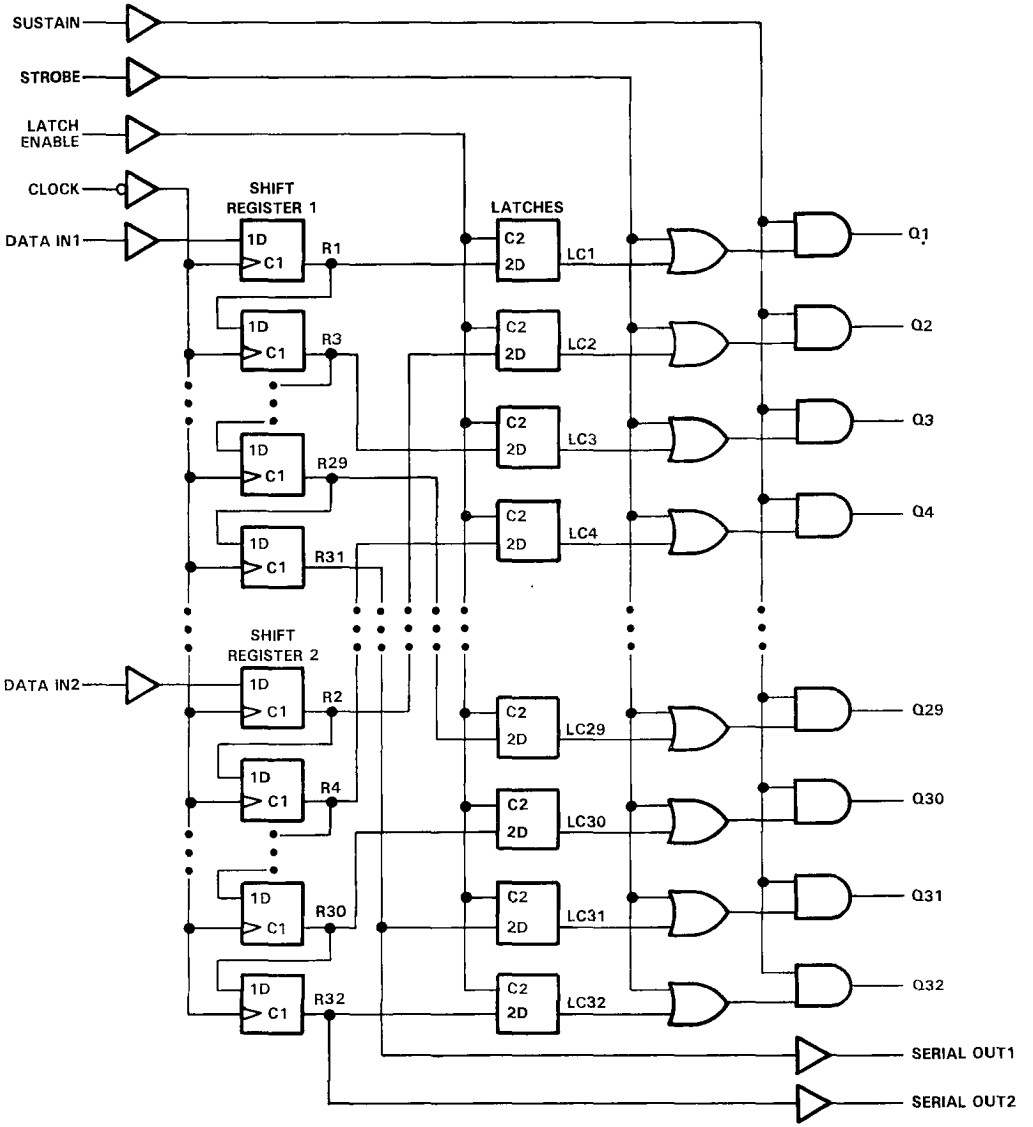


SN751518



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



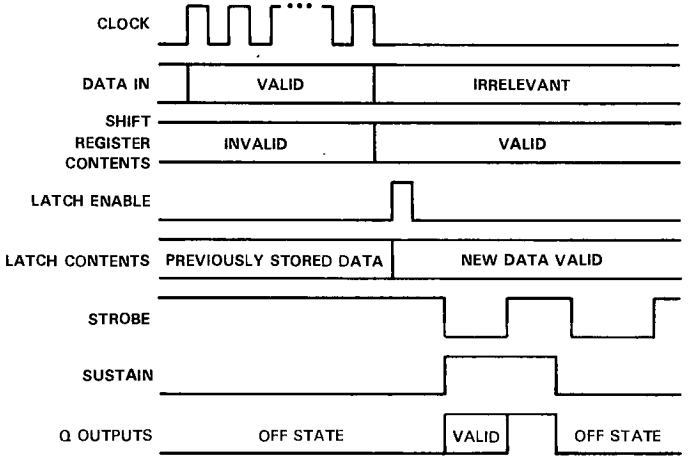
FUNCTION	CONTROL INPUTS				SHIFT REGISTERS R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS		
	CLOCK	LATCH ENABLE	STROBE	SUSTAIN			SERIAL SO1	SERIAL SO2	Q1 THRU Q32
LOAD	↓	X	X	X	Load and shift†	Determined by	R31	R32	Determined by
	No ↓	X	X	X	No change	LATCH ENABLE‡			SUSTAIN and STROBE
LATCH ENABLE	X	L	X	X	As determined	Stored data	R31	R32	Determined by
	X	H	X	X	above	New data			SUSTAIN and STROBE
STROBE	X	X	L	H	As determined	Determined by	R31	R32	LC1 thru LC32
	X	X	H	H	above	LATCH ENABLE‡			All on (high)
SUSTAIN	X	X	X	L	As determined above	Determined by LATCH ENABLE‡	R31	R32	All off

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition

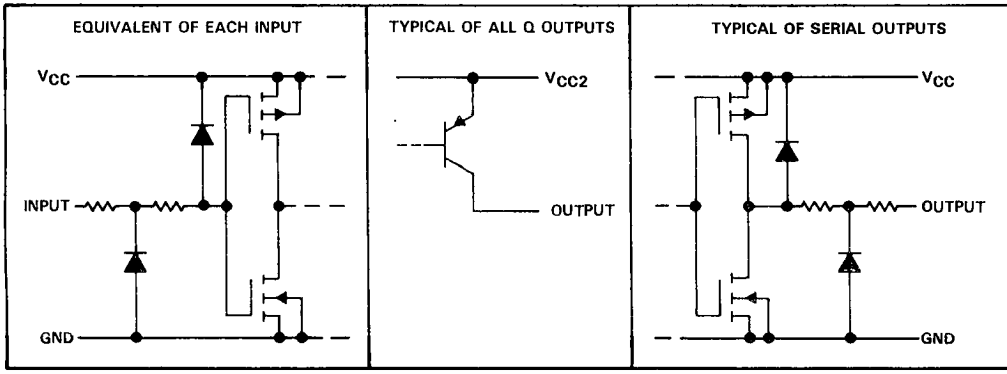
†Each even-numbered shift register stage takes on the state of the next-lower even-numbered stage, and likewise each odd-numbered shift register stage takes on the state of the next-lower odd-numbered stage; i.e., R32 takes on the state of R30, R30 takes on the state of R28, . . . R4 takes on the state of R2, R2 takes on the state of Data In2, R31 takes on the state of R29, R29 takes on the state of R27, . . . R3 takes on the state of R1, and R1 takes on the state on Data In1.

‡New data enters the latches while LATCH ENABLE is high. This data is stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.4 to 7 V
On-state Q output voltage, V_O . . . . . −120 V to V_{CC}+0.4 V
Input voltage . . . . . −0.4 V to V_{CC}+0.4 V
Serial output voltage . . . . . −0.4 V to V_{CC}+0.4 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1025 mW
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltages values are with respect to GND.
2. For operation above 25°C free-air temperature, derate linearly to 656 mW at 70°C at the rate of 8.2 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.5	5	5.5	V
Output voltage, V_O					−75	V
High-level input voltage, V_{IH}		V_{CC} = 4.5 V	3.6			V
		V_{CC} = 5.5 V	4.4			
Low-level input voltage, V_{IL}		V_{CC} = 4.5 V			0.9	V
		V_{CC} = 5.5 V			1	
Output current, I_O (T_A = 25°C)					−1.2	mA
Clock frequency, f_{clock}					5	MHz
Pulse duration, t_w (see Figure 1)	CLOCK		75			ns
	DATA IN		160			
	LATCH ENABLE		90			
	[illegible]		2			μs
	[illegible]		2			
Setup time, t_{su} (see Figure 1)	DATA IN before CL[illegible]		20			ns
	CLOCK low before L[illegible] ENABLE↑		50			
	LATCH ENABLE low before CLOCK↓		0			
	L[illegible] ENABLE high before STROBE↓		0			
	L[illegible] ENABLE high before SUSTAIN↑		0			
Hold time, DATA IN after CLOCK↓, t_h (see Figure 1)			50			μs
Operating free-air temperature, T_A			0		70	°C

electrical characteristics, V_{CC} = 5 V, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH} High-level output voltage	Q outputs		I_{OH} = −0.5 mA		4	4.5		V
	Serial Outputs	V_{CC} = 5.5 V	I_{OH} = −100 μA		4.3	4.6		
			I_{OH} = −20 μA		4.4			
		V_{CC} = 4.5 V	I_{OH} = −100 μA		3.4	3.6		
			I_{OH} = −20 μA		3.6			
V_{OL} Low-level output voltage	Serial Outputs	V_{CC} = 5.5 V	I_{OL} = 100 μA			0.9	1.2	V
			I_{OL} = 20 μA				1.1	
		V_{CC} = 4.5 V	I_{OL} = [illegible] μA			0.9	1.1	
			I_{OL} = 20 μA				0.9	
I_{OH} High-level Q output current			T_A = 25°C,	V_O = 3 V	−1.2			mA
I_{OL} Low-level Q output current			T_A = 25°C,	V_O = −75 V			−500	μA
I_{IH} High-level input current			T_A = 25°C,	V_I = V_{CC}			1	μA
I_{IL} Low-level input current			T_A = 25°C,	V_I = 0			−1	μA
I_{CC} Supply current			All Q outputs high,	V_{CC} = 5.5 V		17	25	mA
			All Q outputs low				3	
C_i Input capacitance							15	pF

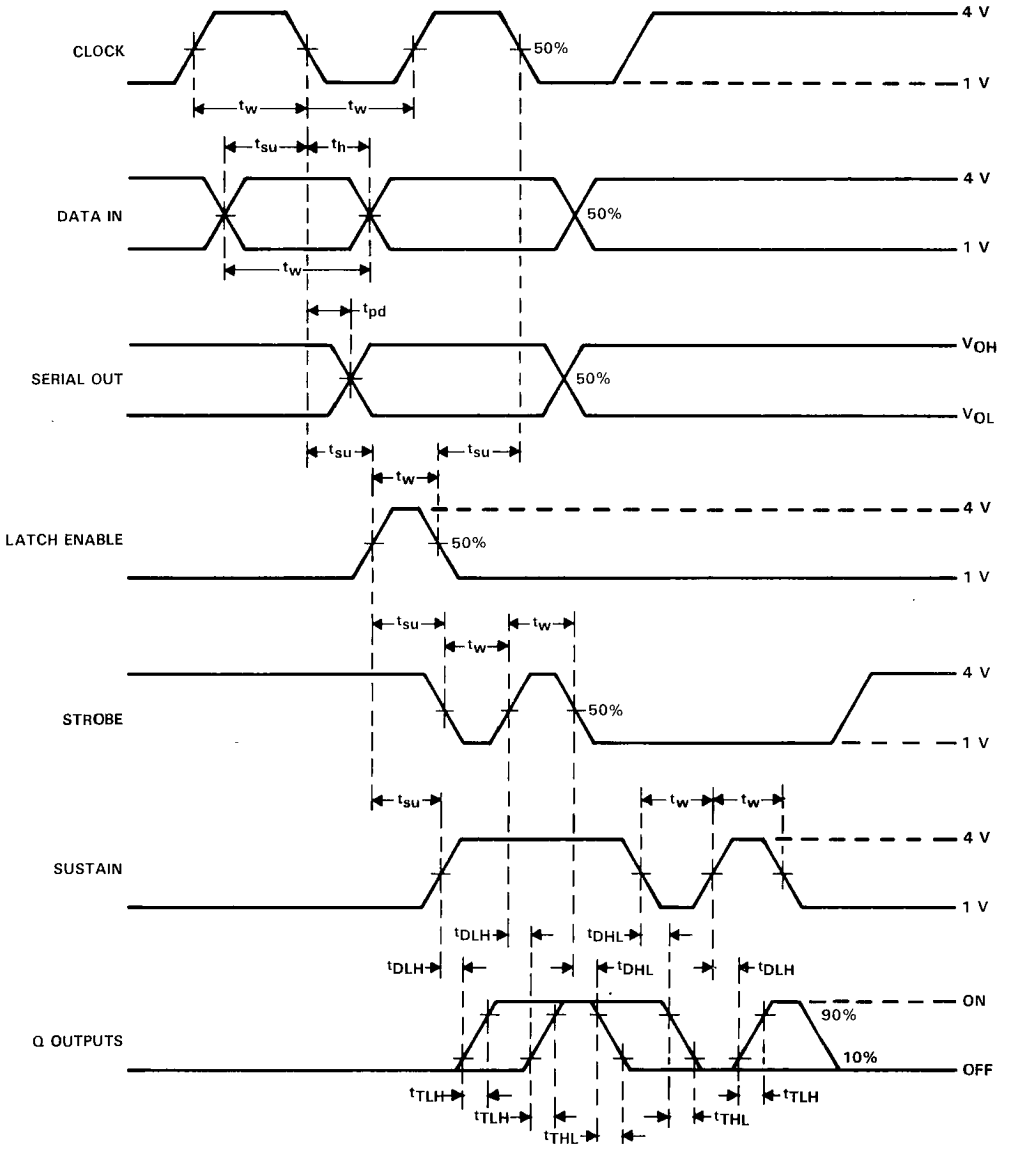
†All typical values are at T_A = 25°C.

switching characteristics V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, CLOCK to Serial Outputs		C_L = 15 pF		100	150	ns
t_{DLH}	Delay time, low-to-high-level Q output from	↑AIN or S̄	C_L = 15 pF, R_L = 91 kΩ, See Figures 1 and 2		0.3‡	1	μs
t_{DHL}	Delay time, high-to-low-level Q output from	AIN or S̄			1‡	2.5	μs
t_{TLH}	Transition time, low-to-high-level Q output				2	5	μs
t_{THL}	Transition time, high-to-low-level Q output				11	18	μs

‡Typical values for delay times are measured from the SUSTAIN input.

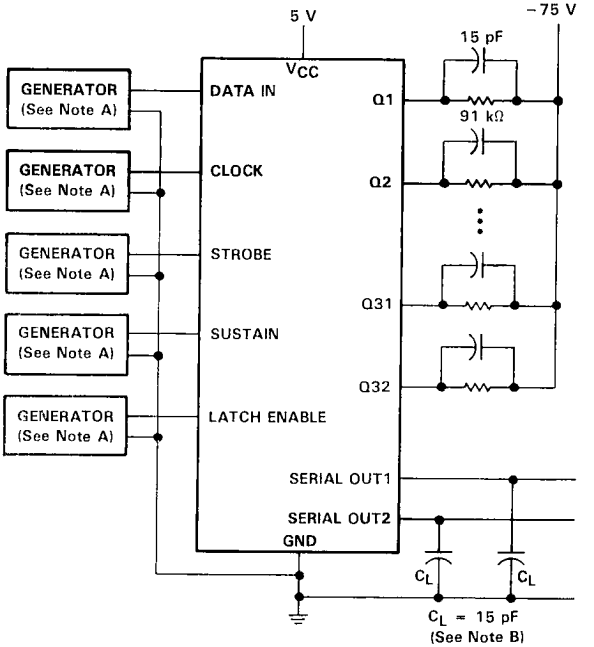
PARAMETER MEASUREMENT INFORMATION



NOTE: Input t_r and t_f are less than or equal to 10 ns.

FIGURE 1. INPUT TIMING AND SWITCHING TIME VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

NOTES: A. Input pulses are supplied by generators having the following characteristics: t_W = 100 ns, PRR ≤ 5 MHz, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_o = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

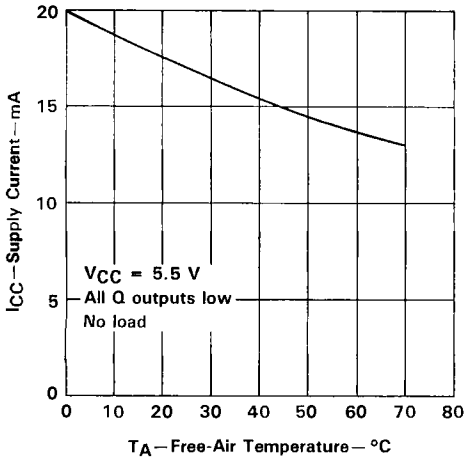


FIGURE 3

DELAY TIME, CLOCK TO SERIAL OUTPUT
vs
FREE-AIR TEMPERATURE

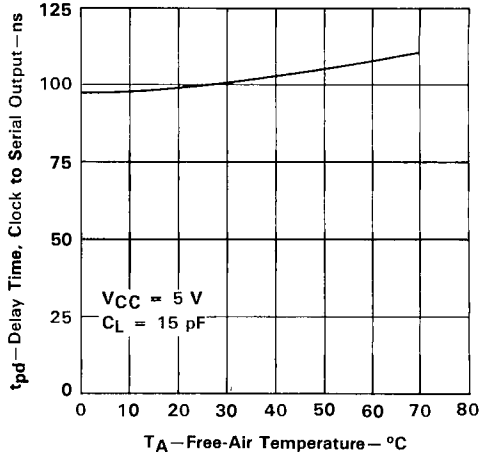


FIGURE 4

DELAY TIME, SUSTAIN INPUT TO Q OUTPUT,
LOW TO HIGH
vs
FREE-AIR TEMPERATURE

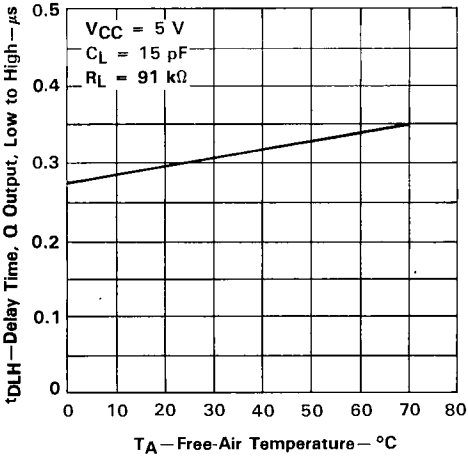


FIGURE 5

DELAY TIME, SUSTAIN INPUT TO Q OUTPUT,
HIGH TO LOW
vs
FREE-AIR TEMPERATURE

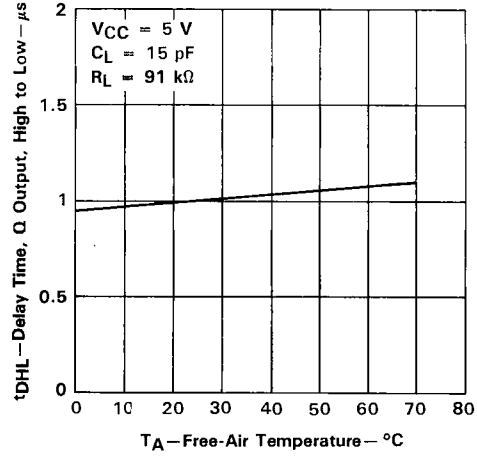


FIGURE 6

TYPICAL CHARACTERISTICS

TRANSITION TIME, Q OUTPUT, LOW TO HIGH vs FREE-AIR TEMPERATURE

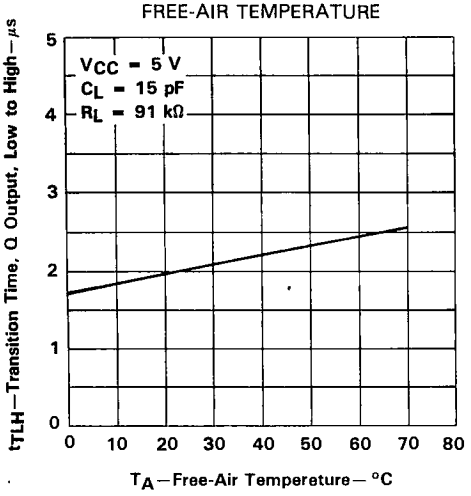


FIGURE 7

TRANSITION TIME, Q OUTPUT, HIGH TO LOW vs FREE-AIR TEMPERATURE

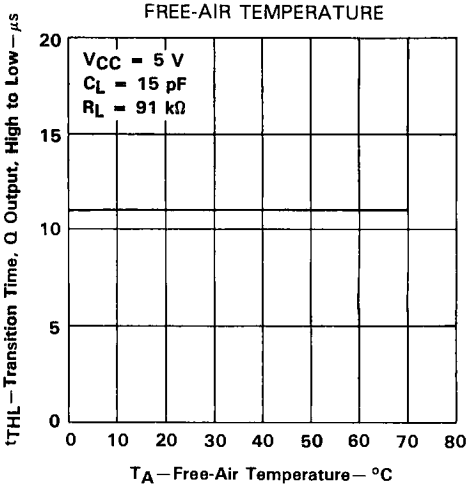
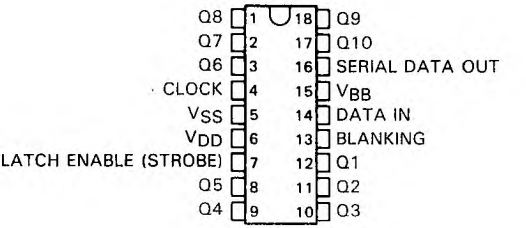


FIGURE 8

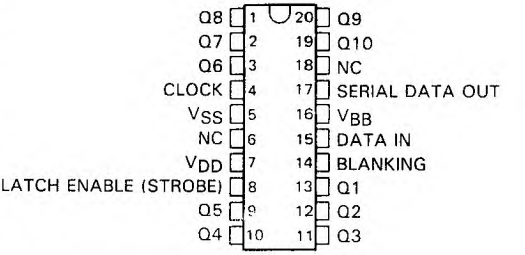
D2715, DECEMBER 1984—REVISED OCTOBER 1989

- **Each Device Drives 10 Lines**
- **60-V Output Voltage Rating**
- **40-mA Output Source Current**
- **High-Speed Serially-Shifted Data Input**
- **CMOS-Compatible Inputs**
- **Latches on All Driver Outputs**
- **Improved Direct Replacement for UCN4810A and TL4810A**

N PACKAGE
(TOP VIEW)



DW
SMALL OUTLINE PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TL4810BI and TL4810B are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). These devices feature a serial data output to cascade additional devices for large display arrays.

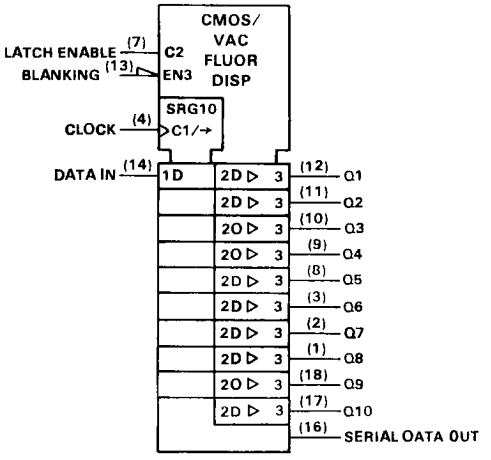
A 10-bit data word is serially loaded into the shift register on the positive-going transitions of the clock. Parallel data is transferred to the output buffers through a 10-bit D-type latch while LATCH ENABLE is high and is latched when LATCH ENABLE is low. When BLANKING is high, all outputs are low.

Outputs are totem-pole structures formed by n-p-n emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 70 V and 40 mA source-current capability. All inputs are compatible with CMOS and TTL levels, but each requires the addition of a pull-up resistor to V_{DD} when driven by TTL logic.

The TL4810BI is characterized for operation from −40°C to 85°C. The TL4810B is characterized for operation from 0°C to 70°C.

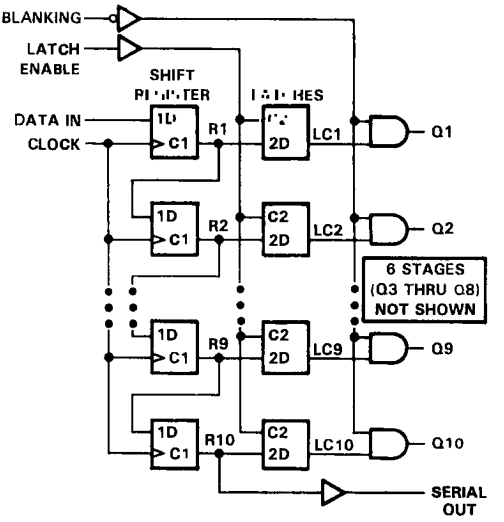
† BIDFET—Bipolar, Double-Diffused, N-Channel and P-Channel MOS transistors on same chip—patented process.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)

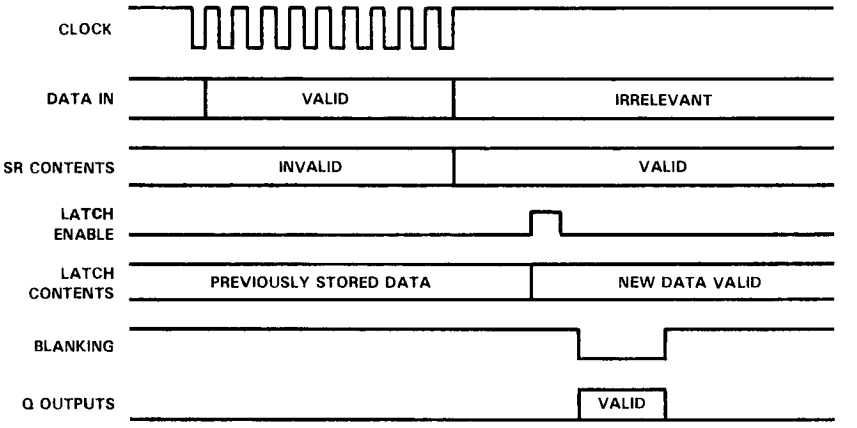


FUNCTION TABLE

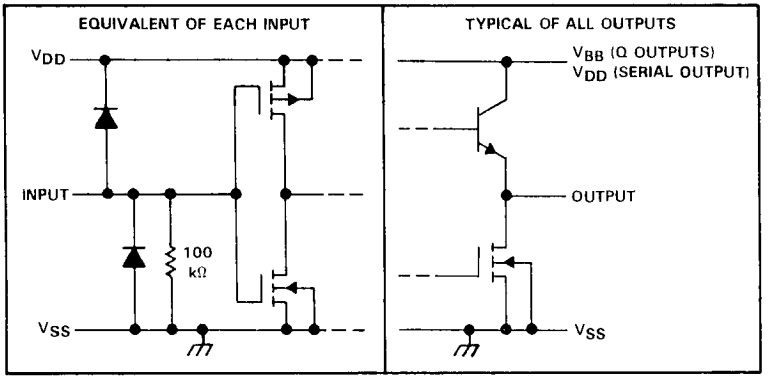
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS	LATCHES	OUTPUTS	
	CLOCK	LATCH ENABLE	BLANKING	R1 THRU R10‡	LC1 THRU LC10	SERIAL	Q1 THRU Q10
LOAD	↑	X	X	Load and shift‡	Determined by LATCH ENABLE§	R10	Determined by BLANKING
	Not↑	X	X	No change			
LATCH	X	L	X	As determined above	Stored data	R10	Determined by BLANKING
	X	H	X		New data		
BLANK	X	X	H	As determined above	Determined by LATCH ENABLE§	R10	All L
	X	X	L				LC1 thru LC10 respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
‡ Register R10 takes on the state of R9, R9 takes on the state of R8 . . . R2 takes on the state of R1, and R1 takes on the state of the data input.
§ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Driver supply voltage, V_{BB} . . . . . 70 V
Output voltage . . . . . 70 V
Input voltage . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TL4810BI . . . . . −40°C to 85°C
TL4810B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to V_{SS}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

PARAMETER		TL4810BI			TL4810B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4.75		15.75	4.75		15.75	V
Supply voltage, V_{BB}		5		60	5		60	V
Supply voltage, V_{SS}			0			0		V
High-level input voltage, V_{IH}	for V_{DD} = 5 V	3.5		5.3	3.5		5.3	V
	for V_{DD} = 15 V	13.5		15.3	13.5		15.3	
Low-level input voltage, V_{IL}		−0.3†		0.8	−0.3†		0.8	V
Continuous high-level output current, I_{OH}				−25			−25	mA
Operating free-air temperature, T_A		−40		85	0		70	°C

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltages only.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V to 15 V, V_{BB} = 60 V, V_{SS} = 0 (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TL4810BI			TL4810B			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	Q outputs	I_{OH} = −25 mA		57.6	58		57.6	58		V
		Serial output	V_{DD} = 5 V,	I_{OH} = −100 μA	4	4.5		4	4.5		
			V_{DD} = 15 V,	I_{OH} = −100 μA	14	14.7		14	14.7		
V_{OL}	Low-level output voltage	Q outputs	I_{OH} = 1 μA,	BLANKING at V_{DD}		0.5	1		0.5	1	V
		Serial output	V_{DD} = 5 V,	I_{OL} = 100 μA		0.05	0.1		0.05	0.1	
			V_{DD} = 15 V,	I_{OL} = 100 μA		0.02	0.1		0.02	0.1	
I_{OL}	Low-level Q output current (pull-down current)		V_O = 60 V, T_A = MIN to 70°C	BLANKING at V_{OO},	2.5	3.7		2.5	3.7		mA
			V_O = 60 V, T_A = 85°C	BLANKING at V_{OO},	2						
$I_{O(off)}$	Off-state output current		V_O = 0, T_A = MAX	BLANKING at V_{DD},		−1	−15		−1	−15	μA
I_H	High-level input current		V_I = V_{DD}			30	50		30	50	μA
I_{BB}	Supply current from V_{BB}		All outputs low			0.5	1		0.5	1	mA
			All outputs high, T_A = 0°C to MAX			2.7	4		2.7	4	
			All outputs high, T_A = −40°C				5				
I_{DD}	Supply current from V_{DD}		All inputs at 0 V, One Q output high	V_{DD} = 5 V		10	50		10	50	μA
				V_{DD} = 15 V		10	100		10	100	
			All inputs at 0 V, All outputs low	V_{DD} = 5 V		10	50		10	50	
				V_{DD} = 15 V		10	100		10	100	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C, except for I_O.

timing requirements over recommended operating free-air temperature range

PARAMETER		V_{DD} = 5 V		V_{DD} = 15 V		UNIT
		MIN	MAX	MIN	MAX	
$t_{w(CKH)}$	Pulse duration, CLOCK high	[illegible]		50		ns
$t_{w(LEH)}$	Pulse duration, LATCH ENABLE high	[illegible]		50		ns
$t_{su(O)}$	Setup time, DATA IN before CLOCK↑	125		25		ns
$t_{h(O)}$	Hold time, DATA IN after CLOCK↑	125		25		ns
$t_{CKH-LEH}$	Delay time, CLOCK↑ to LATCH ENABLE high	125		25		ns

switching characteristics, V_{BB} = 60 V, T_A = 25°C

PARAMETER			MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, LATCH ENABLE to output	V_{DD} = 5 V		1		μs
		V_{DD} = 15 V		0.5		

PARAMETER MEASUREMENT INFORMATION

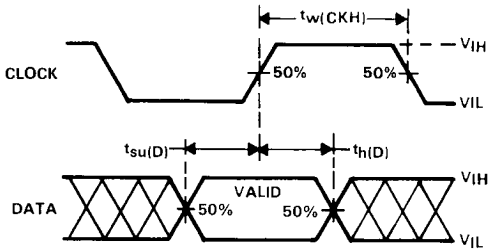


FIGURE 1. INPUT TIMING

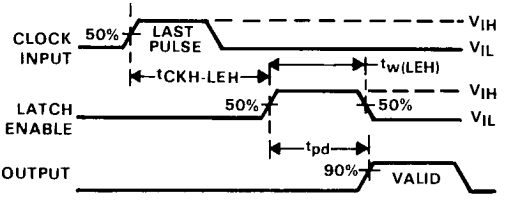


FIGURE 2. OUTPUT SWITCHING TIMES

THERMAL INFORMATION

DW PACKAGE DUTY CYCLE
vs
FREE-AIR TEMPERATURE

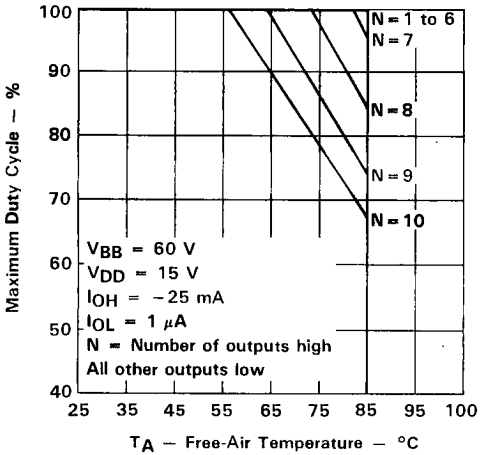


FIGURE 3

N PACKAGE DUTY CYCLE
vs
FREE-AIR TEMPERATURE

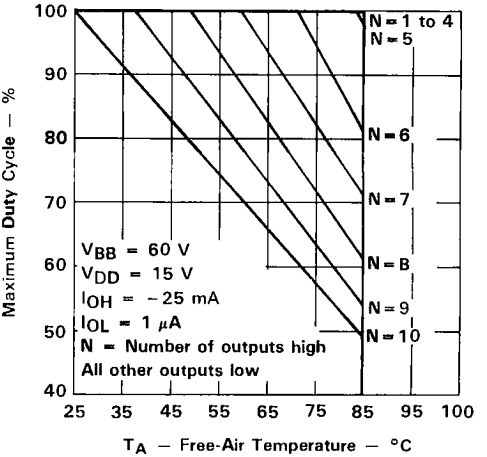
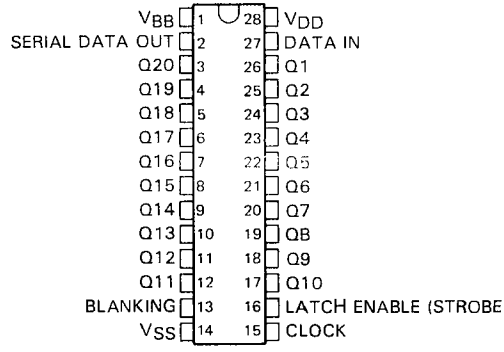


FIGURE 4

D2914, OCTOBER 1985—REVISED OCTOBER 1989

- Drives Up to 20 Lines
- 70-V Output Voltage Swing Capability
- 40-mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- CMOS-Compatible Inputs
- Direct Replacement for Sprague UCN5812A

N PACKAGE
(TOP VIEW)



description

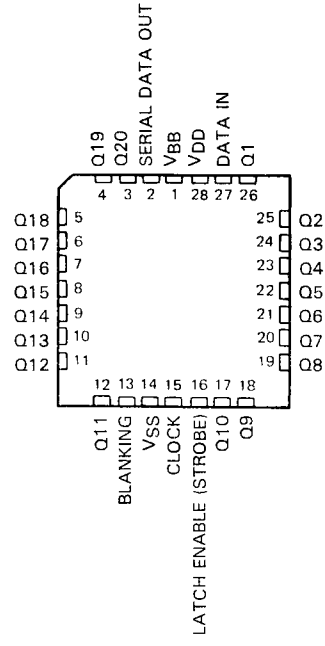
The TLC5812I and TLC5812 are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). Each device features a serial data output to cascade additional devices for large display arrays.

A 20-bit data word is serially loaded into the shift register on the low-to-high transition of CLOCK. Parallel data is transferred to the output buffers through a 20-bit D-type latch while LATCH ENABLE is high and is latched when LATCH ENABLE is low. When BLANKING is high, all outputs are low.

The outputs are totem-pole structures formed by n-p-n emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 70 V and a source-current capability of 40 mA. All inputs are CMOS compatible.

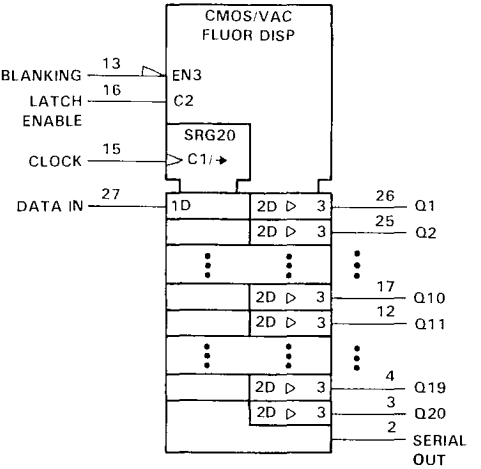
The TLC5812I is characterized for operation from −40°C to 85°C. The TLC5812 is characterized for operation from 0°C to 70°C.

FN PACKAGE
(TOP VIEW)



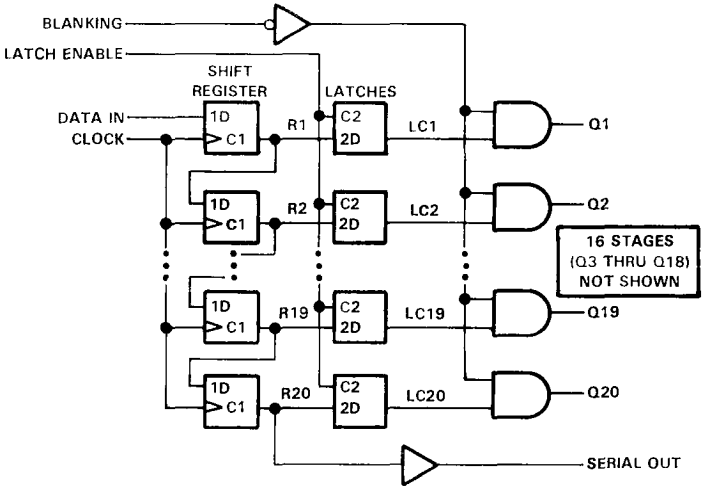
† BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip — patented process.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

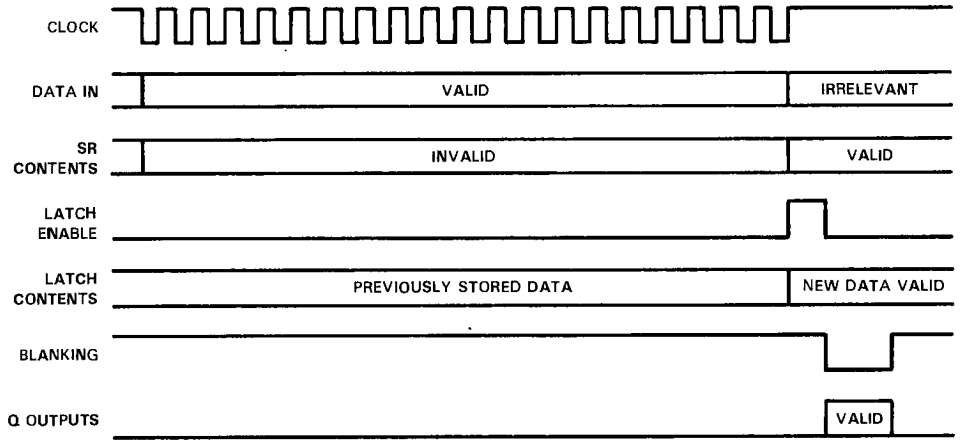


FUNCTION TABLE

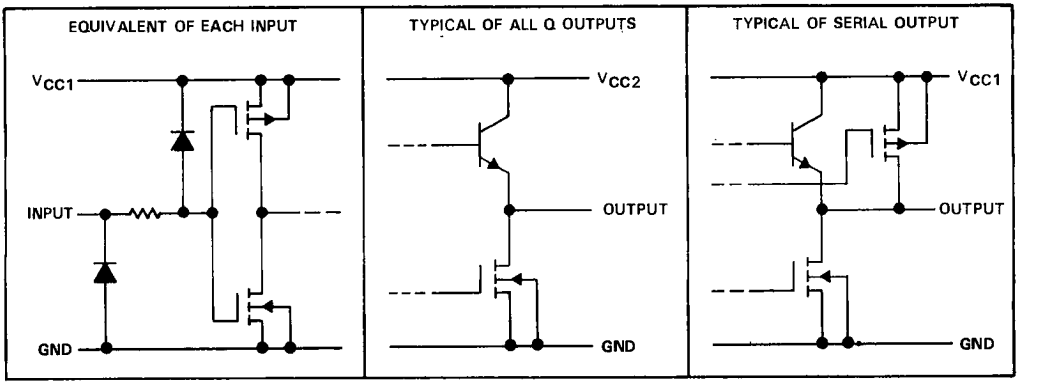
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R20	LATCHES LC1 THRU LC20	OUTPUTS	
	CLOCK	LATCH ENABLE	BLANKING			SERIAL	Q1 THRU Q20
LOAD	↑	X	X	Load and shift†	Determined by	R20	Determined by BLANKING
	Not↑	X	X	No change	LATCH ENABLE‡	R20	
LATCH	X	L	X	As determined above	Stored data	R20	Determined by BLANKING
	X	H	X		New data	R20	
BLANK	X	X	H	As determined above	Determined by	R20	All L
	X	X	L		LATCH ENABLE‡	R20	LC1 thru LC20, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
†R20 takes on the state of R19, R19 takes on the state of R18, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.
‡New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 15 V
Supply voltage, V_{BB} . . . . . 70 V
Output voltage, V_O . . . . . 70 V
Input voltage, V_I . . . . . −0.3 V to V_{DD} +0.3 V
Output current, I_O . . . . . −40 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TL5812I . . . . . −40°C to 85°C
TL5812 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1. All voltage values are with respect to V_{SS}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1400 mW	11.2 mW/°C	[illegible] mW	[illegible] mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions.

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5		15	V
Supply voltage, V_{BB}		0		60	V
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH}		$V_{DD}-1.5$		$V_{DD}+0.3$	V
Low-level input voltage, V_{IL}		−0.3†		0.8	V
High-level output current, I_{OH}				−40	mA
Operating free-air temperature, T_A	TL5812I	−40		85	°C
	TL5812	0		70	

†The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over operating free-air temperature range, V_{DD} = 5 V to 15 V, V_{BB} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output	Q outputs	I_{OH} = −25 mA		57.5	58.2		V
		Serial outputs	V_{DD} = 5 V,	I_{OH} = −20 μA	4.5	4.9		
			V_{DD} = 15 V,	I_{OH} = −20 μA	14.5	14.9		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 mA,	BLANKING at V_{DD}		0.7	1.5	V
		Serial outputs	V_{DD} = 5 V,	I_{OL} = 20 μA		0.06	0.3	
			V_{DD} = 15 V,	I_{OL} = 20 μA		0.03	0.3	
I_{IH}	High-level input current		$V_I = V_{DD}$			0.3	1	μA
I_{IL}	Low-level input current		V_I = 0			−0.3	−1	μA
I_{OL}	Low-level output current (pull down current)		V_O = 60 V,	BLANKING at V_{DD}	2.5	3.2		μA
$I_{O(off)}$	Off-state output current		V_O = 0,	BLANKING at V_{DD}		<−1	−15	μA
I_{BB}	Supply current from V_{BB}		Outputs high			3.5	8	mA
			Outputs low			0.02	0.5	
I_{DD}	Supply current from V_{DD}		V_{DD} = 5 V			1.5	3	mA
			V_{DD} = 15 V			1.7	4	

‡All typical characteristics are at T_A = 25°C.

timing requirements over operating free-air temperature range

PARAMETER			MIN	MAX	UNIT
t_{wCKH}	Pulse duration, CLOCK high	V_{DD} = 5 V			ns
		V_{DD} = 15 V			
t_{wLEH}	Pulse duration, LATCH ENABLE high	V_{DD} = 5 V			ns
		V_{DD} = 15 V			
t_{suD}	Setup time, data before CLOCK↑	V_{DD} = 5 V	150		ns
		V_{DD} = 15 V	75		
t_{hD}	Hold time, data after CLOCK↑	V_{DD} = 5 V			ns
		V_{DD} = 15 V			
$t_{CKH-LEH}$	Delay time, CLOCK↑ to LATCH ENABLE high	V_{DD} = 5 V	150		ns
		V_{DD} = 15 V	75		

switching characteristics, V_{BB} = 60 V, T_A = 25°C

PARAMETER			MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, LATCH ENABLE to output	V_{DD} = 5 V		2.2		μs
		V_{DD} = 15 V		0.8		

PARAMETER MEASUREMENT INFORMATION

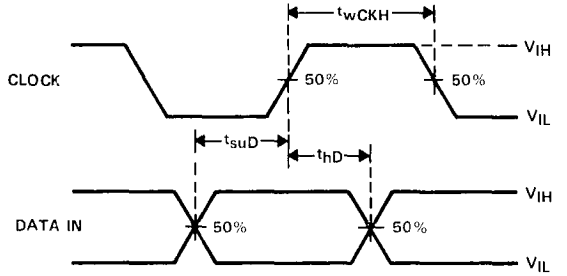


FIGURE 1. INPUT TIMING

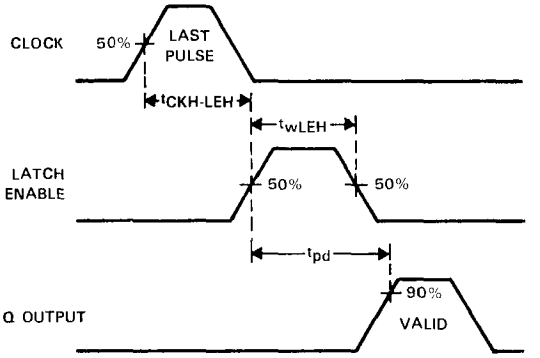


FIGURE 2. OUTPUT SWITCHING TIMES

THERMAL INFORMATION

DUTY CYCLE
vs
FREE-AIR TEMPERATURE

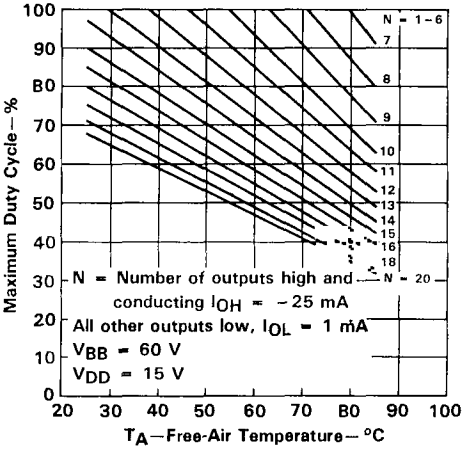


FIGURE 3