ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

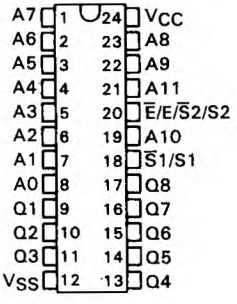
Unused inputs must always be connected to an appropriate logic voltage level, preferably either supply voltage or ground.

Additional information concerning the handling of ESD sensitive devices is provided in Section 12 in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies."*

SEPTEMBER 1984 — REVISED NOVEMBER 1985

- 4096 X 8 Organization
- All Inputs and Outputs TTL Compatible
- Fully Static (No Clocks, No Refresh)
- Single 5-V Power Supply
- Maximum Access Time from Address
  TMS2332-15 150 ns
  TMS2332-20 200 ns
  TMS2332-25 250 ns
- Pin Compatible with 2732A EPROM
- Optional Power Down or Chip Select
- Two Output-Enable Controls for Chip Select Flexibility
- Worst Case Active Power Dissipation . . . 330 mW
- Worst Case Standby Power Dissipation . . . 82.5 mW

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A11	Address Inputs
Ē/E/S̄2/S2	Chip Enable/Power Down or Chip Select
Q1-Q8	Data Out
S̄1/S1	Chip Select
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS2332 is a 32,768-bit read-only memory organized as 4,096 words of 8-bit length. This makes the TMS2332 ideal for microprocessor-based systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS2332 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. Pins 18 and 20 are mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of pins 18 and 20.

This ROM is supplied in a 24-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. The device is designed for operation from 0°C to 70°C.

operation

address (A0-A11)

The address-valid interval determines the device cycle time. The 12-bit positive-logic address is decoded on chip to select one of 4096 words of 8-bit length in the memory array. A0 is the least-significant bit and A11 is the most-significant bit of the word address.

chip selects (S̄1 or S1 and S̄2 or S2)

Each of these pins can be programmed during mask fabrication to be active with either a high- or a low-level input. When both signals are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either signal is not active, all eight outputs are in a high-impedance state.

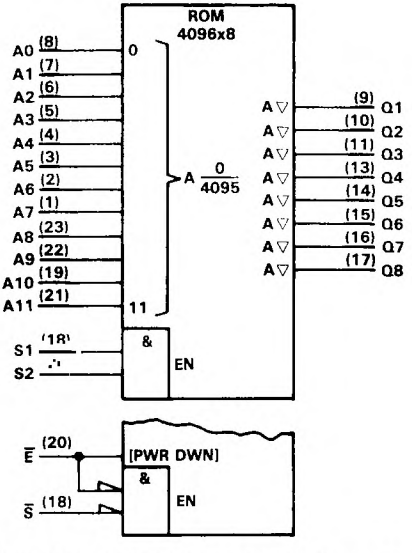
chip enable/power down ($\overline{E}$ or E) or chip select ($\overline{S}2$ or S2)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin ($\overline{E}$ or E) or a secondary chip-select pin ($\overline{S}2$ or S2). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby I_{CC2} of 15 mA. When pin 20 is programmed as a chip-select pin, it is functionally identical to pin 18.

data out (Q1-Q8)

The eight outputs must be enabled by pins 18 and 20 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

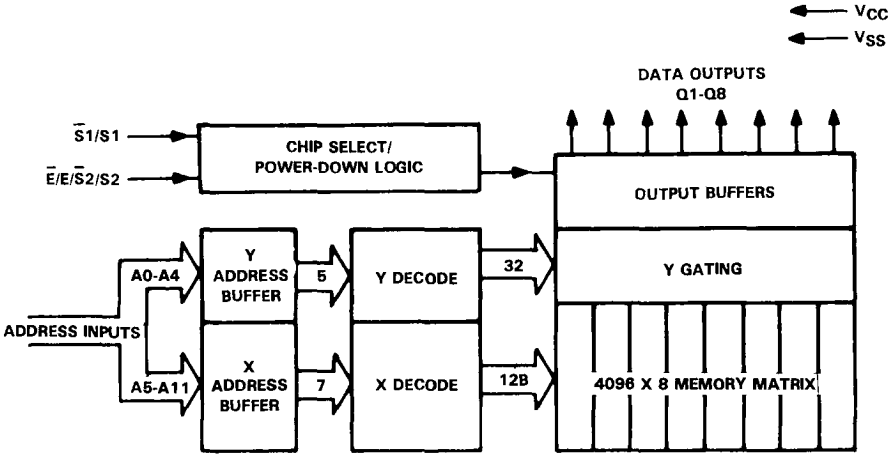
logic symbol†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pins 18 and 20 can be active high as shown in the upper symbol or active low as shown in the lower (partial) symbol. In addition, pin 20 can be either a second chip-select ($\overline{S}2$ or S2) or a chip-enable/power-down ($\overline{E}$ or E) pin.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

functional block diagram



absolute maximum ratings

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Output voltage range (see Note 1) . . . . . −1 V to 7 V
Input voltage range (see Note 1) . . . . . −1 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−1		0.8	V
T_A	Opereting free-air temperature	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} output not loaded		60	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			15	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (see Figure 1)†

PARAMETER		TMS2364-15		TMS2332-20		TMS2332-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200		250	ns
$t_{a(S)}$	Access time from chip select		120		120		120	ns
$t_{a(PD)}$	Access time from chip enable/power down		150		200		250	ns
$t_{v(A)}$	Output data valid after address change	0		0		0		ns
t_{dis}	Output disable time from chip select/chip enable		100		100		100	ns

† All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

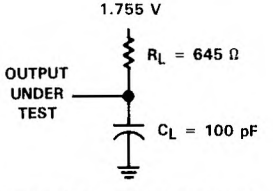
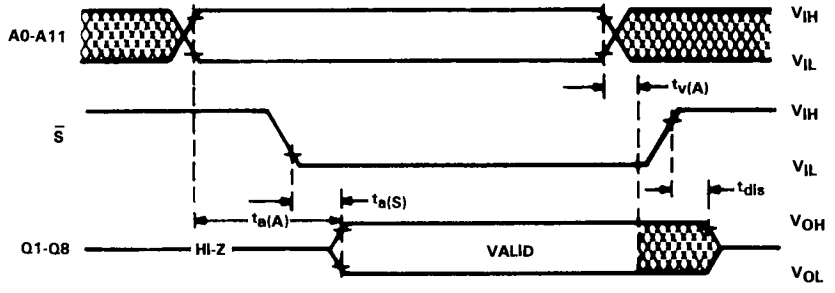


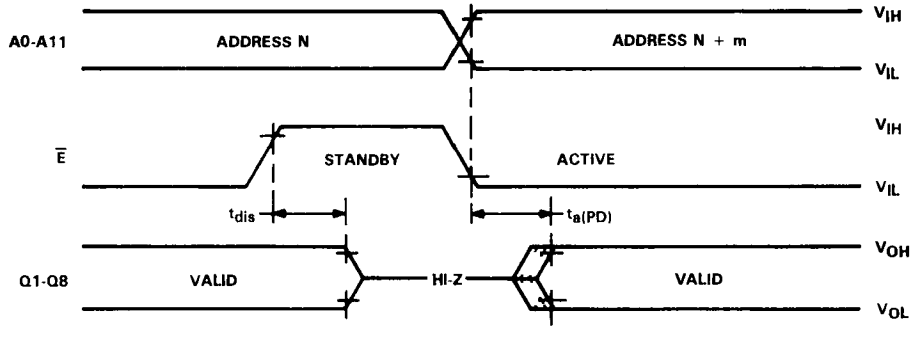
FIGURE 1. LOAD CIRCUIT

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

read cycle timing



standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS2332 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 4,096 8-bit words with address locations numbered 0 to 4,095. The 8-bit words are coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A11 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem. (Contact TI for details on card image transmission.) 32K EPROMS can be used to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____

SPECIFICATION NUMBER: _____

ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO
15 ALPHANUMERIC CHARACTERS PER LINE _____
_____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N)_____

PIN OPTIONS: 1 = HIGH, 0 = LOW, PD = POWER DOWN, CS = CHIP SELECT

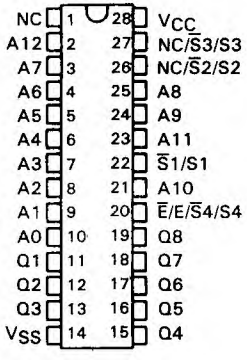
PIN 18: _____ PIN 20: _____ PD/CS: _____

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

SEPTEMBER 1984 — REVISED NOVEMBER 1985

- 8192 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Single 5-V Power Supply
- Optional Power Down or Chip Select
- Maximum Access Time from Address or Power Down
  TMS2364-15 150 ns
  TMS2364-20 200 ns
  TMS2364-25 250 ns
- Pin Compatible with 2764 EPROMs
- Worst Case Active Power Dissipation . . . 330 mW
- Worst Case Standby Power Dissipation . . . 82.5 mW

N PACKAGE
(TOP VIEW)



description

The TMS2364 is a 65,536-bit read-only memory organized as 8192 words of 8-bit length. This makes the TMS2364 ideal for microprocessor-based systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

PIN NOMENCLATURE	
A0-A12	Address Inputs
Ē/E/S̄4/S4	Chip Enable/Power Down or Chip Select
NC	No Connection
Q1-Q8	Data Out
S̄1/S1, S̄2/S2, S̄3/S3	Chip Selects
VCC	5-V Supply
VSS	Ground

The TMS2364 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. Pins 20, 22, 26, and 27 are mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of pins 20, 22, 26, or 27.

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. The device is designed for operation from 0°C to 70°C.

operation

address (A0-A12)

The address-valid interval determines the device cycle time. The 13-bit positive-logic address is decoded on chip to select one of 8192 words of 8-bit length in the memory array. A0 is the least-significant bit and A12 the most-significant bit of the word address.

chip selects ($\overline{S}$1 or S1, $\overline{S}$2 or S2, $\overline{S}$3 or S3)

Pins 26 and 27 can be programmed during mask fabrication to be either chip selects or no connection (NC) at the inputs. Any pin(s) programmed as chip select(s) can also be programmed to be active with either a high- or a low-level input. If pins 26 and 27 are programmed as chip selects, and pins 20, 22, 26, and 27 are active, all eight outputs are enabled; and the eight-bit addressed word can be read. When any of the signals on pins 20, 22, 26, and 27 are not active, all eight outputs are in a high-impedance state. If pins 26 and 27 are programmed as no connection (NC), the previous discussion applies to the remaining active chip select(s).

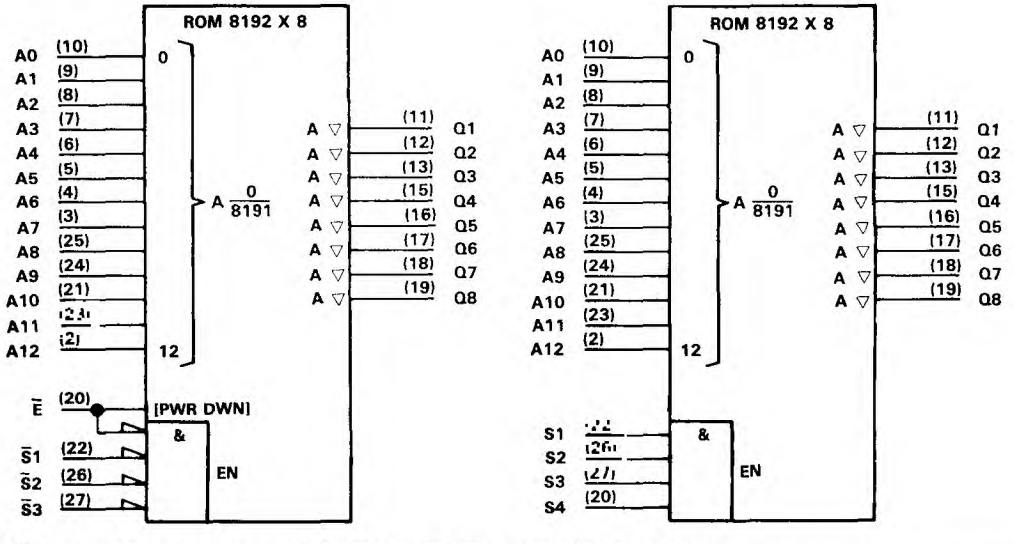
chip enable/power down ($\overline{E}$ or E) or chip select ($\overline{S}$4 or S4)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin ($\overline{E}$ or E) or a fourth chip-select pin ($\overline{S}$4 or S4). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby I_{CC2} of 15 mA. With the chip-select option, pin 20 is functionally identical to pin 22.

data out (Q1-Q8)

The eight outputs must be enabled by pins 20 and 22, and pins 26 and 27 if programmed as chip selects, before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

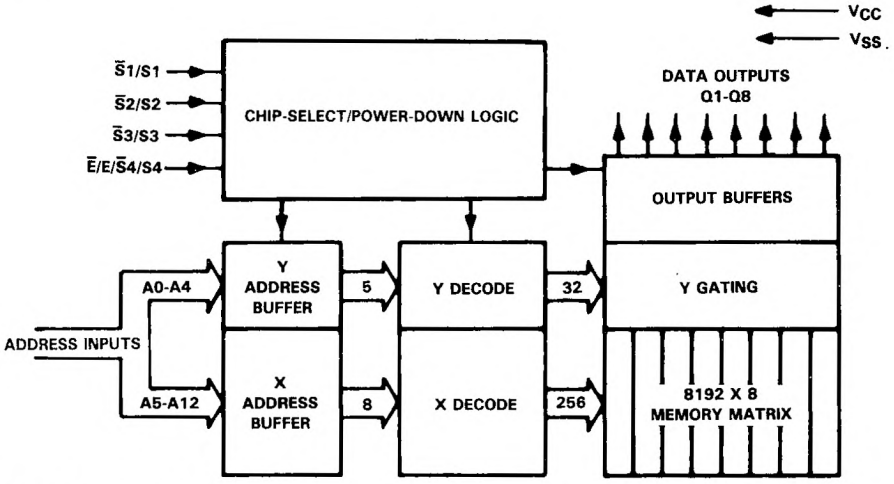
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pins 20 and 22, plus pins 26 and 27 if programmed as chip selects, can be active low as shown in the symbol on the left or active high as shown in the symbol on the right. In addition, pin 20 can be either a fourth chip select ($\overline{S}$4 or S4) or a chip enable/power down ($\overline{E}$ or E).

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

functional block diagram†



† The diagram above assumes that pins 26 and 27 are programmed as chip selects.

absolute maximum ratings

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Output voltage range (see Note 1) . . . . . −1 V to 7 V
Input voltage range (see Note 1) . . . . . −1 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} output not loaded		60	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			15	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (see Figure 1†)

PARAMETER		TMS2364-15		TMS2364-20		TMS2364-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200		250	ns
$t_{a(S)}$	Access time from chip select		120		120		120	
$t_{a(PD)}$	Access time from chip enable/power down		150		200		250	
$t_{v(A)}$	Output data valid after address change	0		0		0		
t_{dis}	Output disable time from chip select/chip enable		100		100		100	

†All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

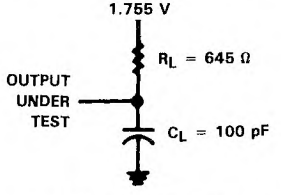
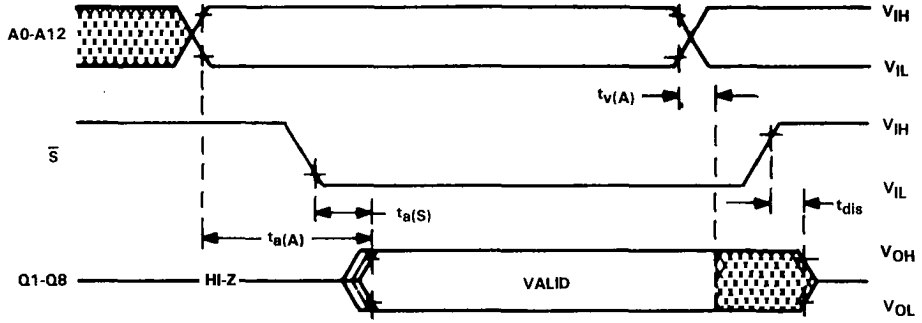


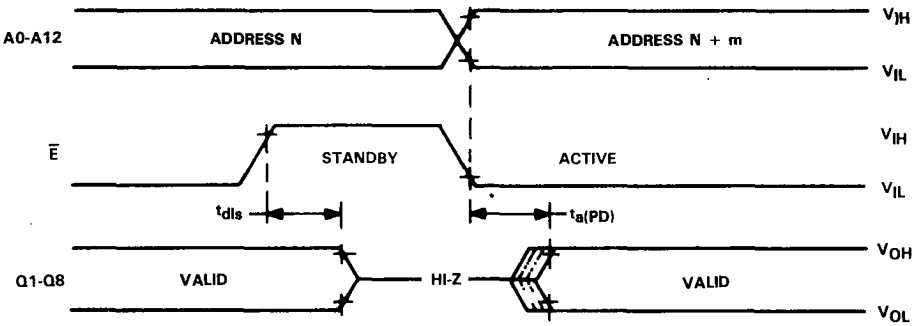
FIGURE 1. LOAD CIRCUIT

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

read cycle timing



standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS2364 is a fixed-program memory in which the programming is *performed* by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 8,192 8-bit words with address locations numbered 0 to 8,191. The 8-bit words can be coded as a 2-bit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A12 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 32K or 64K EPROMS can be used to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____

SPECIFICATION NUMBER: _____

ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO
15 ALPHANUMERIC CHARACTERS PER LINE _____
_____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N)_____

PIN OPTIONS: 1 = HIGH, 0 = LOW, NC = NO CONNECT, PD = POWER DOWN, CS = CHIP SELECT

PIN 20: _____ PIN 22: _____ PD/CS: _____

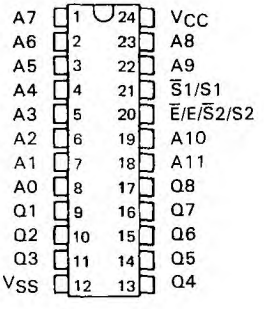
PIN 26: _____ PIN 27: _____

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

MAY 1977 – REVISED NOVEMBER 1985

- 4096 X 8 Organization
- All Inputs and Outputs TTL Compatible
- Fully Static (No Clocks, No Refresh)
- Single 5-V Power Supply
- Maximum Access Time from Address
  TMS4732-15 150 ns
  TMS4732-20 200 ns
  TMS4732-25 250 ns
- Pin-Compatible with TMS2532 EPROM
- Optional Power Down or Chip Select
- Two Output-Enable Controls for Chip Select Flexibility
- Worst Case Active Power Dissipation . . . 330 mW
- Worst Case Standby Power Dissipation . . . 82.5 mW

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A11	Address Inputs
Ē/E/S̄2/S2	Chip Enable/Power Down or Chip Select
Q1-Q8	Data Out
S̄1/S1	Chip Select
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS4732 is a 32,768-bit read-only memory organized as 4,096 words of 8-bit length. This makes the TMS4732 ideal for microprocessor-based systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS4732 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. Pins 20 and 21 are mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of pins 20 and 21.

This ROM is supplied in a 24-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. The device is designed for operation from 0°C to 70°C.

operation

address (A0-A11)

The address-valid interval determines the device cycle time. The 12-bit positive-logic address is decoded on chip to select one of 4096 words of 8-bit length in the memory array. A0 is the least-significant bit and A11 the most-significant bit of the word address.

chip selects (S̄1 or S1 and S̄2 or S2)

Each of these pins can be programmed during mask fabrication to be active with either a high- or a low-level input. When both signals are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either signal is not active, all eight outputs are in a high-impedance state.

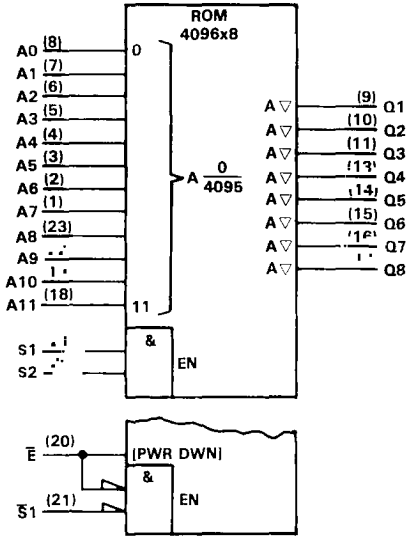
chip enable/power down ($\overline{E}$ or E) or chip select ($\overline{S}2$ or S2)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin ($\overline{E}$ or E) or a secondary chip-select pin ($\overline{S}2$ or S2). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby I_{CC2} of 15 mA. With pin 20 programmed as a chip-select pin, it is functionally identical to pin 21.

data out (Q1-Q8)

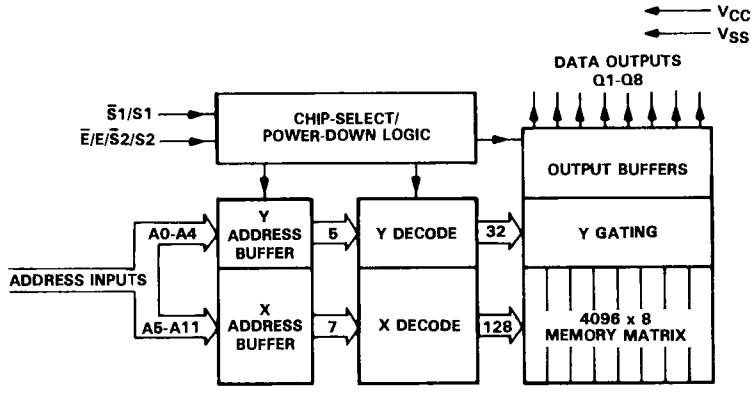
The eight outputs must be enabled by pins 20 and 21 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pins 20 and 21 can be active high as shown in the upper symbol or active low as shown in the lower (partial) symbol. In addition, pin 20 can be either a second chip-select ($\overline{S}2$ or S2) or a chip-enable/power-down ($\overline{E}$ or E) pin.

functional block diagram



absolute maximum ratings

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Output voltage range (see Note 1) . . . . . −1 V to 7 V
Input voltage range (see Note 1) . . . . . −1 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} output not loaded		60	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			15	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (see Figure 1)†

PARAMETER		TMS4732-15		TMS4732-20		TMS4732-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200		250	ns
$t_{a(S)}$	Access time from chip select		120		120		120	ns
$t_{a(PD)}$	Access time from chip enable/power down		150		200		250	ns
$t_{v(A)}$	Output data valid after address change	0		0		0		ns
t_{dis}	Output disable time from chip select or chip enable		100		100		100	ns

† All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

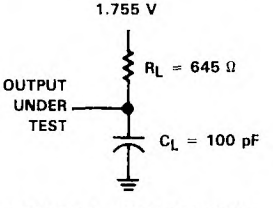


FIGURE 1. LOAD CIRCUIT

TEXAS INSTRUMENTS
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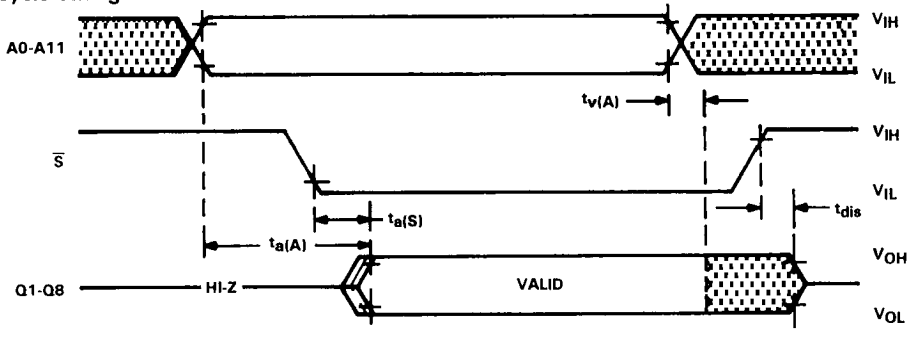
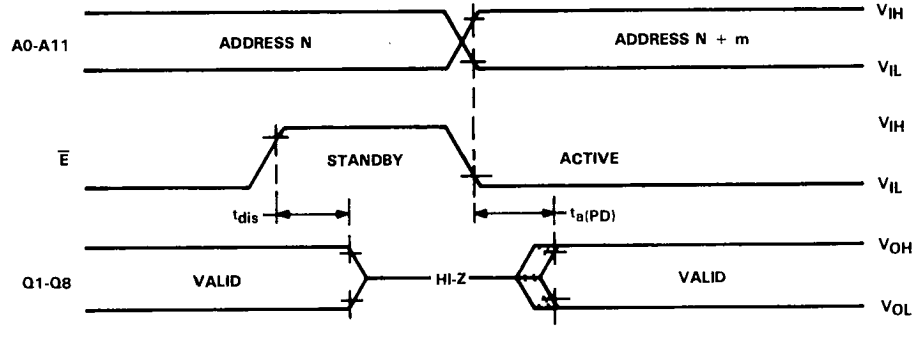
read cycle timing



standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS4732 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 4,096 8-bit words with address locations numbered 0 to 4,095. The 8-bit words can be coded as a 2-bit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A11 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). 32K EPROMS can be used to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____
SPECIFICATION NUMBER: _____
ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO 15 ALPHANUMERIC CHARACTERS PER LINE _____ _____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N) _____

PIN OPTIONS: 1 = HIGH, 0 = LOW, PD = POWER DOWN, CS = CHIP SELECT

PIN 20: _____ PIN 21: _____ PD/CS: _____

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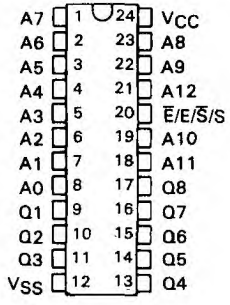
JUNE 1981 – REVISED NOVEMBER 1985

- 8192 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Optional Power Down or Chip Select
- Single 5-V Power Supply
- Maximum Access Time from Address
  TMS4764-15 150 ns
  TMS4764-20 200 ns
  TMS4764-25 250 ns
- Worst Case Active Power Dissipation . . . 330 mW
- Worst Case Standby Power Dissipation . . . 82.5 mW

N PACKAGE
(TOP VIEW)



description

The TMS4764 is a 65,536-bit read-only memory organized as 8,192 words of 8-bit length. This makes the TMS4764 ideal for microprocessor-based systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

PIN NOMENCLATURE	
A0-A12	Address Inputs
Ē/E/S̄/S	Chip Enable/Power Down or Chip Select
Q1-Q8	Data Out
V_{CC}	5-V Supply
V_{SS}	Ground

The TMS4764 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. Pin 20 is mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of pin 20.

This ROM is supplied in a 24-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. The device is designed for operation from 0°C to 70°C.

operation

address (A0-A12)

The address-valid interval determines the device cycle time. The 13-bit positive-logic address is decoded on chip to select one of 8192 words of 8-bit length in the memory array. A0 is the least-significant bit and A12 the most-significant bit of the word address.

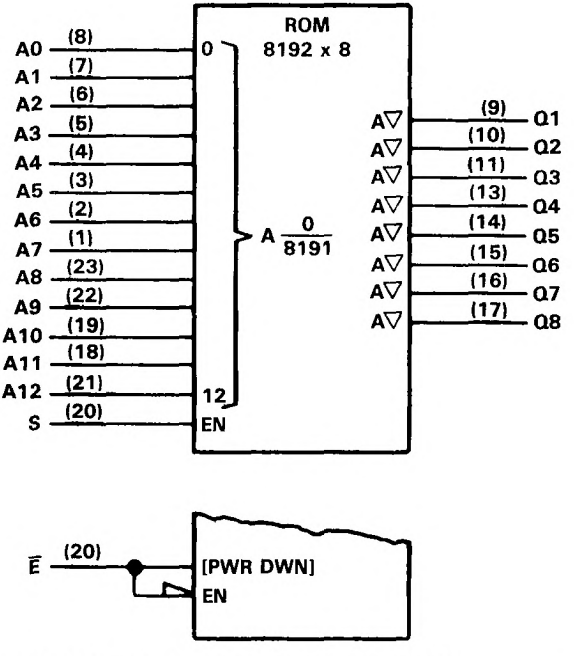
chip enable/power down (Ē or E or chip select S̄ or S)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin (Ē or E) or a chip-select pin (S̄ or S). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1}, which in the active mode is 60 mA, to a standby current of 15 mA. When the signal on pin 20 is active, all eight outputs are enabled and the eight-bit addressed word can be read. When the signal is not active, all eight outputs are in a high-impedance state.

data out (Q1-Q8)

The eight outputs must be enabled by pin 20 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin 20 can be active-high as shown in the upper symbol or active low as shown in the lower (partial) symbol. It can be either a chip select ($\overline{S}$ or S) or a chip enable/power down ($\overline{E}$ or E).

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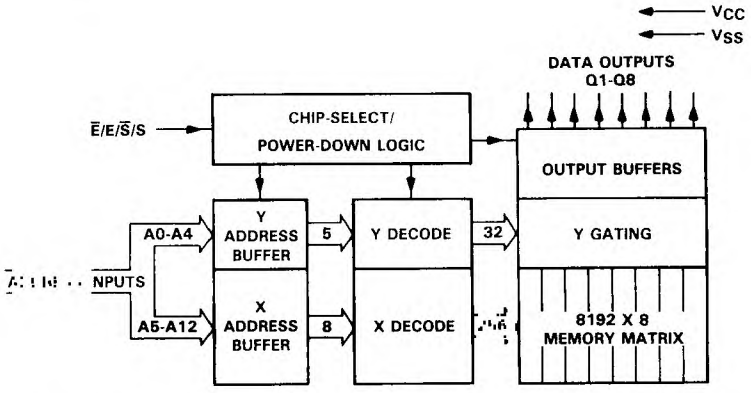
functional block diagram



absolute maximum ratings

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Output voltage range (see Note 1) . . . . . −1 V to 7 V
Input voltage range (see Note 1) . . . . . −1 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} output not loaded		60	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			15	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (see Figure 1)†

PARAMETER		TMS4764-15		TMS4764-20		TMS4764-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200		250	ns
$t_{a(S)}$	Access time from chip select		120		120		120	
$t_{a(PD)}$	Access time from chip enable/power down		150		200		250	
$t_{v(A)}$	Output data valid after address change	0		0		0		
t_{dis}	Output disable time from chip select or chip enable		100		100		100	

†All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

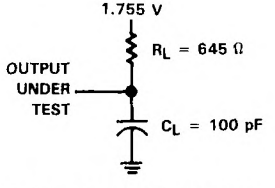
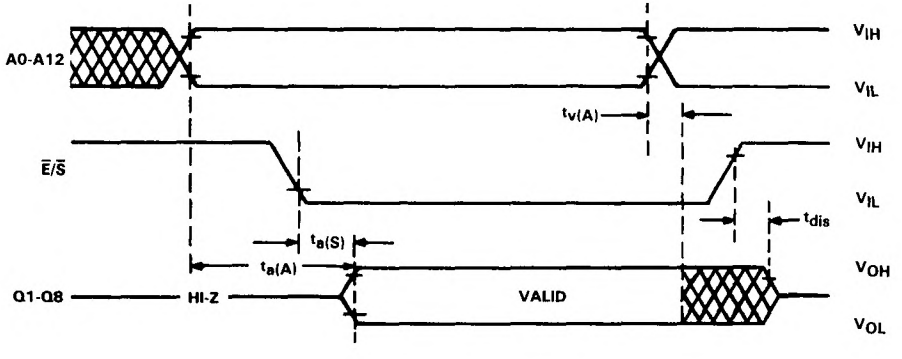


FIGURE 1. LOAD CIRCUIT

read cycle timing



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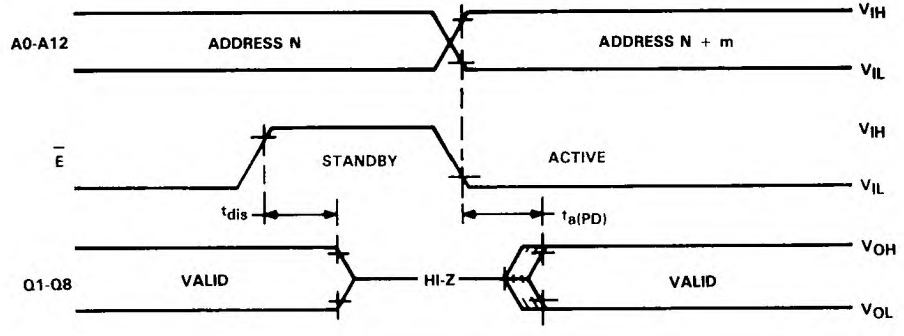
standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS4764 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 8,192 8-bit words with address locations numbered 0 to 8,191. The 8-bit words are coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A12 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formated in card images and transmitted via computer modem. (Contact TI for details on card image transmission.) Either 32K or 64K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____
SPECIFICATION NUMBER: _____
ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO
15 ALPHANUMERIC CHARACTERS PER LINE _____
_____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N)_____

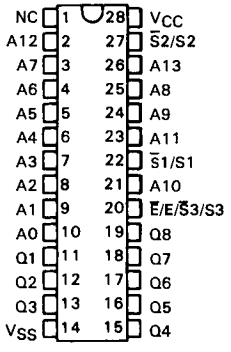
PIN OPTIONS: 1 = HIGH, 0 = LOW, PD = POWER DOWN, CS = CHIP SELECT

PIN 20: _____ PD/CS: _____

JUNE 1983 — REVISED NOVEMBER 1985

- 16,384 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Single 5-V Power Supply
- Optional Power Down or Chip Select
- Maximum Access Time from Address or Power Down
  TMS47128-20 200 ns
  TMS47128-25 250 ns
  TMS47128-35 350 ns
- Pin Compatible with 27128 EPROMs
- Worst Case Active Power Dissipation . . . 330 mW
- Worst Case Standby Power Dissipation . . . 82.5 mW

N PACKAGE
(TOP VIEW)



description

The TMS47128 is a 131,072-bit read-only memory organized as 16,384 words of 8-bit length. This makes the TMS47128 ideal for microprocessor-based systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

PIN NOMENCLATURE	
A0-A13	Address Inputs
Ē/E/S̄3/S3	Chip Enable/Power Down or Chip Select
NC	No Connection
Q1-Q8	Data Out
S̄1/S1, S̄2/S2	Chip Selects
V_{CC}	5-V Supply
V_{SS}	Ground

The TMS47128 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three-state for OR-tying multiple devices on a common bus. Pins 20, 22, and 27 are mask-programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of pins 20, 22 and 27.

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24 mm (600-mil) centers. The device is designed for operation from 0°C to 70°C.

operation, standard ROM

address (A0-A13)

The address-valid interval determines the device cycle time. The 14-bit positive-logic address is decoded on chip to select one of 16,384 words of 8-bit length in the memory array. A0 is the least-significant bit and A13 is the most-significant bit of the word address.

chip select (S̄1 or S1 and S̄2 or S2)

Pins 22 and 27 can be programmed during mask fabrication to be active with either a high- or a low-level input. When the signals on pins 20, 22, and 27 are active, all eight outputs are enabled; and the eight-bit addressed word can be read. When any of the signals on pins 20, 22, and 27 are not active, all eight outputs are in a high-impedence state.

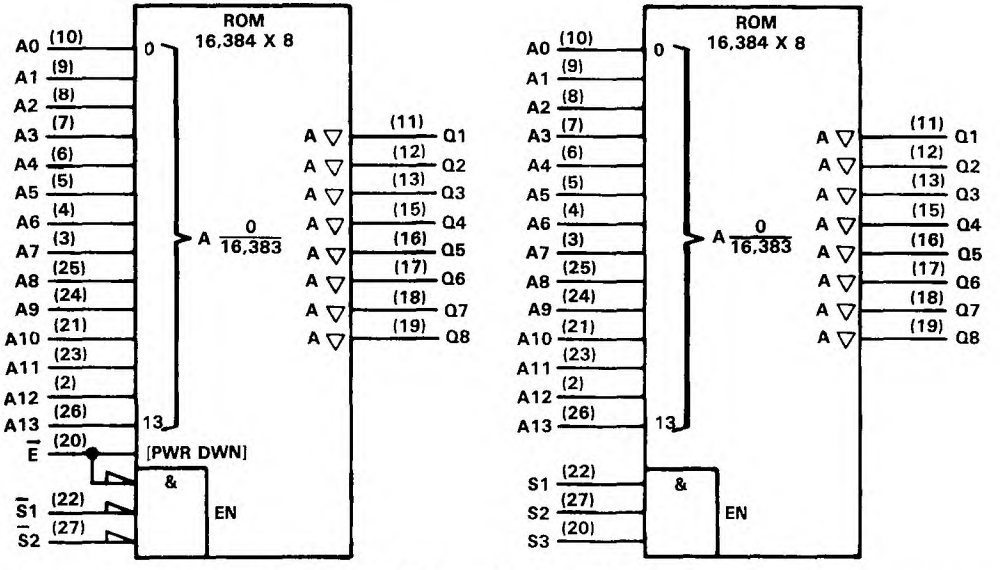
chip enable/power down (E or $\overline{E}$) or chip select (S3 or $\overline{S3}$)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin (E or $\overline{E}$) or a third chip-select pin (S3 or $\overline{S3}$). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby of I_{CC2} 15 mA. With the chip-select option, pin 20 is functionally identical to pins 22 and 27.

data out (Q1-Q8)

The eight outputs must be enabled by pins 20, 22, and 27 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbols†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pins 20, 22 and 27 can be active low as shown in the symbol on the left or active high as shown in the symbol on the right. In addition, pin 20 can be either a third chip select (S3 or $\overline{S3}$) or a chip enable/power down (E or $\overline{E}$).

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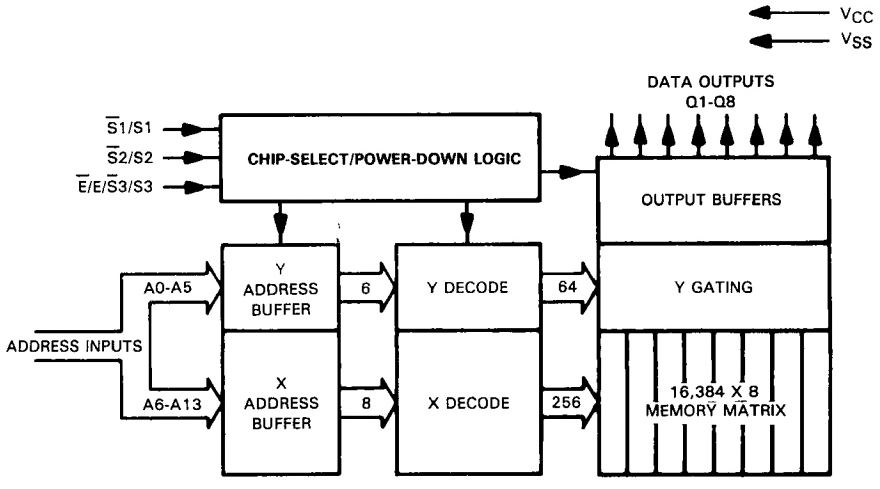
functional block diagram



absolute maximum ratings

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Output voltage range (see Note 1) . . . . . −1 V to 7 V
Input voltage range (see Note 1) . . . . . −1 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} output not loaded		60	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			15	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (see Figure 1)†

PARAMETER		TMS47128-20		TMS47128-25		TMS47128-35		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		200		250		350	ns
$t_{a(S)}$	Access time from chip select		120		120		150	
$t_{a(PD)}$	Access time from power down/chip enable		200		250		350	
$t_{v(A)}$	Output data valid after address change	0		0		0		
t_{dis}	Output disable time from chip select/chip enable		100		100		100	

†All AC measurements are made at 10% and 90% points.

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PARAMETER MEASUREMENT INFORMATION

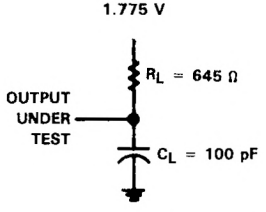
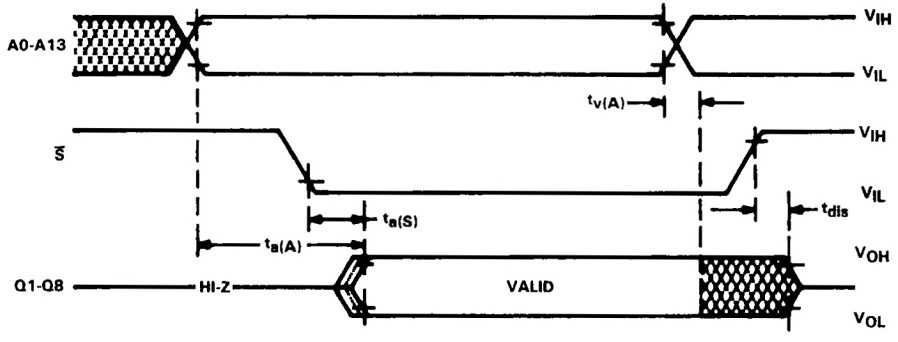
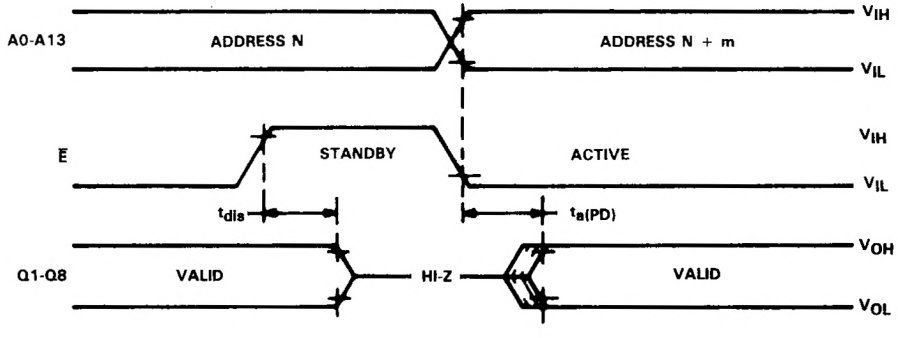


FIGURE 1. LOAD CIRCUIT

read cycle timing



standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47128 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 16,384 8-bit words with address locations numbered 0 to 16,383. The 8-bit words are coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A13 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formated in card images and transmitted via computer modem. (contact TI for details on card image transmission.) Either 64K or 128K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____
SPECIFICATION NUMBER: _____
ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO
15 ALPHANUMERIC CHARACTERS PER LINE _____
_____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N)_____

PIN OPTIONS: 1 = HIGH, 0 = LOW, PD = POWER DOWN, CS = CHIP SELECT

PIN 20: _____ PIN 22: _____ PD/CS: _____

PIN 27: _____

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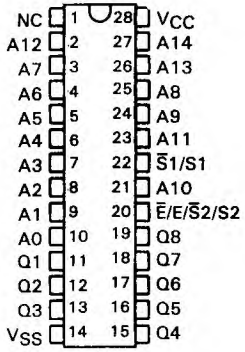
JUNE 1983 — REVISED NOVEMBER 1985

- 32,768 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Single 5-V Power Supply
- Optional Power Down or Chip Select
- Maximum Access Time from Address or Power Down

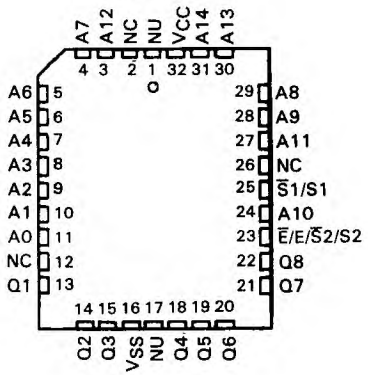
TMS47256-20	200 ns
TMS47256-25	250 ns
TMS47256-30	300 ns

- Worst Case Active Power Dissipation . . . 330 mW
- Worst Case Standby Power Dissipation . . . 82.5 mW
- Pin Compatible with 27256 and 27C256 Type EPROMs

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



description

The TMS47256 is a 262,144-bit read-only memory organized as 32,768 words of 8-bit length. This makes the TMS47256 ideal for microprocessor-based systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS47256 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. Pins 20 and 22 (dual-in-line package) and pins 23 and 25 (chip carrier) are mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of $\overline{E}$ and $\overline{S}$ pins.

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. It is also supplied in a 32-lead plastic leaded chip carrier package designed for surface mount applications using 1,25-mm (50-mil) lead spacing. Both package styles conform to JEDEC standards. The device is designed for operation from 0°C to 70°C.

PIN NOMENCLATURE	
A0-A14	Address Inputs
$\overline{E}$/E/$\overline{S}$2/S2	Chip Enable/Power Down or Chip Select
NC	No Connection
NU	Make No External Connection
Q1-Q8	Data Out
$\overline{S}$1/S1	Chip Select
V_{CC}	5-V Supply
V_{SS}	Ground

operation

address (A0-A14)

The address-valid interval determines the device cycle time. The 15-bit positive-logic address is decoded on chip to select one of 32,768 words of 8-bit length in the memory array. A0 is the least-significant bit and A14 is the most-significant bit of the word address.

chip select ($\overline{S}1$ or S1)

Pin 22 (dual-in-line package) and pin 25 (chip carrier) can be programmed during mask fabrication to be active with either a high- or low-level input. When the signal on both pins 22 and 20 (dual-in-line package) and pins 23 and 25 (chip carrier) are active, all eight outputs are enabled; and the eight-bit addressed word can be read. When the signal on either of these pins is not active, all eight outputs are in a high-impedance state.

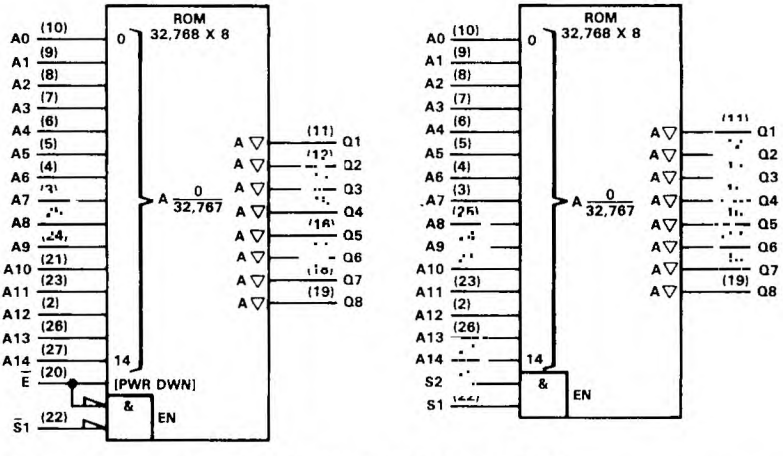
chip enable/power down ($\overline{E}$ or E) or chip select ($\overline{S}2$ or S2)

Pin 20 (dual-in-line package) and pin 23 (chip carrier) can be programmed during mask fabrication to be a chip-enable/power down pin ($\overline{E}$ or E) or a secondary chip-select pin ($\overline{S}2$ or S2). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put in the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby I_{CC2} of 15 mA. With the chip-select option, pin 20 is functionally identical to pin 22 for the dual-in-line package and pin 23 is functionally identical to pin 25 for the chip carrier.

data out (Q1-Q8)

The eight outputs must be enabled by the $\overline{E}$ and $\overline{S}$ pins before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

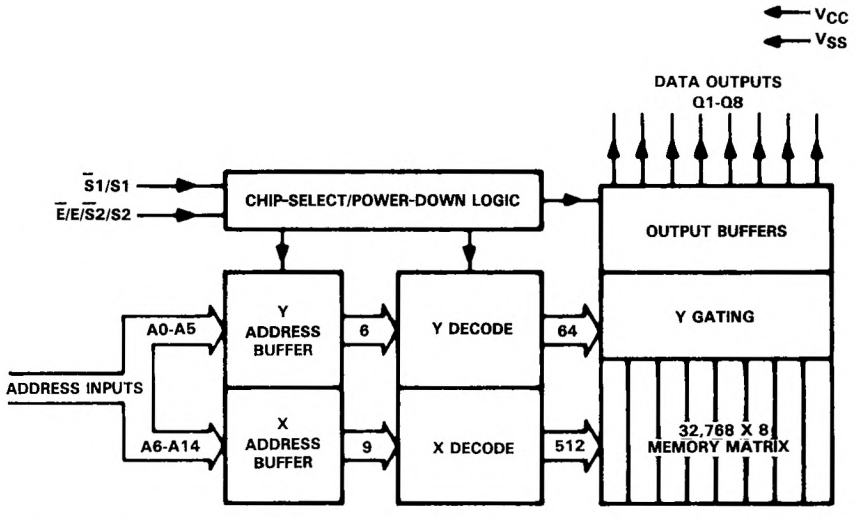
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pins 20 and 22 can be active low as shown in the symbol on the left or active high as shown in the symbol on the right. In addition, pin 20 can be either a secondary chip select (S2 or $\overline{S}2$) or a chip enable/power down (E or $\overline{E}$). The pin numbers shown are for the 28-pin dual-in-line package.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1) . . . . . −0.5 V to 7 V
Applied output voltage (see Note 1) . . . . . −1 V to 7 V
Applied input voltage (see Note 1) . . . . . −1 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} Output not loaded		60	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			15	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (see Figure 1)†

PARAMETER		TMS47256-20		TMS47256-25		TMS47256-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(AD)}$	Access time from address		200		250			ns
$t_{a(S)}$	Access time from chip select		120		120			
$t_{a(PD)}$	Access time from power down/chip enable		200		250			
$t_{v(A)}$	Output data valid after address change	0		0		0		
t_{dis}	Output disable time from chip select/chip enable				100			

†All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

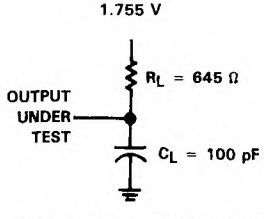
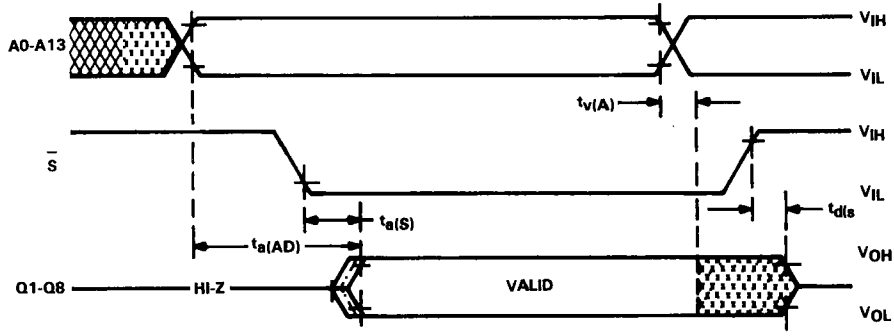


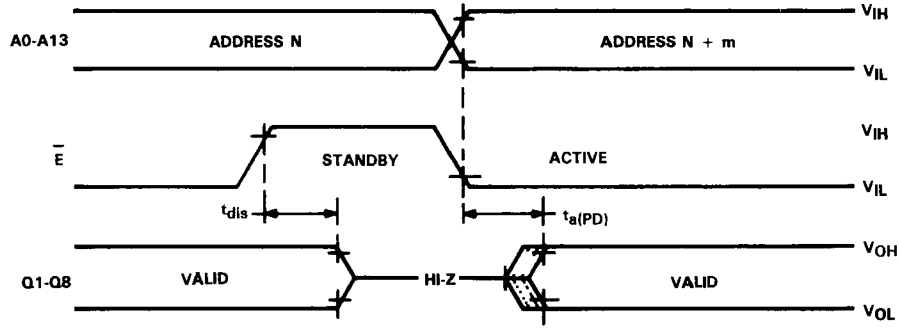
FIGURE 1. LOAD CIRCUIT

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

read cycle timing



standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47256 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 32,768 8-bit words with address locations numbered 0 to 32,767. The 8-bit words are coded as a 2-digit hexadecimal number from 00 and FF. Q1 is considered the least-significant bit and Q8 is the most-significant bit. For addresses, A0 is the least-significant bit and A14 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 64K, 128K, or 256K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____
SPECIFICATION NUMBER: _____
ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO
15 ALPHANUMERIC CHARACTERS PER LINE _____
_____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N)_____ SURFACE MOUNT (FM)_____

PIN OPTIONS: 1 = HIGH, 0 = LOW, PD = POWER DOWN, CS = CHIP SELECT

N PACKAGE: PIN 20 _____ PIN 22 _____ PD/CS _____

FM PACKAGE: PIN 23 _____ PIN 25_____ PD/CS _____

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

TMS47C256
32,768-WORD BY 8-BIT READ-ONLY MEMORY

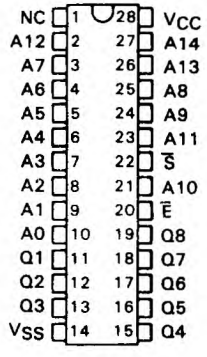
NOVEMBER 1985

- 32,768 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Single 5-V Power Supply
- HVCMOS Technology
- Maximum Access Time from Address or Power Down

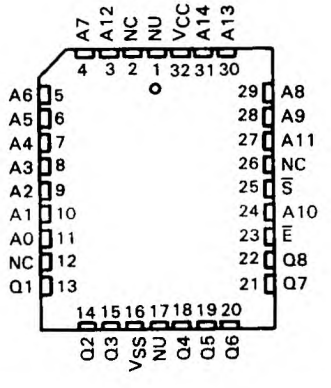
TMS47C256-15	150 ns
TMS47C256-20	200 ns
TMS47C256-25	250 ns

- Pin Compatible with 27256 EPROMs
- Worst Case Active Power Dissipation . . . 275 mW
- Worst Case Standby Power Dissipation . . . 2.8 mW

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



description

The TMS47C256 is a 262,144-bit read-only memory organized as 32,768 words of 8-bit length. This makes the TMS47C256 ideal for microprocessor-based systems. The device is fabricated using HVCMOS technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS47C256 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of the chip-select pin(s).

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. It is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing. Both package styles conform to JEDEC standards. The device is designed for operation from 0°C to 70°C.

PIN NOMENCLATURE	
A0-A14	Address Inputs
$\overline{E}$	Chip Enable/Power Down
NC	No Connection
NU	Make No External Connection
Q1-Q8	Data Out
$\overline{S}$	Chip Select
V_{CC}	5-V Supply
V_{SS}	Ground

operation

address (A0-A14)

The address-valid interval determines the device cycle time. The 15-bit positive-logic address is decoded on-chip to select one of 32,768 words of 8-bit length in the memory array. A0 is the least-significant bit and A14 the most-significant bit of the word address.

chip select ($\overline{S}$)

When the signal on both the chip-select and chip-enable/power-down pins are active, all eight outputs are enabled; and the 8-bit addressed word can be read. When the signal on either the chip-select or the chip-enable/power-down pin is not active, all eight outputs are in a high-impedance state.

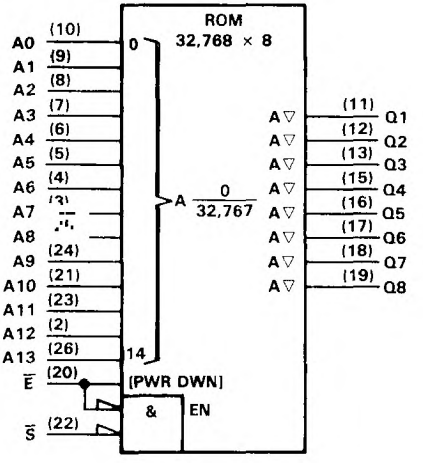
chip enable/power down ($\overline{E}$)

When the chip-enable/power-down pin is inactive, the chip is put in the standby mode. This reduces I_{CC1}, which in the active state is 50 mA, to a standby I_{CC2} of 500 μA. In this mode all outputs are in a high-impedance state.

data out (Q1-Q8)

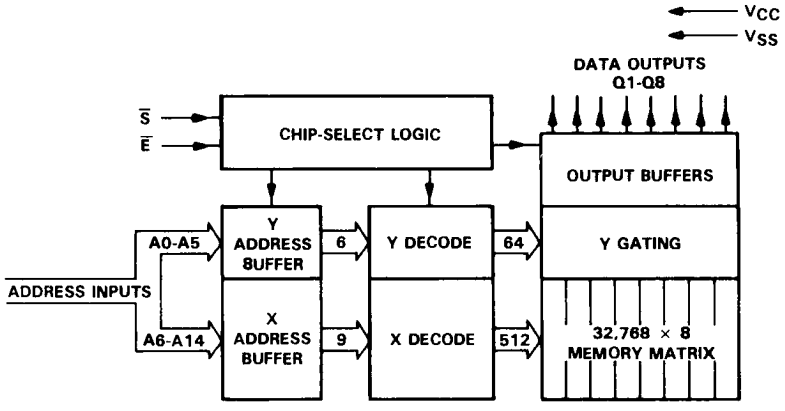
The eight outputs must be enabled by the chip-select and chip-enable/power-down pins before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 28-pin dual-in-line package.

functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1) . . . . . -0.5 V to 7 V
Applied output voltage (see Note 1) . . . . . -0.3 V to V_{CC} + 0.3 V
Applied input voltage (see Note 1) . . . . . -0.3 V to V_{CC} + 0.3 V
Power dissipation . . . . . 300 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . -55°C to 150°C

NOTE 1: Voltage values are with raspact to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	-0.5		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} Output not loaded		50	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			500	μA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (see Figure 1)†

PARAMETER		TMS47C256-15		TMS47C256-20		TMS47C256-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200		250	ns
$t_{a(S)}$	Access time from chip select		75		75		100	
$t_{a(PD)}$	Access time from power down/chip enable		150		200		250	
$t_{v(A)}$	Output data valid after address change	0		0		0		
t_{dis}	Output disable time from chip select/chip enable		60		60		60	

†All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

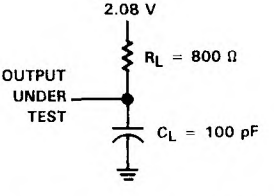
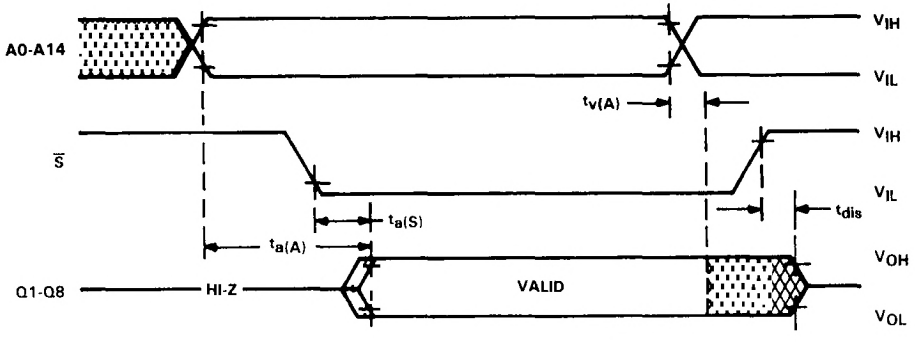


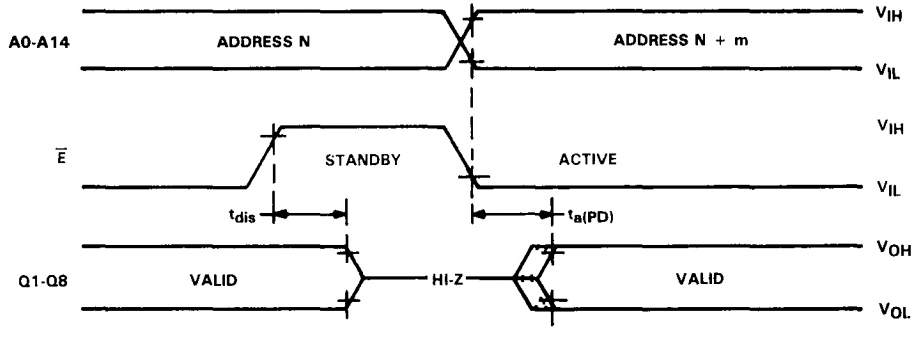
FIGURE 1. LOAD CIRCUIT

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

read cycle timing



standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47C256 is a fixed program memory in which the programming is *performed* by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 32,768 8-bit words with address locations numbered 0 to 32,767. The 8-bit words are coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A14 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 64K, 128K, or 256K EPROMs can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____
SPECIFICATION NUMBER: _____
ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO
15 ALPHANUMERIC CHARACTERS PER LINE _____
_____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N)_____ SURFACE MOUNT (FM)_____

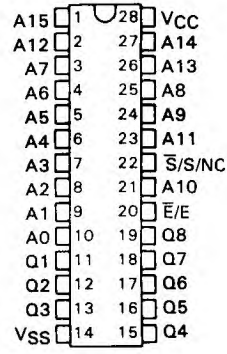
TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

TMS47C512
65,536-WORD BY 8-BIT READ-ONLY MEMORY

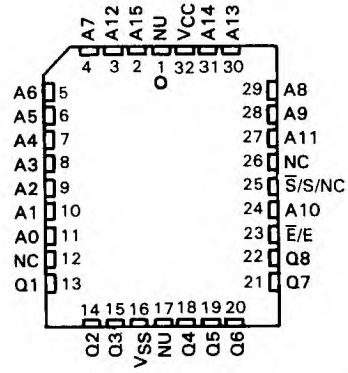
NOVEMBER 1985

- 65,536 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL and CMOS Compatible
- Single 5-V Power Supply
- Standby Mode for Minimum Power Usage
- Maximum Access Time from Address or Power Down
  TMS47C512-20 200 ns
  TMS47C512-25 250 ns
  TMS47C512-30 300 ns
- Pin Compatible with 27512 EPROMs

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



description

The TMS47C512 is a 524,288-bit read-only memory organized as 65,536 words of 8-bit length. This makes the TMS47C512 ideal for microprocessor-based systems. The device is fabricated using HVCMOS technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS47C512 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. The chip-select and chip-enable/power-down pins are mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of the chip-select and chip-enable/power-down pins.

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. It is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing. Both package styles conform to JEDEC standards. The device is designed for operation from 0°C to 70°C.

PIN NOMENCLATURE	
A0-A15	Address Inputs
Ē/E	Chip Enable/Power Down
NC	No Connection
NU	Make No External Connection
Q1-Q8	Data Out
S̄/S	Chip Select
V_{CC}	5-V Supply
V_{SS}	Ground

operation

address (A0-A15)

The address-valid interval determines the device cycle time. The 16-bit positive-logic address is decoded on-chip to select one of 65,636 words of 8-bit length in the memory array. A0 is the least-significant bit and A15 is the most-significant bit of the word address.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

chip select ($\overline{S}$ or S)

The chip-select pin (pin 23 for the dual-in-line package and pin 25 for the chip carrier) can be programmed during mask fabrication to be active with either a high- or low-level input. When the signal on both the chip-select and chip-enable/power-down pins are active, all eight outputs are enabled; and the 8-bit addressed word can be read. When the signals on the chip-select and chip-enable/power-down pins are not active, all eight outputs are in a high-impedance state. Pin 22 (dual-in-line package) and pin 25 (chip carrier) can also be programmed as a no connection if only a chip enable is required.

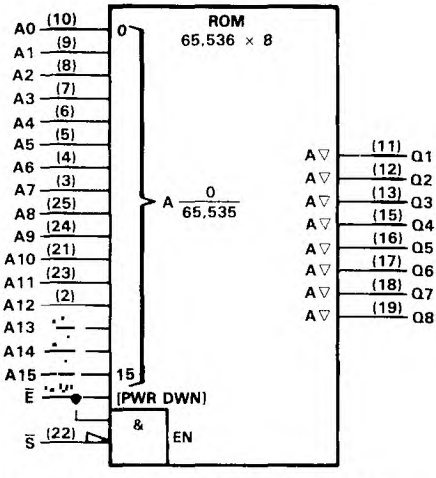
chip enable/power down ($\overline{E}$)

The chip-enable/power-down pin (pin 20 for the dual-in-line package and pin 23 for the chip carrier) can be programmed during mask fabrication to be active with either a high-level or low-level input. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. In this mode all outputs are in the high-impedance state.

data out (Q1-Q8)

The eight outputs must be enabled by the chip-select and chip-enable/power-down pins before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 28-pin dual-in-line package. Pins 20 and 22 can be active low as shown in the symbol above or active high. In addition, pin 22 can be a no connection.

TEXAS INSTRUMENTS
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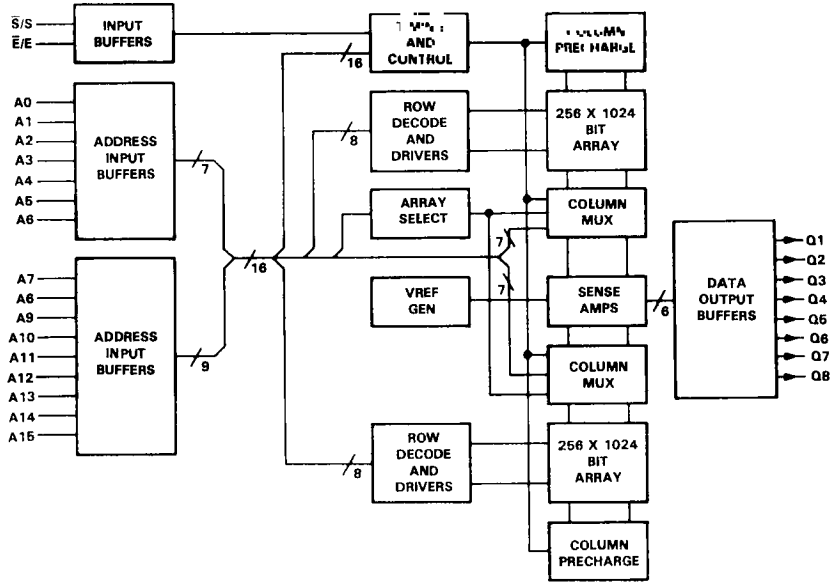
functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1) . . . . . −0.5 V to 7 V
Applied output voltage (see Note 1) . . . . . −0.3 V to V_{CC} + 0.3 V
Applied input voltage (see Note 1) . . . . . −0.3 V to V_{CC} + 0.3 V
Power dissipation . . . . . T.B.D.
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	−0.5		0.8	V
T_A	Operating free-air temperature	0		70	°C

Additional information on these products can be obtained from the factory as it becomes available.

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input leakage current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} Output not loaded		T.B.D.	
I_{CC2}	Supply current from V_{CC} (standby)	V_{CC} = 5.5 V			T.B.D.	
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		10	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		15	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TMS47C512-20		TMS47C512-25		TMS47C512-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		200		250		300	ns
$t_{a(S)}$	Access time from chip select		100		100		100	
$t_{a(PD)}$	Access time from power down/chip enable		200		250		300	
$t_{v(A)}$	Output data valid after address change	0		0		0		
t_{dis}	Output disable time from chip select		100		100		100	

†All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

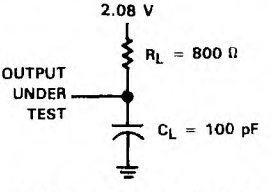


FIGURE 1. LOAD CIRCUIT

Additional information on these products can be obtained from the factory as it becomes available.

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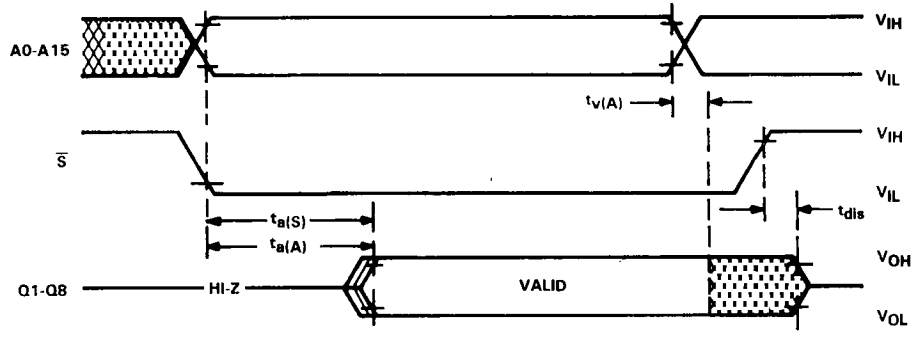
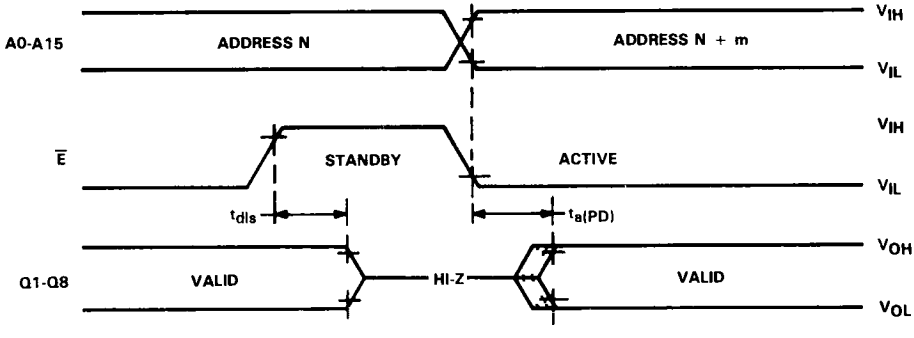
read cycle timing



standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47C512 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code requirements. The device is organized as 65,536 8-bit words with address locations numbered 0 to 65,535. The 8-bit words can be coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A15 is the most significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 64K, 128K, 256K, or 512K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____
SPECIFICATION NUMBER: _____
ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO 15 ALPHANUMERIC CHARACTERS PER LINE _____ _____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N) _____ SURFACE MOUNT (FM) _____

PIN OPTIONS: 1 = HIGH, 0 = LOW.

N PACKAGE:	PIN 20: _____	PIN 22: _____
PLCC:	PIN 23: _____	PIN 25 _____

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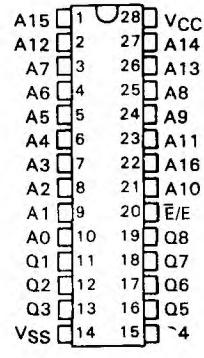
TMS47C1024
131,072-WORD BY 8-BIT READ-ONLY MEMORY

NOVEMBER 1985

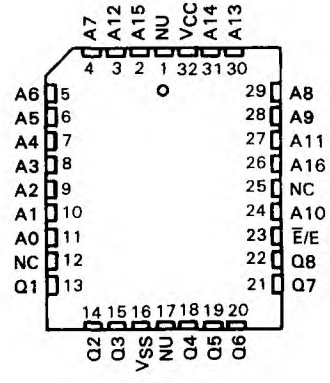
- **131,072 X 8 Organization**
- **Fully Static (No Clocks, No Refresh)**
- **All Inputs and Outputs TTL and CMOS Compatible**
- **Single 5-V Power Supply**
- **Standby Mode for Minimum Power Usage**
- **Maximum Access Time from Address or Power Down**

TMS47C1024-20	200 ns
TMS47C1024-25	250 ns
TMS47C1024-30	300 ns

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



description

The TMS47C1024 is a 1,048,576-bit read-only memory organized as 131,072 words of 8-bit length. This makes the TMS47C1024 ideal for microprocessor-based systems. The device is fabricated using HVCMOS technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS47C1024 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. The chip-enable/power-down pin is mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of the chip-enable/power-down pin.

This ROM is supplied in a 28-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. It is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing. Both package styles conform to JEDEC standards. The device is designed for operation from 0°C to 70°C.

PIN NOMENCLATURE	
A0-A16	Address Inputs
$\overline{E}$/E	Chip Enable/Power Down
NC	No Connection
NU	Make No Internal Connection
Q1-Q8	Data Out
V_{CC}	5-V Supply
V_{SS}	Ground

operation

address (A0-A16)

The address-valid interval determines the device cycle time. The 17-bit positive-logic address is decoded on-chip to select one of 131,072 words of 8-bit length in the memory array. A0 is the least-significant bit and A16 is the most-significant bit of the word address.

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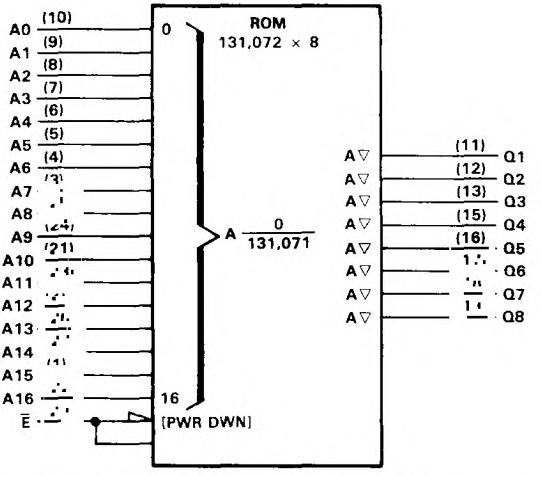
chip-enable/power down ($\overline{E}$ or E)

The chip-enable/power-down pin can be programmed during mask fabrication to be active with either a high- or low-level input. When the signal on the chip-enable/power-down pin is active, all eight outputs are enabled; and the 8-bit addressed word can be read. When the signal on the chip-enable/power-down pin is not active, all eight outputs are in a high-impedance state and the device goes into a standby current mode.

data out (Q1-Q8)

The eight outputs must be enabled by the chip-enable/power-down pin before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 28-pin dual-in-line package. Pin 20 can be active low as shown in the symbol above or active high.

TEXAS INSTRUMENTS
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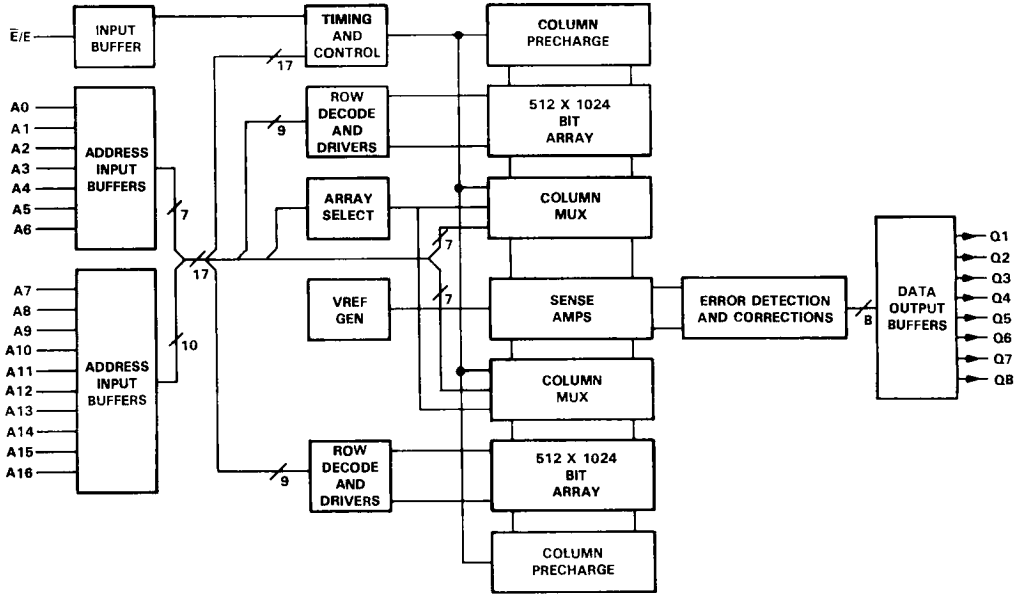
functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1) . . . . . −0.5 V to 7 V
Applied output voltage (see Note 1) . . . . . −0.3 V to V_{CC} + 0.3 V
Applied input voltage (see Note 1) . . . . . −0.3 V to V_{CC} + 0.3 V
Power dissipation . . . . . T.B.D.
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	−0.5		0.8	V
T_A	Operating free-air temperature	0		70	°C

Additional information on these products can be obtained from the factory as it becomes available.

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input leakage currant	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		±10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} Output not loaded		T.B.D.	
I_{CC2}	Supply current from V_{CC} (standby)	V_{CC} = 5.5 V			T.B.D.	
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		10	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		15	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (see Figure 1)†

PARAMETER		TMS47C1024-20		TMS47C1024-25		TMS47C1024-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		200		250		300	ns
$t_{a(E)}$	Access time from chip enable		200		250		300	
$t_{v(A)}$	Output data valid after address change	0		0		0		
t_{dis}	Output disable time from chip enable		100		100		100	

†All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

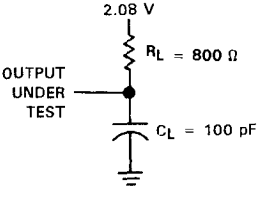


FIGURE 1. LOAD CIRCUIT

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
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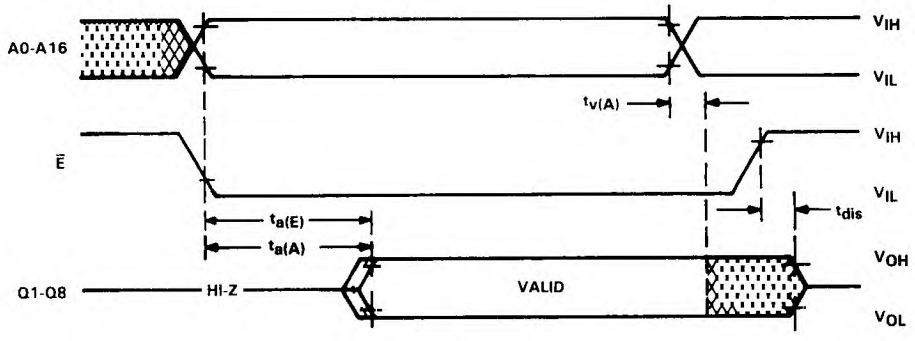
read cycle timing



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS47C1024 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 131,072 8-bit words with address locations numbered 0 to 131,071. The 8-bit words can be coded as a 2-digit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A16 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). Either 64K, 128K, 256K, 512K, or 1024K EPROMS can be used or any combination of them to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____
SPECIFICATION NUMBER: _____
ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO
15 ALPHANUMERIC CHARACTERS PER LINE _____
_____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N) _____ SURFACE MOUNT (FM)_____

PIN OPTIONS: 1 = HIGH, 0 = LOW

N PACKAGE: PIN 20: _____
PLCC: PIN 23 _____