



ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximumrated voltages to these high-impedance circuits.

Unused inputs must always be connected to an appropriate logic voltage level, preferably either supply voltage or ground.

Additional information concerning the handling of ESD sensitive devices is provided in Section 12 in a document entitled *''Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies.''*

MBER 1985

		JULY 1984 - REVISED NOVEMBER
•	65,536 X 5 Organization	P SINGLE-IN-LINE PACKAGE
•	Single 5-V Supply (10% Tolerance)	(TOP VIEW)
•	35-Pin Single-in-Line Package (SIP)	
•	Utilizes Five Multiport Video RAMs in Plastic Chip Carriers	SOE (2) SIN1 (3) SOUT1 (4)
•	Serial In/Serial Out Capability	
•	Dual Accessibility — One Port Sequential Access, One Port Random Access	$\begin{array}{c} \hline CAS1 & (6) \\ A0 & (7) \\ A1 & (8) \end{array}$
•	Five Serial Shift Registers for Sequential Access Applications, Each Comprised of Four Cascaded 64-Bit Segments	A2 (9) TR/OE (10) SIN2 (11) SOUT2 (12)
•	Designed for both Video and Non-Video Applications	DQ2 (13) CAS2 (14)
•	Fast Serial Port Can Be Configured for Video Data Rates in Excess of 150 MHz	A3 (15) A4 (16) SIN3 (17)
•	TR/QE as Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design	SOUT3 (18) DO3 (19) CAS3 (20)
•	Separate Serial In and Serial Out to Allow Simultaneous Shift In and Out	$\begin{array}{c} A5 \\ A6 \\ (22) \end{array}$
•	Supported by TI's TMS34061 Video System Controller (VSC)	A7 (23) RAS (24) W (25)
•	SOE Simplifies Multiplexing of Serial Data Streams	SIN4 (26)
•	Long Refresh Period 4 ms (256 Cycles)	$\begin{array}{c} DQ4 (28) \\ \hline CAS4 (29) \\ \hline \end{array}$
•	All Inputs, Outputs, Clocks Fully TTL Compatible	SIN5 (30) SOUT5 (31)
•	3-State Outputs	$\begin{array}{c} DQ5 \\ CAS5 \\ (33) \end{array}$
	Performance Ranges:	SCLK (34)
	ACCESS ACCESS READ	V _{DD} (35)
	TIME TIME OR	
	ROW COLUMN WRITE ADDRESS ADDRESS CYCLE	PIN NOMENCLATURE
	(MAX) (MAX) (MIN) TM4161EP5-15 150 ns 100 ns 240 ns	A0-A7 Address Inputs
	TM4161EP5-20 200 ns 135 ns 315 ns	CAS1-CAS5 Column-Address Strobes DQ1-DQ5 Random-Access Data In/Data Out
٠	Separate CAS Control with Common Data-	RAS Row-Address Strobe
	In and Data-Out Lines	SCLK Serial Data Clock
•	Low Power Dissipation: —Operating 1250 mW (Typ) —Standby 400 mW (Typ)	SIN1-SIN5 Serial Data In SOE Serial Output Enable SOUT1-SOUT5 Serial Data Out
•	Operating Free-Air Temperature 0°C to	TR/QE Register Transfer/Q Output Enable VDD 5-V Supply

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warenty. Production processing does not necessarily include testing of all parameters.

70°C

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Write Enable

Ground



Vss

W

description

The TM4161EP5 is a 320K dual-access dynamic random-access memory module organized as $65,536 \times 5$ -bits in a 35-pin single-in-line package comprising five TMS4161FML, $65,536 \times 1$ -bit Multiport Video RAMs in 22-lead plastic chip carriers mounted on top of a substrate together with five decoupling capacitors. The random-access port makes the module look like it is organized as 65,536 words of five bits each. The sequential-access port is interfaced to five internal 256-bit dynamic shift registers each organized as four cascaded 64-bit shift register segments which are accessed serially. One, two, three, or four 64-bit shift register segments can be sequentially read out after a transfer cycle depending on a two-bit code applied to the two most significant column address inputs.

The TM4161EP5 features full asynchronous dual access capability except when transferring data between the shift registers and the memory array.

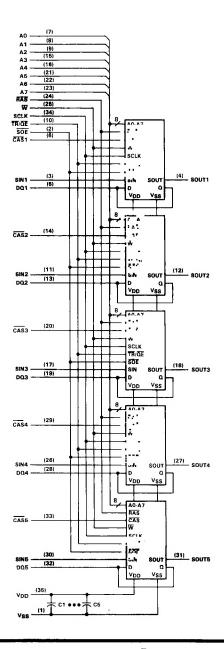
Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with RAS in order to retain data. CAS can remain high during the refresh sequence to conserve power. Note that the transfer of a row of data from the memory array to the shift registers also refreshes that row.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

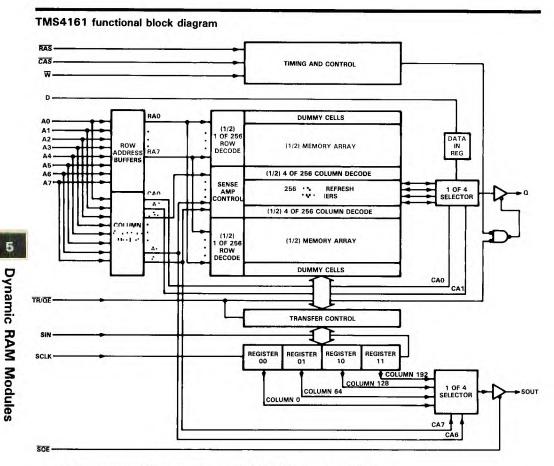
The TM4161EP5 is guaranteed for operation from 0°C to 70°C.



functional block diagram







random-access address space to sequential address space mapping

The TM4161EP5 is designed with each row divided into four, 64-column sections which map directly onto the four segments of each shift register (see TMS4161 functional block diagram). The first column section to be shifted out is selected by the two most-significant column-address bits. If the two bits represent binary 00, then one to four register segments can be shifted out in order. If the two bits represent binary 01, then only 1 to 3 (the most significant) register segments can be shifted out in order. If the two bits represent 10, then one to two of the most-significant register segments can be shifted out in order. If the two bits represent 10, then one to two of the most-significant register segment can be shifted out in order. All register segments are shifted out with the least-significant bit (bit 0) first and the most-significant bit (bit 63) last. Note that if the two column-address bits equal 00 during the last register transfer cycle (TR/ $\overline{\Omega}$ E at logic level "0" as RAS falls) a total of 256 bits can be sequentially read out of each serial output pin.



5-6

random-access operation

TR/QE

The TR/QE pin has two functions. First, it selects either register transfer or random-access operation as RAS falls, and second, during a random-access operation, it functions as an output enable after CAS falls.

To use the TM4161EP5 in the random-access mode, $\overline{TR}/\overline{\Omega E}$ must be high as \overline{RAS} falls. Holding $\overline{TR}/\overline{\Omega E}$ high as RAS falls keeps the 256 elements of the shift registers disconnected from the corresponding 256 bit lines of the memory array. If data is to be shifted, the shift registers must be disconnected from the bit lines. Holding TR/QE low as RAS falls enables the 256 switches that connect the shift registers to the bit lines and indicates that a transfer will occur between the shift registers and one of the memory rows.

During random-access operation, once CAS has been pulled low, TR/QE controls when the data will appear at the Q output (if this is a read cycle). Whenever $\overline{TR}/\overline{QE}$ is held high during random-access operation, the Q output will be in the high-impedance state. This feature removes the possibility of an overlap between data on the address lines and data appearing on the Q output making it possible to connect the address lines to the Q and D lines (Use of this organization prohibits the use of the early write cycle.).

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe (RAS). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe (CAS). All addresses must be stable on or before the falling edges of RAS and CAS. RAS is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. CAS is used as a chip select activating the column decoder and the input and outputs buffers.

write enable (W)

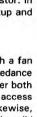
The read or write mode is selected through the write-enable (\overline{W}) input. A logic high on the \overline{W} input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM4161EP5 dictates the use of early write cycles to prevent contention on DQ. When \overline{W} goes low prior to \overline{CAS} , the data outputs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ5)

Data is written during a write or read-modify-write cycle. The falling edge of CAS or W strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, W is brought low prior to CAS and the data is strobed in by CAS with setup and hold times referenced to this signal.

data out (DQ1-DQ5)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data C:* i- the same polarity as data in. The output is in the high-impedance $\cdot \cdots$ ng) state as long as \overline{CAS} or $\overline{TR} \cdot i$ is held high. Data will not appear on the output until after both ** and TR/QE have been brought low. In a read cycle, the guaranteed maximum output enable access time is valid only if tCOE is greater than tCOE MAX, and tRLCL is greater than tRLCL MAX. Likewise, ta(C) MAX is valid only if tRLCL is greater than tRLCL MAX. Once the output is valid, it will remain valid while CAS and TR/QE are both low; CAS or TR/QE going high will return the output to a high-impedance state. In an early write cycle, the output is always in a high-impedance state. In a register transfer cycle, the output will always be in a high-impedance state.





refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in high-impedance state unless CAS is applied, the RAS-only refresh : ... nce avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with the causes all bits in each row to be refreshed. CAS can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on M1-M5, the row address and RAS are applied to multiple modules. CAS is then decoded to select the proper module.

power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, \overline{RAS} must remain high for 100 μ s immediately prior to initialization. Initialization consists of performing eight \overline{RAS} cycles before proper device operation is achieved.

sequential-access operation

TR/QE

Memory tran \cdots operations involving parallel use of the shift registers are first indicated by bringing $\overline{TR}/\overline{QE}$ low before I: \cdot falls low. This enables the switches connecting the 256 elements of the shift registers to the 256 bit lines of the memory array. The \overline{W} line determines whether the data will be transferred from or to the shift registers.

write enable (W)

In the sequential-access mode, \overline{W} determines whether a transfer will occur from the shift registers to the memory array, or from the memory array to the shift registers. To transfer from the shift registers to the memory array, \overline{W} is held low as \overline{RAS} falls, and, to transfer from the memory array to the shift registers, \overline{W} is held high as \overline{RAS} falls. Thus, reads and writes are always with respect to the memory array. The write setup and hold times are referenced to the falling edge of \overline{RAS} for this mode of operation.

row address (A0 through A7)

Eight address bits are required to select one of \cdots 256 possible rows involved in the transfer of data to or from the shift registers. A0-A7, \overline{W} , and $\overline{TR} \cdots$ are latched on the falling edge of \overline{RAS} .

register column address (A7, A6)

To select one of the four shift register segments within each shift register (transfer from memory to register only), the appropriate 2-bit column address (A7, A6) must be valid when CAS falls. However, the CAS and segment address signals need not be supplied every transfer cycle, only when it is desired to change or select a new segment.

SCLK

Data is shifted in and out on the rising edge of SCLK. This makes it possible to view each shift register as though it were made of 256 rising edge D flip-flops connected D to Q. The TM4161EP5 is designed to work with a wide range duty cycle clock to simplify system design. Note that data will appear at the SOUT pins not only on the rising edge of SCLK but also after an access time of $t_a(RSO)$ from RAS high during a parallel load of the shift registers.

SIN and SOUT

Data is shifted in through the SIN pins and is shifted out through the SOUT pins. The TM4161EP5 is designed such that it requires 3 ns hold time on SIN as SCLK rises. SOUT is guaranteed not to change for at least



8 ns after SCLK rises. When loading data into the shift registers from the serial inputs in preparation for a shift register to memory transfer operation, the serial clock must be clocked an even number of times. To guarantee proper serial clock sequence after power up, a transfer cycle must be initiated before a serial data stream is applied at SIN.

SOE

The serial output enable pin controls the impedance of the serial outputs, allowing multiplexing of more than one bank of TM4161EP5 memories into the same external video circuitry. When SOE is at a logic low level, the SOUTs will be enabled and the proper data read out. When SOE is at a logic high level, the SOUTs will be disabled and be in the high-impedance state.

refresh

The shift registers are also dynamic storage elements. The data held in the registers will be lost unless SCLK goes high to shift the data one bit position, a transfer write operation is invoked, or the data is reloaded from the memory array. See specifications for maximum register data retention times. Important: If the shift registers have remained idle for a time period which exceeds the maximum SCLK high or SCLK low time, the dynamic clock circuits will lose charge. Under these conditions, the shift register clocks must be re-enabled by performing any transfer cycle before data can be shifted into or out of the shift registers.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness Bypass capacitors: Multilayer ceramic Leads: Tin/lead solder coated over phosphor-bronze

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Voltage range on any pin except VDD and data out (see Note 1)
Voltage range on VDD supply and data out with respect to VSS
Short circuit output current
Power dissipation
Operating free-air temperature range
Storage temperature range

[†]Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to VSS.

recommended operating conditions

1		MIN	NOM	MAX	UNIT
VDD	Supply voltage	4.5	5	5.5	V
Vss	Supply voltage		0		V
VIH	High-level input voltage	2.4	١	DD+0.3	V
VIL	Low-level input voltage (see Notes 2 and 3)	-0.6		0.8	۷
TA	Operating free-air temperature	0		70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

Due to input protection circuitry, the applied voltage may begin to clamp at -0.6 V; test conditions must comprehend this occurrence.

4. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.



	PARAMETER	TM4161EP5-15 TM4161EP5-20			TEST CONDITIONS TM4161EP5-15 TM	5-20			
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP [†]	MAX	
Vон	High-level output voltage (DQ1-DQ5, SOUT1-SOUT5)	l _{OH} = -5 mA	2.4			2.4			v
VOL	Low-level output voltage (DQ1-DQ5, SOUT1-SOUT5)	I _{OL} = 4.2 mA			0.4			0.4	v
4	Input current (leakage)	$V_1 = 0 V$ to 5.8 V, $V_{DD} = 5 V$, All other pins = 0 V			± 10			±10	μA
10	Output current (leakage) (DQ1-DQ5, SOUT1-SOUT5)	$V_{O} = 0.4 V \text{ to } 5.5 V,$ $V_{DD} = 5 V$			±10			± 10	μA
IDD 1	Average operating current during read or write cycle	t _{c(rd)} = minimum cycle time, TR/QE low after RAS falls, [‡] SCLK and SIN low, SOE high, No load on DQ1-DQ5 and SOUT1-SOUT5		250	350		250	350	mA
IDD2 [§]	Standby current	After 1 RAS cycle, RAS and CAS high, SCLK and SIN low, SOE high, No load on DQ1-DQ5 and SOUT1-SOUT5		80	100		80	100	m#
IDD3	Average refresh current	= minimum cycle time, 		210	275		185	250	mA
IDD4	Average page-mode current	t _{c(P)} = minimum cycle time, RAS low, CAS cycling, TR/QE low after RAS falls, SCLK and SIN low, SOE high, No load on DQ1-DQ5 and SOUT1-SOUT5		225	275		200	250	mA
IDD5	Average shift register current (includes IDD2)	RAS and CAS high, t _{c(SCLK)} = t _c (SCLK) min, No load on DQ1-DQ5 and SOUT1-SOUT5		150	200		150	200	mA
IDD6	Worst case average DRAM and shift register current	t _{c(rd)} = minimum cycle time, · · · · · · = minimum cycle time, · · · · · ow after RAS falls, No load on DQ1-DQ5 and SOUT1-SOUT5		425	475		400	450	mA

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

 $^{\dagger}All$ typical values are at T_A = 25°C and nominal supply voltages. *See appropriate timing diagram. $^{\$}V_{IL}$ > -0.6 V



capacitance over recommended supply voltage and operating free-air temperature range, f = 1 MHz

	PARAMETER	MAX	UNI
Ci(A)	Input capacitance, address inputs	35	
	Input capacitance, data inputs	25	[
Ci(RC)	Input capacitance, strobe inputs	50	
Ci(W)	Input capacitance, write enable input	50	pF
CI(CK)	Input capacitance, serial clock	50	pr
Ci(SI)	Input capacitance, serial in	25	
Ci(SOE)	Input capacitance, serial output enable	30	
Ci(TR)	Input capacitance, register transfer input	35	
Co(SOUT)	Output capacitance, serial out	35	

[†]All typical values are at T_A = 25 °C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1)

1		TTOT CONDITIONOT	ALT.	TM4161EP5-15	TM4161EP5-20	
P/	ARAMETER	TEST CONDITIONS [†]	SYMBOL	MIN MAX	MIN MAX	UNI
ta(C)	Access time from CAS	C _L = 100 pF	^t CAC	100	135	
^t a(QE)	Access time of Q from TR/QE low	C _L = 100 pF		40	50	
t _{a(R)}	Access time from RAS	$t_{RLCL} = MAX,$ $C_L = 100 pF$	tRAC	150	200	
t _{a(RSO)}	SOUT access time from RAS high	C _L = 30 pF		65	85	
^t a(SOE)	Access time from SOE low to SOUT	C _L = 30 pF		30	30	ns
ta(SO)	Access time from SCLK	$C_L = 30 \text{ pF}$		45	50	
^t dis(CH) [‡]	Ω output disable time from CAS high	C _L = 100 pF	tOFF	40	40	
^t dis(QE) [‡]	Q output disable time from TR/QE high	$C_L = 100 \text{ pF}$		40	40	
^t dis(SOE) [‡]	Serial output disable time from SOE high	C _L = 30 pF		30	30	

[†]Figure 1 shows the load circuit.

*The maximum values for tdis(CH), tdis(QE), and tdis(SOE) define the time at which the output achieves the open circuit condition and are not referenced to VOH or VOL.



		ALT.	TM416	1EP5-15	TM416	1EP5-20	UNF
		SYMBOL	MIN	MAX	MIN	MAX	UNI
c(P)	Page-mode cycle time	tPC	160		225		ns
c(rd)	Read cycle time [†]	^t RC	240		315		ns
c(W)	Write cycle time	twc	240		315		ns
tc(TW)	Transfer write cycle time [‡]		240		315		ns
tc(Trd)	Transfer read cycle time		240		315		ns
tc(SCLK)	Serial-clock cycle time	tscc	45	50,000	50	50,000	ns
tw(CH)	Pulse duration, CAS high (precharge time) [§]	t _{CP}	50		80		ns
tw(CL)	Pulse duration, CAS low	tCAS	100	10,000	135	10,000	ns
tw(RH)	Pulse duration, PAS high (precharge time)	tRP	80		105		กร
tw(RL)	Pulse duration, low	tRAS	150	10,000	200	10,000	ns
tw(W)	Write pulse duration	twp	45		45		ns
tw(CKL)	Pulse duration, SCLK low		10	-,	10		ns
tw(CKH)	Pulse duration, SCLK high		12		12		ns
tw(QE)	TR/QE pulse duration low time (read cycle)		40		40		ns
t _t	Transition times (rise and fall) RAS, CAS, and SCLK	тт	3	50	3	50	ns
t _{su} (CA)	Column-address setup time	tASC	0		0		ns
t _{su(RA)}	Row-address setup time	tASR	0		0		ns
t _{su} (RW)	W setup time before RAS low with TR/QE low		0		o		ns
t _{su(D)}	Data setup time	tDS	0		0		ns
tsu(rd)	Read-command setup time	tRCS	0		0		ns
t _{su} (WCL)	Early write-command setup time before CAS low	twcs	- 5		- 5		ns
t _{su} (WCH)	Write-command setup time before CAS high	tCWL	40		60		ns
t _{su} (WRH)	Write-command setup time befora RAS high	tRWL	40		60		ns
^t su(TR)	TR/QE setup time before RAS low		0		0		ns
t _{su} (SI)	Serial-data setup time before SCLK high		6		6		ns
th(SI)	Serial-data-in hold tima after SCLK high		3		3		ns
th(CLCA)	Column-address hold time after CAS low	^t CAH	45		55		ns
th(RA)	Row-address hold time	tRAH	20		25		ns
th(RW)	W hold time after RAS low with TR/QE low		20		20		ns
th(RLCA)	Column-address hold time after RAS low	tAR	95		120		ns
^t h(CLD)	Data hold time after CAS low	tDH	60	_	80		ns
th(RLD)	Data hold time after RAS low	¹ DHR	110		145		ns
th(WLD)	Data hold time after W low		45		55		ns
th(CHrd)	Read-command hold time after CAS high		0		0		ns

(Continued next page.)

NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, VIL max and VIH min must be met at the 10% and 90% points.

[†]All cycle times assume $t_t = 5$ ns axcept $t_c(SCLK)$ which assumes $t_t = 3$ ns. [‡]Multiple transfer write cycles require separation by either a 500-ns RAS-precharge interval or any other active RAS-cycle. §Page-mode onlγ.



		ALT.	TM416	1EP5-15	TM416	1EP5-20	
	Contractor and the contractor of the	SYMBOL	MIN	MAX	MIN	MAX	UNIT
th(RHrd)	Read-command hold time after RAS high	^t RRH	5		5		ns
th(CLW)	Write-command hold time after CAS low	tWCH	60		80		ns
th(RLW)	Write-command hold time after RAS low	tWCR	110		145		ns
th(RSO)	Serial-data-out hold time after RAS low with TR/QE low		30	11	30		ns
th(SO)	Serial-data-out hold time after SCLK high		8		8		ns
th(TR)	TR/QE hold time after RAS low (transfer)		20		20		ns
TRLCH	Delay time, RAS low to CAS high	tCSH	150	1	200		ns
tCHRL	Delay time, CAS high to RAS low	tCRP	0		0		ns
^tCLQEH	Delay time, CAS low to OF high		100		135		ns
tCLRH	Delay time, CAS low to high	trsh	100		135		ns
†CQE	Delay time, CAS low to us low (maximum value specified only to guarantee tergs) access time)			60		85	ns
TRHSC	Delay time, nigh to SCIK high		80	50,000	80	50,000	ns
^t RLCL	Delay time, RAS low to : low (maximum value specified only to guarantee access time)	^t RCD	25	50	30	65	ns
^t CKRL	Delay time, SCLK high before RAS low with TR/QE low¶		10	50,000	10	50,000	ns
trf(MA)	Refresh time interval, memory array	tREF1	-	4		4	ms
trf(SR)	Refresh time interval, shift register#	tREF2	1	50,000		50,000	ns

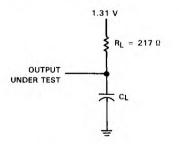
timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, VIL max and VIH min must be met at the 10% and 90% points.

SCLK may be high or low during $t_{W(RL)}$, but there can not be any positive edge transitions on SCLK for a minimum of 10 ns prior to RAS going low with TR/QE low (i.e., before a transfer cycle).

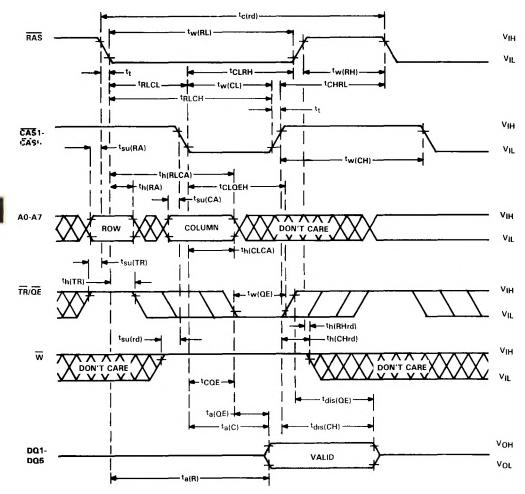
#See "refresh" on page 5-9.

PARAMETER MEASUREMENT INFORMATION





read cycle timing



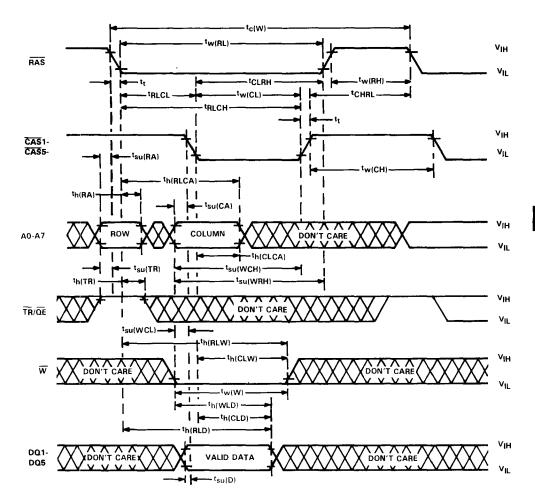


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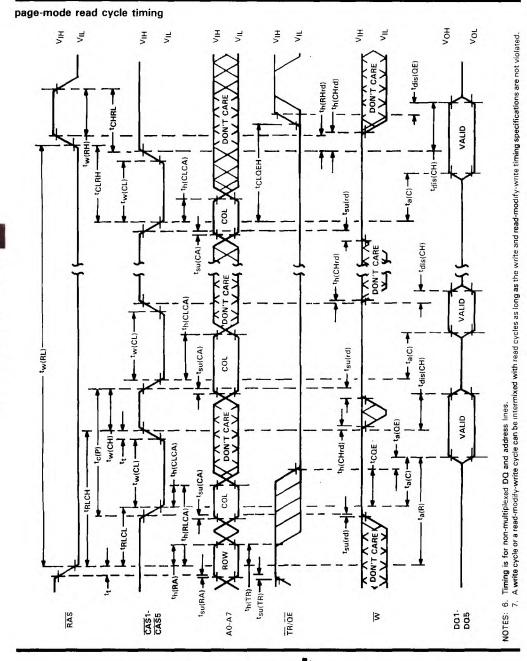
Dynamic RAM Modules

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early write cycle timing





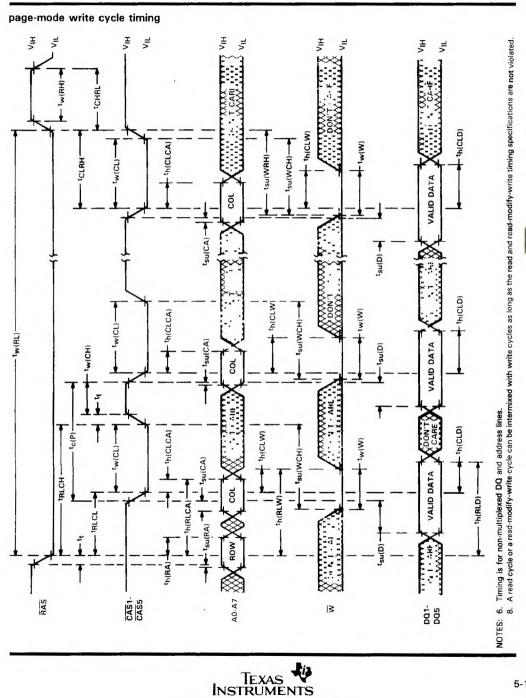


TEXAS V INSTRUMENTS

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Dynamic RAM Modules



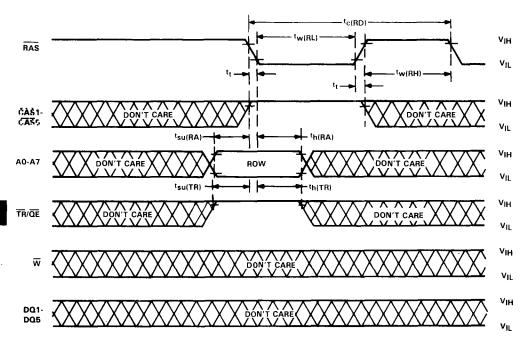
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Dynamic RAM Modules

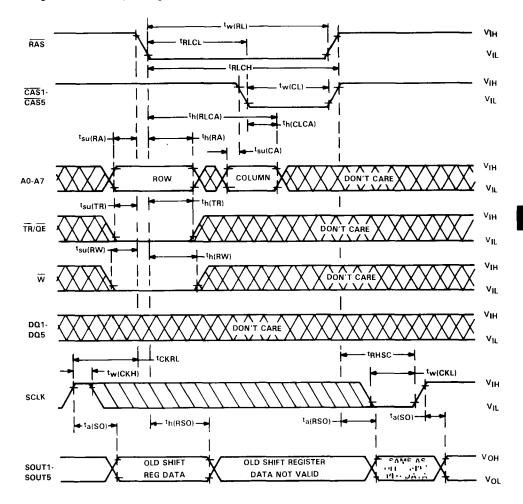
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RAS-only refresh timing





shift register to memory timing

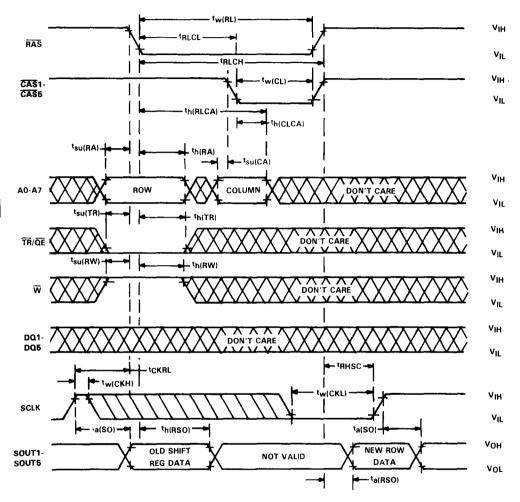


- NOTES: 9. The shift register to memory cycle is used to transfer data from the shift registers to the memory array. Every one of the 256 locations in each shift register is written into the 256 columns of the selected row. Note that the data that was in the shift registers may have resulted, either from a serial shift in or from a parallel load of the shift registers from one of the ory array rows. 10
 - assumed low
 - SCLK may be high or low during tw(RL)-11



Б

memory to shift register timing



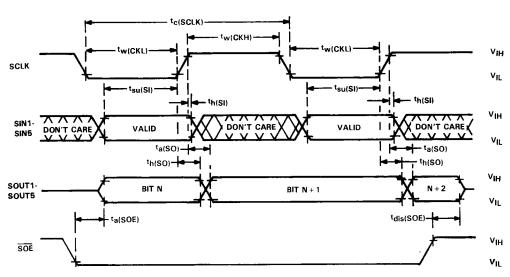
NOTES: 10. SOE assumed low.

11. SCLK may be high or low during tw(RL).

12. The memory to shift register cycle is used to load the shift registers in parallel from the memory array. Every one of the 256 locations in each shift register are written into from the 256 columns of the selected row. Note that the data that is loaded into the shift registers may be either shifted out or written back into another row.

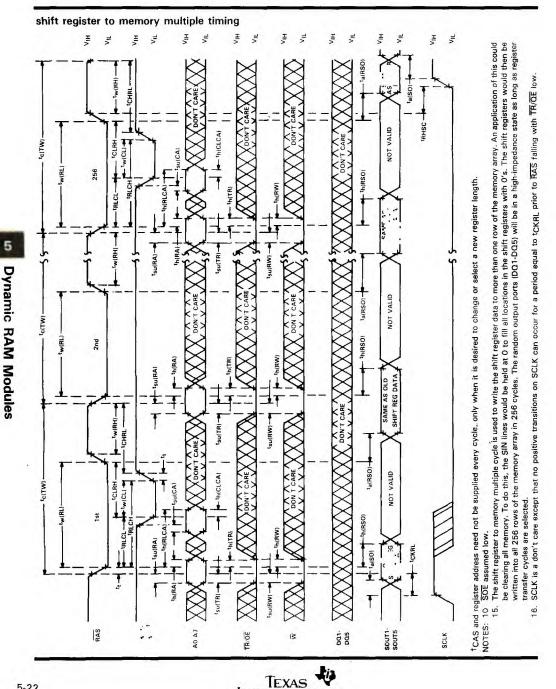


serial data shift timing



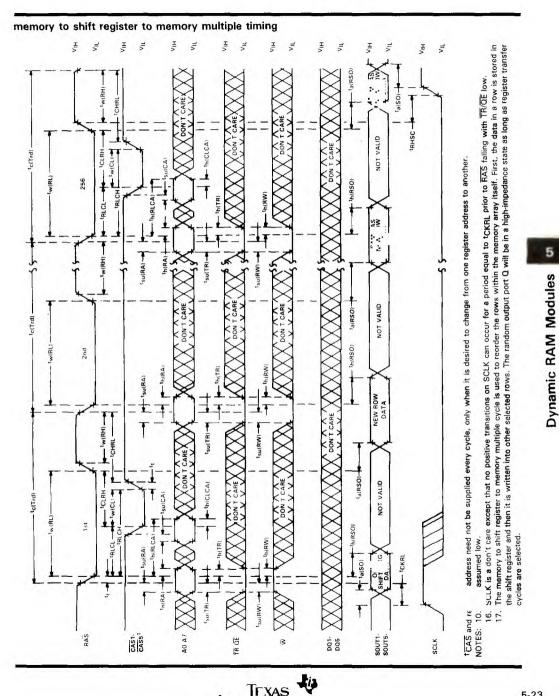
- NOTES: 13. When loading data into the shift registers from the serial input in preparation for a shift register to memory transfer operation, the serial clock must be clocked an even number of times.
 - 14. While shifting data through the serial shift registers, the state of TR/QE is a don't care as long as TR/QE is held high when RAS goes low and t_{su(TR)} and t_{h(TR)} timings are observed. This requirement avoids the initiation of a register-to-memory or memory-to-register data transfer operation. The serial data transfer cycle is used to shift data in and/or out of the shift registers.





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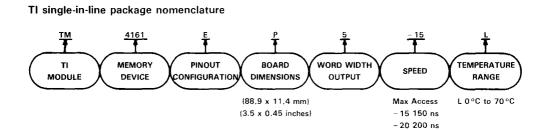
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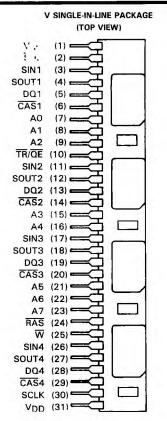


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- 65,536 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- 31-Pin Single-in-Line Package (SIP)
- Utilizes Four Multiport Video RAMs in Plastic Chip Carriers
- Serial In/Serial Out Capability
- Dual Accessibility One Port Sequential Access, One Port Random Access
- Four Serial Shift Registers for Sequential Access Applications, Each Comprised of Four Cascaded 64-Bit Segments
- Designed for both Video and Non-Video Applications
- Fast Serial Port . . . Can Be Configured for Video Data Rates in Excess of 150 MHz
- TR/QE as Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design
- Separate Serial In and Serial Out to Allow Simultaneous Shift In and Out
- Supported by TI's TMS34061 Video System Controller (VSC)
- SOE Simplifies Multiplexing of Serial Data Streams
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

	ACCESS	ACCESS	READ
	TIME	TIME	OR
	ROW	COLUMN	WRITE
	ADDRESS	ADDRESS	CYCLE
	(MAX)	(MAX)	(MIN)
TM4161EV4-15	150 ns	100 ns	240 ns
TM4161EV4-20	200 ns	135 ns	315 ns

- Separate CAS Control with Common Data-In and Data-Out Lines
- Low Power Dissipation:
 Operating . . . 1000 mW (Typ)
 Standby . . . 320 mW (Typ)
- Operating Free-Air Temperature . . . 0 °C to 70 °C



1	Pil	PIN NOMENCLATURE					
	A0-A7	Address Inputs					
	CAS1-CAS4	Column-Address Strobes					
	DQ1-DQ4	Random-Access Data In/Data Out					
	RAS	Row-Address Strobe					
	SCLK	Serial Data Clock					
	SIN1-SIN4	Serial Data In					
	SOE	Serial Output Enable					
	SOUT1-SOUT4	Serial Data Out					
	TR/QE	Register Transfer/Q Output Enable					
Ĩ	VDD	5-V Supply					
	VSS	Ground					
	$\overline{\mathbf{w}}$	Write Enable					

PRODUCTION DATA documents contain information current as of publication data. Products conform to specifications per the terms of Texas Instruments standard warrenty. Production processing does not necessarily include testing of all parameters.



description

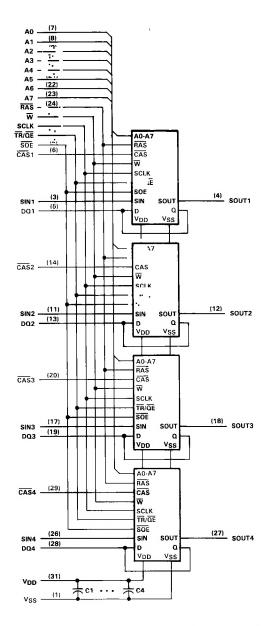
The TM4161EV4 is a 256K dual-access dynamic random-access memory module organized as 65,536 \times 4-bits in a 31-pin single-in-line package comprising four TMS4161FML, 65,536 \times 1-bit Multiport Video RAMs in 22-lead plastic chip carriers mounted on top of a substrate together with four decoupling capacitors. The random-access port makes the memory look like it is organized as 65,536 words of four bits each. The sequential access port is interfaced to four internal 256-bit dynamic shift registers each organized as four cascaded 64-bit shift register segments which are accessed serially. One, two, three, or four 64-bit shift register segments can be sequentially read out after a transfer cycle depending on a two-bit code applied to the two most significant column address inputs.

The TM4161EV4 features full asynchronous dual access capability except when transferring data between the shift registers and the memory array.

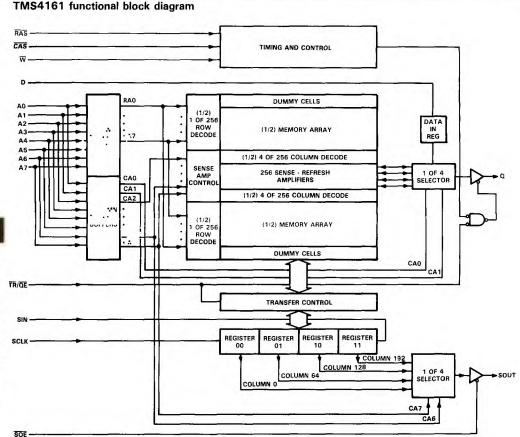
All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4161EV4 is guaranteed for operation from 0°C to 70°C.

functional block diagram







random-access address space to sequential-address space mapping



Dynamic RAM Modules

random-access operation

TR/QE

The TR/QE pin has two functions. First, it selects either register transfer or random-access operation as RAS falls, and second, during a random-access operation, it functions as an output enable after CAS falls.

To use the TM4161EV4 in the random-access mode, $\overline{TR}/\overline{QE}$ must be high as \overline{RAS} falls. Holding $\overline{TR}/\overline{QE}$ high as \overline{RAS} falls keeps the 256 elements of the shift registers disconnected from the corresponding 256 bit lines of the maximum ry array. If data is to be shifted, the shift registers must be disconnected from the bit lines. Holding $\frac{15}{2E}$ low as \overline{RAS} falls enables the 256 switches that connect the shift registers to the bit lines and indicates that a transfer will occur between the shift registers and one of the memory rows.

During random-access operation, once \overline{CAS} has been :...: low, $\overline{TR}/\overline{QE}$ controls when the data will appear at the Q output (if this a read cycle). Whenever \overline{TI} :: is held high during random-access operation, the Q output will be in the high-impedance state. This feature removes the possibility of an overlap between data on the address lines and data appearing on the Q output making it possible to connect the address lines to the Q and D lines (Use of this organization prohibits the use of the early write cycle.).

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe (\overline{RAS}). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe (\overline{CAS}). All addresses must be stable on or before the falling edges of \overline{RAS} and \overline{CAS} . \overline{RAS} is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. \overline{CAS} is used as a chip select activating the column decoder and the input and output buffers.

write enable (W)

The read or write mode is selected through the write-enable (\overline{W}) input. A logic high on the \overline{W} input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM4161EV4 dictates the use of early write cycles to prevent contention on DQ. When \overline{W} goes low prior to \overline{CAS} , the data outputs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ4)

Data is written during a write or read-modify-write cycle. The falling edge of \overline{CAS} or \overline{W} strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, \overline{W} is brought low prior to \overline{CAS} and the data is strobed in by \overline{CAS} with setup and hold times referenced to this signal.

data out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state as long as \overline{CAS} or $\overline{TR}/\overline{QE}$ is held high. Data will not appear on the output until after both \overline{CAS} and $\overline{TR}/\overline{QE}$ have been brought low. In a read cycle, the guaranteed maximum output enable access time is valid only if tCQE is greater than tCQE MAX, and tRLCL is greater than tRLCL MAX. Likewise, ta(C) MAX is valid only if tRLCL is greater than '19 CL MAX. Once the output is valid, it will remain valid while \overline{CAS} and $\overline{TR}/\overline{QE}$ are both low; \overline{CAS} or \overline{TR} '19 CL MAX. Once the output to a high-impedance state. In an early write cycle, the output is always in a high-impedance state. In a register transfer cycle, the output will always be in a high-impedance state.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in high-impedance state unless CAS is applied, the RAS-only refresh sequence avoids any output



during refresh. Strobing each of the 256 row addresses (A0 through A7) with \overline{RAS} causes all bits in each row to be refreshed. \overline{CAS} can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on M1-M4, the row address and RAS are applied to multiple modules. CAS is then decoded to select the proper module.

power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, RAS must remain high for 100 μ s immediately prior to initialization. Initialization consists of performing eight RAS cycles before proper device operation is achieved.

sequential-access operation

TR/QE

Memory transfer operations involving parallel use of the shift registers are first indicated by bringing TR/QE low before \overline{RAS} falls low. This enables the switches connecting the 256 elements of the shift registers to the 256 bit lines of the memory array. The \overline{W} line determines whether the data will be transferred from or to the shift registers.

write enable (W)

In the sequential-access mode, \overline{W} determines whether a transfer will occur from the shift registers to the memory array, or from the memory array to the shift registers. To transfer from the shift registers to the memory array, \overline{W} is held low as \overline{RAS} falls, and, to transfer from the memory array to the shift registers, \overline{W} is held high as \overline{RAS} falls. Thus, reads and writes are always with respect to the memory array. The write setup and hold times are referenced to the falling edge of \overline{RAS} for this mode of operation.

row address (A0 through A7)

Eight address bits are required to select one of the 256 possible rows involved in the transfer of data to or from the shift registers. A0-A7, \overline{W} , and $\overline{TR}/\overline{QE}$ are latched on the falling edge of \overline{RAS} .

register column address (A7, A6)

To select one of the four shift register segments within each shift register (transfer from memory to register only), the appropriate 2-bit column address (A7, A6) must be valid when \overline{CAS} falls. However, the \overline{CAS} and segment address signals need not be supplied every transfer cycle, only when it is desired to change or select a new segment.

SCLK

Data is shifted in and out on the rising edge of SCLK. This makes it possible to view each shift register as though it were made of 256 rising edge D flip-flops connected D to Q. The TM4161EV4 is designed to work with a wide range duty cycle clock to simplify system design. Note that data will appear at the SOUT pins not only on the rising edge of SCLK but also after an access time of $t_{a}(RSO)$ from RAS high during a parallel load of the shift registers.

SIN and SOUT

Data is shifted in through the SIN pins and is shifted out through the SOUT pins. The TM4161EV4 is designed such that it requires 3 ns hold time on SIN as SCLK rises. SOUT is guaranteed not to change for at least 8 ns after SCLK rises. When loading data into the shift registers from the serial inputs in preparation for a shift register to memory transfer operation, the serial clock must be clocked an even number of times. To guarantee proper serial clock sequence after power up, a transfer cycle must be initiated before a serial data stream is applied at SIN.



SOE

The serial output enable pin controls the impedance of the serial outputs, allowing in the serial outputs allowing in the series into the same external video circuitry. When the series is at a logic low level, the SOUTs will be enabled and the proper data read out. When SOE is at a logic high level, the SOUTs will be disabled and be in the high-impedance state.

refresh

The shift registers are also dynamic storage elements. The data held in the registers will be lost unless SCLK goes high to shift the data one bit position, a transfer write operation is invoked, or the data is reloaded from the memory array. See specifications for maximum register data retention times. Important: If the shift registers have remained idle for a time period which exceeds the maximum SCLK high or SCLK low time, the dynamic clock circuits will lose charge. Under these conditions, the shift register clocks must be re-enabled by performing any transfer cycle before data can be shifted into or out of the shift registers.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness Bypass capacitors: Multilayer ceramic Leads: Tin/lead solder coated over phosphor-bronze

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Voltage range on any pin except VDD and data out (see Note 1)	- 1.5 V to 10 V
Voltage range on VDD supply and data out with respect to VSS	1 V to 6 V
Short circuit output current	50 mA
Power dissipation	4 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	65°C to 150°C

[†]Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to VSS.

recommended operating conditions

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	4.5	5	5.5	V
Vss	Supply voltage		0		۷
VIH	High-level input voltage	2.4		DD+0.3	٧
VIL	Low-level input voltage (see Notes 2 and 3)	-0.6		0.8	V
TA	Operating free-air temperature	0		70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

Due to input protection circuitry, the applied voltage may begin to clamp at -0.6 V; test conditions must comprehend this occurrence.

4. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.



	PARAMETER	TEST CONDITIONS	TM4161EV4-15			TM4161EV4-20			UNIT
	PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	MIN	TYPT	MAX	UNI
Vон	High-level output voltage (DQ1-DQ4, SOUT1-SOUT4)	l _{OH} = -5 mA	2.4			2.4			v
VOL	Low-level output voltage (DQ1-DQ4, SOUT1-SOUT4)	I _{OL} = 4.2 mA			0.4			0.4	v
ų	Input current (leakage)	$V_I = 0 V \text{ to } 5.8 V,$ $V_{DD} = 5 V,$ All other pins = 0 V			±10			± 10	μΑ
0	Output current (leakage) (DQ1-DQ4, SOUT1-SOUT4)	$V_{O} = 0.4 V \text{ to } 5.5 V,$ $V_{DD} = 5 V$			±10			±10	μA
וסס ^ן	Average operating current during read or write cycle	t _{c(rd)} = minimum cycle time, TR/ΩE low after RAS falls, [‡] SCLK and SIN low, SOE high, No load on DQ1-DQ4 and SOUT1-SOUT4		200	280		200	280	mA
IDD2 [§]	Standby current	After 1 RAS cycle, RAS and CAS high, SCLK and SIN low, SOE high, No load on DQ1-DQ4 and SOUT1-SOUT4		64	80		64	80	mA
IDD3	Average refresh current	t _{c(rd)} = minimum cycle time, CAS high, RAS cycling, SCLK and SIN low, SOE high, TR/QE high, No load on DQ1-DQ4 and SOUT1-SOUT4		168	220		148	220	mA
IDD4	Average page-mode current	t _{c(P)} = minimum cycle time, RAS low, CAS cycling, TR/QE low after RAS falls, SCLK and SIN low, SOE high, No load on DQ1-DQ4 and SOUT1-SOUT4		180	220		160	220	mA
IDD5	Average shift register current (includes IDD2)	\overline{RAS} and \overline{CAS} high, $t_{c(SCLK)} = t_{c(SCLK)}$ min, No load on DQ1-DQ4 and SOUT1-SOUT4		120	160		120	160	mA
IDD6	Worst case average DRAM and shift register current	$\label{eq:tc(rd)} = \mbox{minimum cycle time,} \\ t_{c(SCLK)} = \mbox{minimum cycle time,} \\ \hline TR/\overline{\Omega E} \mbox{ low after RAS falls,} \\ No \mbox{ load on } DQ1-DQ4 \\ \mbox{and } SOUT1-SOUT4 \\ \end{tabular}$		340	380		320	360	mA

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

 $^{\dagger}All$ typical values are at $T_A=25\,^oC$ and nominal supply voltages. *See appropriate timing diagram. §V_{JL}>~-0.6 V



capacitance over recommended supply voltage and operating free-air temperature range, $f\,=\,1\,\,\text{MHz}$

	PARAMETER	MAX	UNIT
Ci(A)	Input capacitance, address inputs	35	
Ci(DQ)	Input capacitance, data inputs	20	
Ci(RC)	Input capacitance, strobe inputs	40	
Ci(W)	Input capacitance, write enable input	40	pF
Ci(CK)	Input capacitance, serial clock	30	pr
Ci(SI)	Input capacitance, serial in	20	
Ci(SOE)	Input capacitance, serial output enable	30	
Ci(TR)	Input capacitance, register transfer input	30	
Co(SOUT)	Output capacitance, serial out	20	

[†]All typical values are at $T_A = 25 \,^{\circ}C$ and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1)

PARAMETER		TEST CONDITIONS	ALT.	TM4161EV4-15	TM4161EV4-20	UNIT
		TEST CONDITIONS	SYMBOL	MIN MAA	MIN MAX	
ta(C)	Access time from CAS	C _L = 100 pF	tCAC	100	135	
^t a(QE)	Access time of Q from TR/QE low	$C_L = 100 \text{ pF}$		40	50	
t _{a(R)}	Access time from RAS	$t_{RLCL} = MAX,$ $C_L = 100 pF$	^t RAC	150	200	
ta(RSO)	SOUT access time from RAS high	$C_L = 30 pF$		65	85	
ta(SOE)	Access time from SOE low to SOUT	C _L = 30 pF		30	30	ns
ta(SO)	Access time from SCLK	CL = 30 pF		45	50	
^t dis(CH) [‡]	Q output disable time from CAS high	C _L = 100 pF	tOFF	40	40	
t _{dis(QE)} ‡	Q output disable time from TR/QE high	$C_L = 100 \text{ pF}$		40	40	
tdis(SOE) [‡]	Serial output disable time from SOE high	$C_L = 30 \text{ pF}$		30	30	

[†]Figure 1 shows the load circuit.

⁺The maximum values for t_{dis(CH)}, t_{dis(QE)}, and t_{dis(SOE)} define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.



		ALT.	TM416	1EV4-15	TM416	EV4-20	UNIT
		SYMBOL	MIN	MAX	MIN	MAX	UNH
t _{c(P)}	Page-mode cycle time	tPC	100				ns
tc(rd)	Read cycle time [†]	tRC	240		315		ns
tc(W)	Write cycle time	twc	240		315		ns
tc(TW)	Transfer write cycle time [‡]		240		315		ns
tc(Trd)	Transfer read cycle time		240		315		ns
tc(SCLK)	Serial-clock cycle time	tscc	45	50,000	50	50,000	ПS
tw(CH)	Pulse duration, CAS high (precharge time)§	tCP	50	2.5	80		ns
tw(CL)	Pulse duration, CAS low	^t CAS	100	10,000	135	10,000	ns
tw(RH)	Pulse duration, RAS high (precharge time)	tRP	80		105		ns
tw(RL)	Pulse duration, RAS low	tRAS	150	10,000	200	10,000	ns
tw(W)	Write pulse duration	tWP	45		45		пѕ
tw(CKL)	Pulse duration, SCLK low		10	6 I.	10		ns
tw(CKH)	Pulse duration, SCLK high		12		12		ПS
tw(QE)	TR/QE pulse duration low time (read cycle)		40		40		ns
tt	Transition times (rise and fall) RAS, CAS, and SCLK	۲Ť	3	50	3	50	ns
tsu(CA)	Column-address setup time	tASC	0		0	1990	ns
tsu(RA)	Row-address setup time	tASR	0		0		ns
^t su(RW)	W setup time before RAS low with TR/QE low		0		0		ns
t _{su(D)}	Data setup time	tDS	0	01.0	0	-2 - 22	ns
tsu(rd)	Read-command setup time	tRCS	0		0	5 i i i	ns
t _{su} (WCL)	Early write-command setup time before CAS low	twcs	- 5		- 5		ns
t _{su} (WCH)	Write-command setup time before CAS high	tCWL	40		60		ns
t _{su} (WRH)	Write-command setup time before RAS high	tRWL	40		60		ns
tsu(TR)	TR/QE setup time before RAS low		0		0		ns
tsu(SI)	Serial-data setup time before SCLK high	1	6	· · · · · · · · ·	6	-	ns
th(SI)	Serial-data-in hold time after SCLK high		3		3		ns
th(CLCA)	Column-address hold time after CAS low	^t CAH	. 45		55		ns
th(RA)	Row-address hold time	tRAH	20		25		ns
th(RW)	W hold time after RAS low with TR/QE low		20		20		ns
th(RLCA)	Column-address hold time after RAS low	tAR	95		120		ns
th(CLD)	Data hold time after CAS low	tDH	60		80		ns
th(RLD)	Data hold time after RAS low	tDHR	110		145		ns
th(WLD)	Data hold time after ₩ low	tDH	45		55		ns
th(CHrd)	Read-command hold time after CAS high	tRCH	0		0		ns

timing requirements over recommended supply voltage range and operating free-air temperature range

(Continued next page.)

NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, VIL max and VIH min must be met at the 10% and 90% points.

[†]All cycle times assume $t_t = 5$ ns except $t_{c(SCLK)}$ which assumes $t_t = 3$ ns. [‡]Multiple transfer write cycles require separation by either a 500 ns RAS-precharge interval or any other active RAS-cycle. SPage-mode only.



		ALT.	TM4161EV4-15		TM4161EV4-20		
		SYMBOL	MIN	MAX	MIN	MAX	UNIT
th(RHrd)	Read-command hold time after RAS high	^t RRH	5		5		ns
th(CLW)	Write-command hold time after CAS low	tWCH	60		80		ns
th(RLW)	Write-command hold time after RAS low	tWCR	110		145		ns
t _h (RSO)	Serial-data-out hold time after RAS low with TR/QE low		30		30		ns
th(SO)	Interout hold time after SCLK high		8		8		ns
th(TR)	. nold time after RAS low (transfer)		20		20		ns
TRLCH	Delay time, RAS low to CAS high	tCSH	150		200		ns
tCHRL	Delay time, CAS high to RAS low	tCRP	0		0		ΠS
^t CLQEH	Delay time, CAS low to OF high		100		135		ns
^t CLRH	Delay time, CAS low to migh	tRSH	100		135		ns
^t CQE	Delay time, CAS low to ue low (maximum value specified only to guarantee t _{a(QE)} access time)			60		85	ns
TRHSC	Delay time, RAS high to SCLK high		80	50,000	80	50,000	ns
TRLCL	Delay time, RAS low to CAS low (maximum value specified only to guarantee access time)	tRCD	25	50	30	65	ns
^t CKRL	Delay time, SCLK high before RAS low with TR/QE low¶		10	50,000	10	50,000	ns
trf(MA)	Refresh time interval, memory array	tREF1		4		4	ms
trf(SR)	Refresh time interval, shift register#	tREF2		50,000		50,000	ns

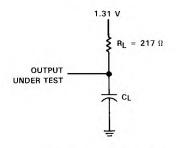
timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

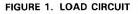
NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, VIL max and VIH min must be met at the 10% and 90% points.

SCLK may be high or low during $t_{W(RL)}$, but there can not be any positive edge transitions on SCLK for a minimum of 10 ns prior to RAS going low with TR/QE low (i.e., before a transfer cycle).

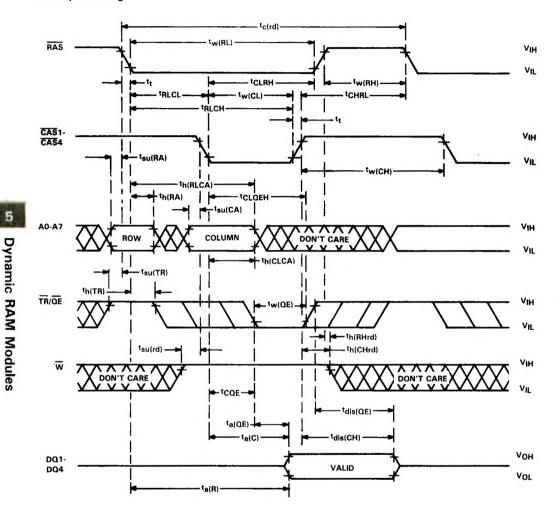
#See "refresh" on page 5-31.

PARAMETER MEASUREMENT INFORMATION

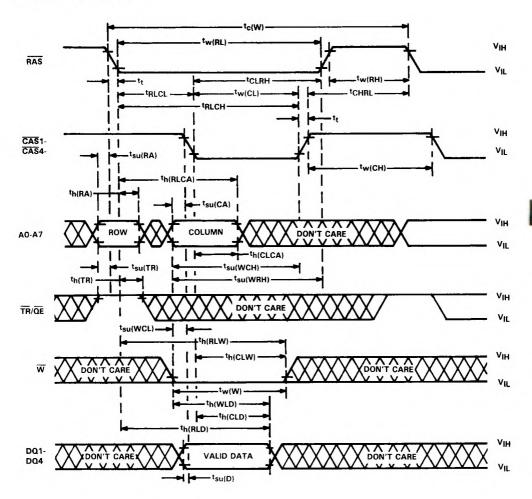




read cycle timing

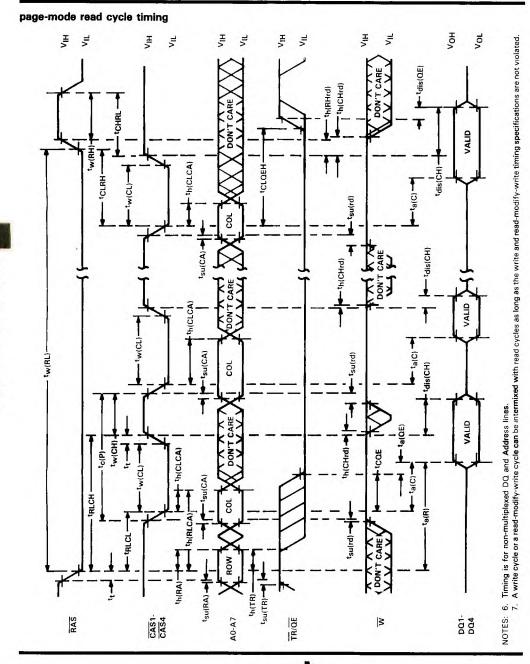


early write cycle timing





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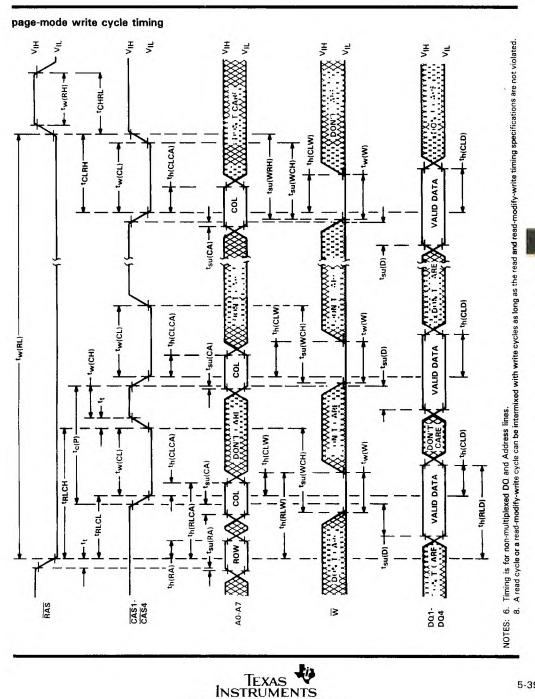


TEXAS V INSTRUMENTS

5-38

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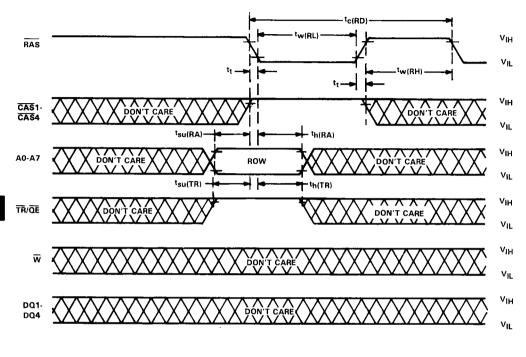


POST OFFICE BOX 1443 . HOUSTON TEXAS 77001

5-39

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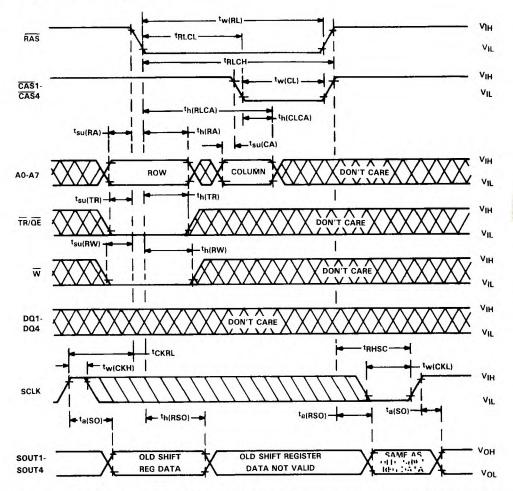
RAS-only refresh timing





Dynamic RAM Modules

shift register to memory timing



NOTES: 9. The shift register to memory cycle is used to transfer data from the shift registers to the memory array. Every one of the 256 locations in each shift register is written into the 256 columns of the selected row. Note that the data that was in the shift registers may have resulted, either from a serial shift in or from a parallel load of the shift registers from one of the 1 m my array rows.

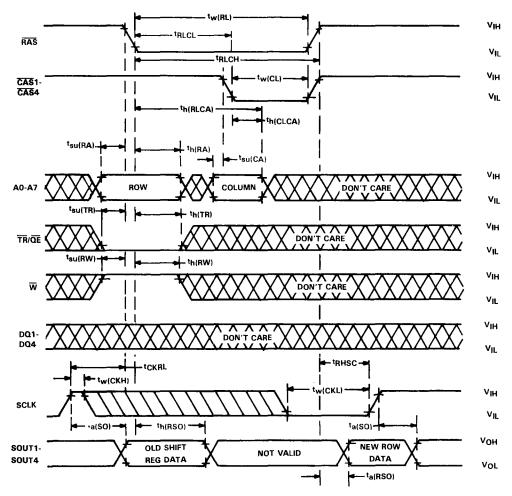
10. 'ssumed low.

11. SULK may be high or low during tw(RL).



5

memory to shift register timing



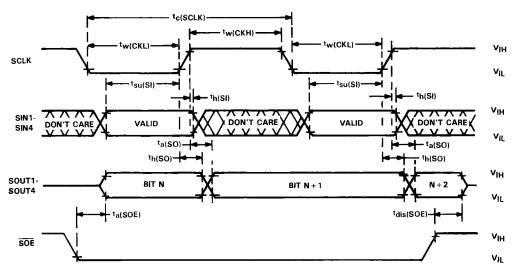
NOTES: 10. SOE assumed low.

12. The memory to shift register cycle is used to load the shift registers in parallel from the memory array. Every one of the 256 locations in each shift register are written into from the 256 columns of the selected row. Note that the data that is loaded into the shift registers may be either shifted out or written back into another row.



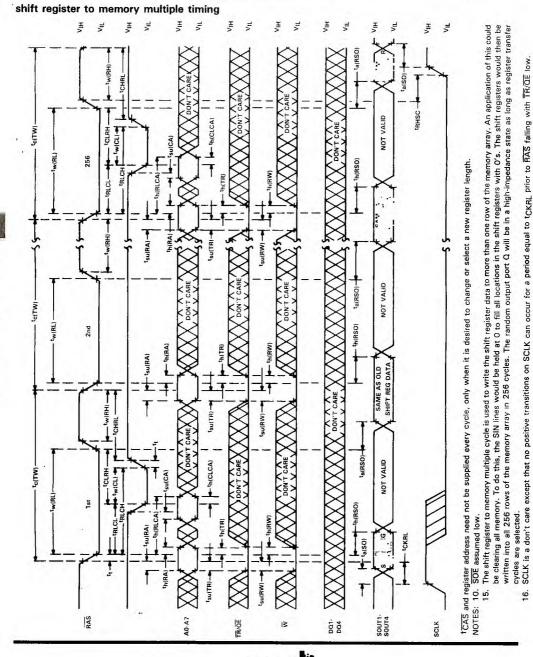
^{11.} SCLK may be high or low during tw(RL).

serial data shift timing



- NOTES: 13. When loading data into the shift registers from the serial input in preparation for a shift register to memory transfer operation, the serial clock must be clocked an even number of times.
 - 14. While shifting data through the serial registers, the state of TR/QE is a don't care as long as TR/QE is held high when RAS goes low and t_{su(TR)} and t_{h(TR)} timings are observed. This requirement avoids the initiation of a register-to-memory or memory-to-register data transfer operation. The serial data transfer cycle is used to shift data in and/or out of the shift registers.



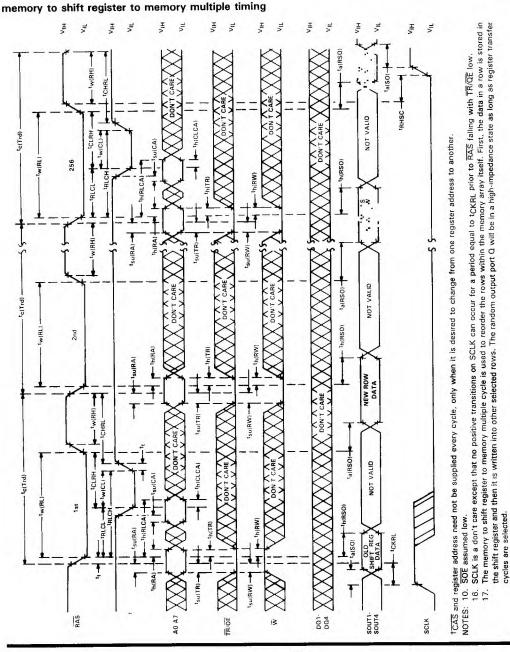


TEXA

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5-44

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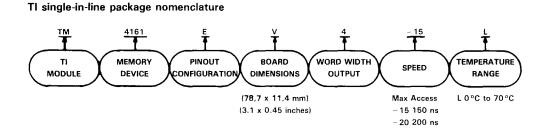


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Τr

Dynamic RAM Modules





ADVANCE INFORMATION

TM4161GW4, TM4161GY4 65,536 BY 4-BIT DYNAMIC RAM MODULES

TM4161GW4 . . . W SINGLE-IN-LINE PACKAGE[†] TM4161GY4 . . . Y SINGLE-IN-LINE PACKAGE[†]

NOVEMBER 1985

- 65,536 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
 - -Pinned Version for Through-Hole Insertion (TM4161GY4)
 - -Leadless Version for Use with Sockets (TM4161GW4)
- Utilizes Four Multiport Video RAMs in **Plastic Chip Carriers**
- Long Refresh Period . . . 4 ms (256 Cycles)
- . All Inputs, Outputs, Clocks Fully TTL Compatible
- **3-State Outputs**
- Performance of Unmounted RAMs:

	ACCESS	ACCESS	READ	READ-
	ROW	COLUMN	WRITE	WRITE
	ADDRESS	ADDRESS	CYCLE	CYCLE
	(MAX)	(MAX)	(MIN)	(MIN)
TMS4161-15	150 ns	100 ns	240 ns	265 ns
TMS4161-20	200 ns	135 ns	315 ns	330 ns

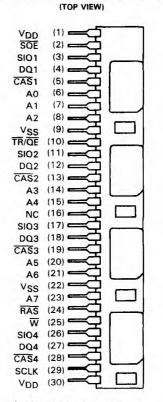
- Separate CAS Control with Common Data-In and Data-Out Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)	
TM4161G_4-15	1000 mW	256 mW	
TM4161G_4-20	1000 mW	256 mW	

Operating Free-Air Temperature . . . 0°C To 70°C

description

The TM4161G_4 series are 256K dual-access dynamic random-access memory modules organized as 65,536 × 4-bits in a 30-pin singlein-line package. This module is comprised of four TMS4161FML, 65,536 × 1-bit Multiport Video RAMs in 22-lead plastic chip carriers mounted on top of a substrate together with four decoupling capacitors. Each TMS4161FML is described in the TMS4161 data sheet and is fully electrically tested and processed according to TI's MIL-STD-883B (as amended for commercial applications) flows prior to assembly. After assembly onto the substrate, a further set of electrical tests is performed. The TM4161G_4 is rated for operation from 0°C to 70°C.



[†]TM4161GY4 package is shown.

	PIN NOMENCLATURE
A0-A7	Address Inputs
CAS1-CAS4	Column-Address Strobes
DQ1-DQ4	Random-Access Data in/Data Out
NC	No Connection
RAS	Row-Address Strobe
SCLK	Serial Data Clock
SI01-SI04	Serial-Access Data In/Data Out
SOE	Serial Output Enable
TR/QE	Register Transfer/Q Output Enable
VDD	5-V Supply
VSS	Ground
W	Write Enable

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice



TM4161GW4, TM4161GY4 65,536 BY 4-BIT DYNAMIC RAM MODULES

operation

The TM4161G_4 operates as four TMS4161's connected as shown in the functional block diagram. Refer to the TMS4161 data sheet for details of its operation.

specifications

For TMS4161 electrical specifications, refer to the TMS4161 data sheet.

single-in-line package components

PC substrate: TM4164GY4 . . . 0,79 mm (0.031 inch) minimum thickness TM4161GW4 . . . 1,35 mm (0.053 inch) maximum thickness

Bypass capacitors: Multilayer ceramic

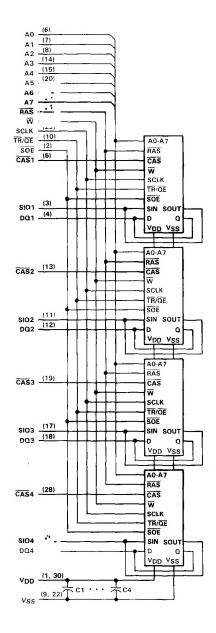
Leads: Tin/lead solder coated over phosphor-bronze

Contact area for socketable devices: Nickel plate and solder plate on top of copper



TM4161GW4, TM4161GY4 65,536 BY 4-BIT DYNAMIC RAM MODULES

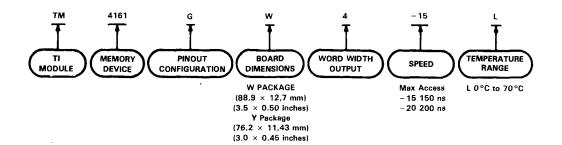
functional block diagram





TM4161GW4, TM4161GY4 65,536 BY 4-BIT DYNAMIC RAM MODULES

TI single-in-line package nomenclature





SINGLE-IN-LINE PACKAGE (TOP VIEW)

NC[†] (1) =

VDD (2)

> D1 (3)

NOVEMBER 1983 - REVISED NOVEMBER 1985

- 65,536 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- 22-Pin Single-in-Line Package (SIP)
- Utilizes Four 64K Dynamic RAMs in Plastic **Chip Carrier**
- Long Refresh Period . . . 4 ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- **3-State Outputs**
- **Performance Ranges:**

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ- MODIFY- WRITE CYCLE (MIN)
TM4164EC4-12	120 ns	75 ns	230 ns	260 ns
TM4164EC4-15	150 ns	90 ns	260 ns	285 ns
TM4164EC4-20	200 ns	135 ns	326 ns	345 ns

- Common CAS Control with Separate Data-In and Data-Out Lines with an "Early Write" Feature
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4164EC4-12	800 mW	70 mW
TM4164EC4-15	700 mW	70 mW
TM4164EC4-20	540 mW	70 mW

- Operating Free-Air Temperature . . . 0 °C to 70°C
- Upward Compatible with 256K X 4 Single-In-Line Package

Q1 (4)CAS (5) A7 (6) A5 (7) A4 (8) D2 (9) Q2 (10) W (11) A1 (12) A3 (13) A6 (14) Q3 (15) D3 (16) A2 (17) A0 (18) C RAS (19) D4 (20) 04 (21) VSS (22)

[†]Reserved for A8 on TM4256EC4

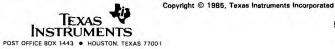
	PIN NOMENCLATURE
A0-A7	Address Inputs
CAS	Column-Address Strobe
D1-D4	Data Inputs
NC	No Connection
Q1-Q4	Data Outputs
RAS	Row-Address Strobe
VDD	5-V Supply
VSS	Ground
W	Write Enable

description

The TM4164EC4 is a 256K, dynamic random-access memory module organized as 65,536 × 4 bits in a 22-pin single-in-line package comprising four TMS4164FPL, 65,536 × 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with four 0.1 μ F decoupling capacitors. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM4164EC4 has a density of six devices per square inch (approximately 2.4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4164EC4 is rated for operation from 0°C to 70°C.



upward compatibility

Future 256K × 4 memory modules in single-in-line packages will have identical pin functions and spacing, and will be directly upward compatible. Pin 1 of the TM4256EC4 (256K X 4 SIP) module will be memory address A8.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations on each of the four chips. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe (\overline{RAS}). Then the eight column-address bits are set up on Pins A0 through A7 and latched onto the chip by the column-address strobe (\overline{CAS}). All addresses must be stable on or before the falling edges of \overline{RAS} and \overline{CAS} . \overline{RAS} is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. \overline{CAS} is used as a chip select activating the column decoder and the input and output buffers.

write enable (W)

The read or write mode is selected through the write-enable (\overline{W}) input. A logic high on the \overline{W} input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. When \overline{W} goes low prior to \overline{CAS} , the data-outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D1-D4)

Data is with during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overrightarrow{(A)}$ or \overrightarrow{W} strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, \overrightarrow{W} is brought low prior to \overrightarrow{CAS} and the data is strobed in by \overrightarrow{CAS} with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, \overrightarrow{CAS} will already be low, thus the data will be strobed in by \overrightarrow{W} with setup and hold times referenced to this signal.

data out (Q1-Q4)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state unti $C\overline{AS}$ s brought low. In a read cycle the outputs go active after the access time interval $t_{a}(C)$ that begins with the negative transition of \overline{CAS} as long as $t_{a}(R)$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while \overline{CAS} is low; \overline{CAS} going high returns them to a high-impedance state. In an early write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless CAS is applied, the RAS-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (AO through A7) with RAS causes all bits in each row to be refreshed. CAS can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single module, the row address and RAS are applied to multiple modules. CAS is then decoded to select the proper module.



power up

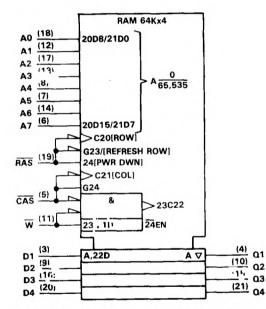
After power up, the power supply must remain at its steady-state value for 1 ms. In addition, \overline{RAS} must remain high for 100 μ s immediately prior to initialization. Initialization consists of performing eight \overline{RAS} cycles before proper device operation is achieved.

single-in-line package and components

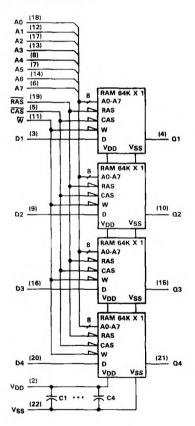
PC substrate: 0,79 mm (0.031 inch) minimum thickness Bypass capacitors: Multilayer ceramic Leads: Tin/lead solder coated over phosphor-bronze

logic symbol[†]

functional block diagram



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.





absolute maximum ratings over operating free-air temperature range (unless otherwise noted) †

Voltage range on any pin except VDD and data out (see Note 1)	-1.5 V to 10 V
Voltage range on VDD supply and data out with respect to VSS	1 V to 6 V
Short circuit output current for any output	50 mA
Power dissipation	
Operating free-air temperature range	0°C to 70°C
Storage temperature range	65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to VSS.

recommended operating conditions

1.2.5			MIN N	OM MAX	
VDD	Suptractor		4.5	Ե Ե.Ե	T • T
V _{DD} V _{SS}	E and the factor			0	V
		V _{DD} = 4.5 V	2.4	4.8	N.
∨ін	High-level input voltage	V _{DD} = 5.5 V	2.4	ს ს.ს 0	l v
VIL	Low-level input voltage (see Not	es 2 and 3)	-0.6	0.8	V
TA	Operating free-air temperature		0	70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

 Due to input protection circuitry, the applied voltage may begin to clamp at -0.6 V. Test conditions should comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

DADAMETED		PARAMETER TEST		TM4164EC4-12			TM4164EC4-15		
_	FARAMETER	CONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VOH	High-level output voltage	IOH = -5 mA	2.4		-	2.4			V
VOL	Low-level output voltage	IOL = 4.2 mA			0.4		1000	0.4	V
h.	Input current (leakage)	$V_{I}=0$ V to 5.8 V, $V_{DD}=5$ V, All other pins = 0 V			±10			±10	μA
ю	Output current (leakage)	$V_0 = 0.4$ to 5.5 V, $V_{DD} = 5$ V, \overline{CAS} high			±10			±10	μА
IDD1	Average operating current during read or write cycle	t _C = minímum cγcle, All outputs open		160	192		140	180	mA
IDD2	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open,		14	20		14	20	mA
IDD3	Average refresh current	$t_c = minimum cycle,$ CAS high and RAS cycling, All outputs open		112	160		100	148	mA
IDD4	Average page-mode current	t _{c(P)} = minimum cycle, RAS low and CAS cycling, All outputs open		112	160		100	148	mA

[†]All typical values are at $T_A = 25 \,^{\circ}$ C and nominal supply voltages.



	PARAMETER TEST CONDITIONS		TM4164EC MIN TYPT		UNIT
VOH	High-level output voltage	1 _{0H} = -5 mA	2.4		V
VOL	Low-level output voltage	IOL = 4.2 mA		0.4	V
4	Input current (leakage)	$V_{I} = 0 V$ to 5.8 V, $V_{DD} = 5 V$ All other pins = 0 V		±10	μA
ю	Output current (leakage)	VO = 0.4 to 5.5 V, VO⊡ = 5 V, IA- nigh		±10	μА
IDD1	Average operating current during read or write cycle	t _C = minimum cycle, All outputs open	108	148	mA
IDD2	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open	14	20	mA
IDD3	Average refresh current	t _c = minimum cycle, CAS high and RAS cycling, All outputs open	80	128	mA
IDD4	Average page-mode current	t _C (P) = minimum cycle, RAS low and CAS cycling, All outputs open	80	128	mA

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

[†]All typical values are at $T_A = 25 \,^{\circ}C$ and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, $f\,=\,1\,\,\text{MHz}$

	PARAMETER	MAX	UNIT
Ci(A)	Input capacitance, address inputs	20	pF
Ci(D)	Input capacitance, data input	5	pF
Ci(RC)	Input capacitance, strobe inputs	32	pF
Ci(W)	Input capacitance, write enable input	32	pF
Co	Output capacitance	6	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4184EC4-12 MIN MAX		TM4164EC4-15 MIN MAX		UNIT
t _{a(C)}	Access time from CAS	CL = 100 pF, Load = 2 Series 74 TTL gates	tCAC		75		90	ns
t _{a(R)}	Access time from RAS	tRLCL = MAX, Load = 2 Series 74 TTL gates	tRAC		120		150	ns
^t dis(CH)	Output disable time after CAS high	CL = 100 pF, Load = 2 Series 74 TTL gates	tOFF	0	40	0	40	ns



switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4164EC4-20 MIN MAX	UNIT
t _a (C)	Access time from CAS	C _L = 100 pF Load = 2 Series 74 TTL gates	tCAC	135	ns
t _{a(R)}	Access time from RAS	tRLCL = MAX,• Load = 2 Series 74 TTL gatas	^t RAC	200	ns
^t dis(CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL gates	tOFF	0 50	រាន



		ALT.	TM4164	TM4164EC4-12 TM4164EC4-15		UNIT	
		SYMBOL	MIN	MAX	MIN	MAX	UNI
c(P)	Page-mode cycle time	tPC	130		160		ns
tc(rd)	Read cycle time [†]	tRC	230		260		ns
c(W)	Write cycle time	tWC	230		260		ns
tc(rdW)	Read-write/read-modify-write cycle time	tRWC					ns
W(CH)	Pulse duration, CAS high (precharge time) [‡]	tCP	50		50		ns
tw(CL)	Pulse duration, CAS low [§]	tCAS	75	10,000	90	10,000	ns
tw(RH)	Pulse duration, RAS high (precharge time)	tRP	80		100		ns
tw(RL)	Pulse duration, RAS low	tRAS	120	10,000	150	10,000	ns
tw(W)	Write pulse duration	tWP	40		45		ns
tt	Transition times (rise and fall) for RAS and CAS	tŢ	5	50	5	50	ns
tsu(CA)	Column-address setup time	tASC	0		0		ns
tsu(RA)	Row-address setup time	tASR	0		0		ns
tsu(D)	Data setup time	tDS	0		0		ns
tsu(rd)	Read-command setup time	tRCS	0		0		ns
tsu(WCH)	Write-command setup time before CAS high	tCWL	50		50	1	ns
tsu(WRH)	Write-command setup time before RAS high	tRWL	50		50		ns
th(CLCA)	Column-address hold time after CAS low	^t CAH	40		45		ns
th(RA)	Row-address hold time	tRAH	20		25		ns
th(RLCA)	Column-address hold time after RAS low	tAR	85		105		ns
th(CLD)	Data hold time after CAS low	^t DHC	45		50		ns
th(RLD)	Data hold time after RAS low	^t DHR	90		100		ns
th(WLD)	Data hold time after W low	tDHW	45		50		ns
th(CHrd)	Read-command hold time after CAS high	^t RCH	0		0		ns
th(RHrd)	Read-command hold time after RAS high	tRRH	5		5		ns
th(CLW)	Write-command hold time after CAS low	tWCH	45		50		ns
th(RLW)	Write-command hold time after RAS low	tWCR	90		100		ns
TRLCH	Delay time, RAS low to CAS high	tCSH	120		150		ns
tCHRL	Delay time, CAS high to RAS low	tCRP	0		0		ns
	Delay time, CAS low to RAS high	tRSH	60		100		ns
^t CLRH	Delay time, CAS low to W low	non					
tCLWL	(read-modify-write cycle only)	tCWD	50		60		ns
	Delay time, RAS low to CAS low						12
^t RLCL	(maximum value specified only to guarantee access time)	^t RCD	25	45	30	60	ns
^t RLWL	Delay time, RAS low to W low (read-modify-write cycle only)	tRWD	110		120	7. E.	ns
tWLCL	Delay time, W low to CAS low (early write cycle)	twcs	0		0		ns
trf	Befresh time interval	TREF		4		4	m

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, VIL max and VIH min must be met at the 10% and 90% points.

[†]All cycle times assume $t_t = 5$ ns.

[‡]Page mode only.

§In a read-modify-write cycle, t_{CLWL} and t_{su(WCH)} must be observed. Depending on the user's transition times, this may require additional CAS low time (t_{w(CL)}). This applies to page mode read-modify-write also.

In a read-modify-write cycle, tRLWL and t_{SU(WRH)} must be observed. Depending on the user's transition times, this may require additional RAS low time (tw(RL)).



		ALT.	TM416	4EC4-20	
		SYMBOL	MIN	MAX	UNI
c(P)	Page-mode cycle time	tPC	206		ns
c(rd)	Read cycle time [†]	^t RC	326		ns
c(W)	Write cycle time	twc	326		ns
c(rdW)	Read-write/read-modify-write cycle time	tRWC	345		ns
w(CH)	Pulse duration, CAS high (precharge time) [‡]	tCP	80		ns
w(CL)	Pulse duration, CAS low [§]	tCAS	135	10,000	ns
w(RH)	Pulse duration, RAS high (precharge time)	tRP	120		ns
w(RL)	Pulse duration, RAS low	^t RAS	200	10,000	ns
w(W)	Write pulse duration	tWP	55		ns
it .	Transition times (rise and fall) for RAS and CAS	tŢ	3	50	ns
su(CA)	Column-address setup time	tASC	0		ns
su(RA)	Row-address setup time	tASR	0		ns
su(D)	Data setup time	tDS	0		ns
su(rd)	Read-command setup time	tRCS	0		n
su(WCH)	Write-command setup time before CAS high	tCWL	60		ns
su(WRH)	Write-command setup time before RAS high	trwL	60		ns
h(CLCA)	Column-address hold time after CAS low	^t CAH	55		ns
h(RA)	Row-address hold time	tRAH	30		ns
h(RLCA)	Column-address hold time after RAS low	^t AR	120		ns
h(CLD)	Data hold time after CAS low	t DHC	60		ns
h(RLD)	Data hold time after RAS low	tDHR	125		ns
th(WLD)	Data hold time after W low	tDHW	60		ns
th(CHrd)	Read-command hold time after CAS high	tRCH	0		ns
th(RHrd)	Read-command hold time after RAS high	tran transfer	5		n
th(CLW)	Write-command hold time after CAS low	twch	60		ns
th(RLW)	Write-command hold time after RAS low	twcr	145		лs
RLCH	Delay time, RAS low to CAS high	tCSH	200		ns
CHRL	Delay time, CAS high to RAS low	tCRP	0		ns
	Delay time, CAS low to RAS high	tRSH	135		
	Delay time, CAS low to W low	<u></u>			
^t CLWL	(read-modify-write cycle only)	tCWD	65		ns
	Delay time, RAS low to CAS low		+		
RLCL	(maximum value specified only	t _{RCD}	35	65	ля
INLUL	to guarantee access time)				
	Delay time, RAS low to W low				
^t RLWL	(read-modify-write cycle only)	^t RWD	130		ាទ
	Delay time, W low to CAS				
tWLCL	• • • • • • • • • • • • • • • • • • • •	twcs	0		l ns

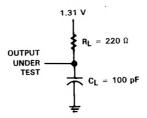
NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, VIL max and VIH min must be met at the 10% and 90% points.

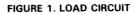
[†]All cycles times assume $t_t = 5$ ns.

[‡]Pege mode only.

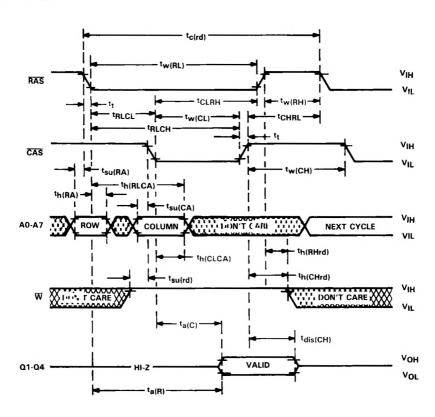
In a read-modify-write cycle, tCLWL and t_{su(WCH)} must be observed. Depending on the user's transition times, this may require additional CAS low time (t_{w(CL)}). This applies to page mode read-modify-write also.

PARAMETER MEASUREMENT INFORMATION



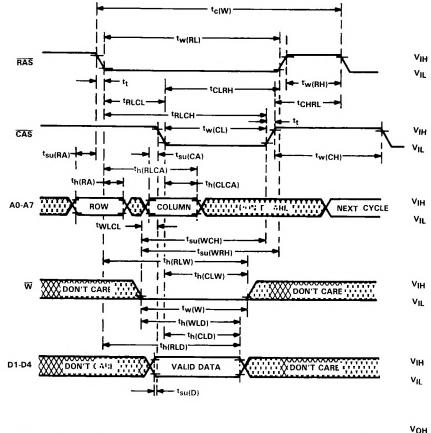


read cycle timing





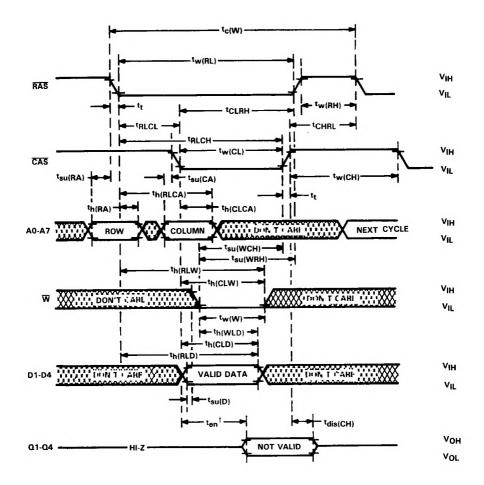
early write cycle timing





Dynamic RAM Modules

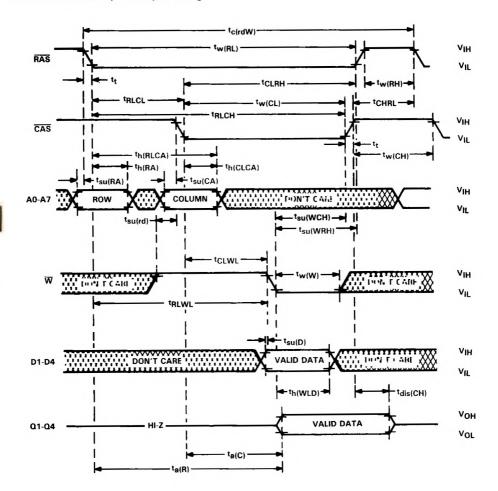
write cycle timing



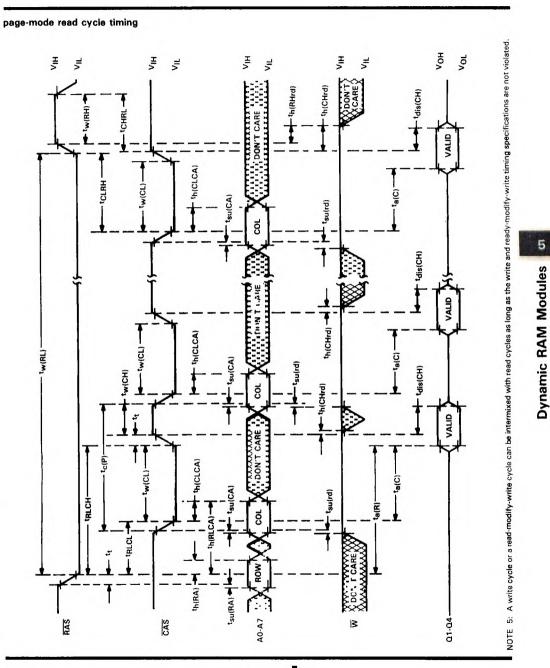
[†] The enable time (t_{en)} for a write cycle is equal in duration to the access time from CAS (t_{a(C)}) in a read cycle; but the active levels at the output are invalid.



read-write/read-modify-write cycle timing





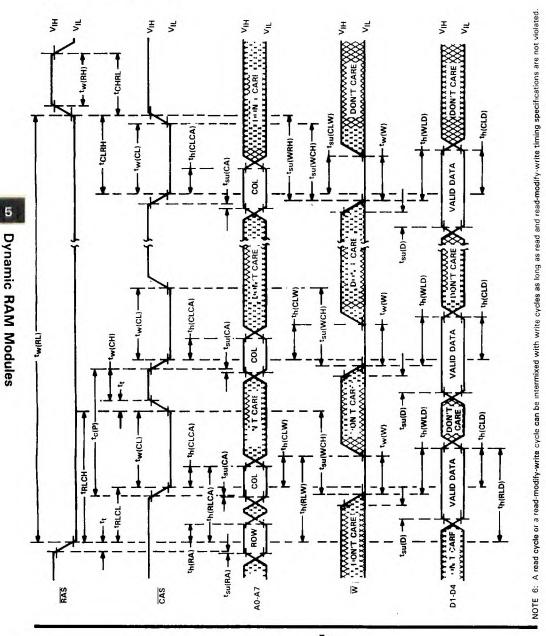


5-63

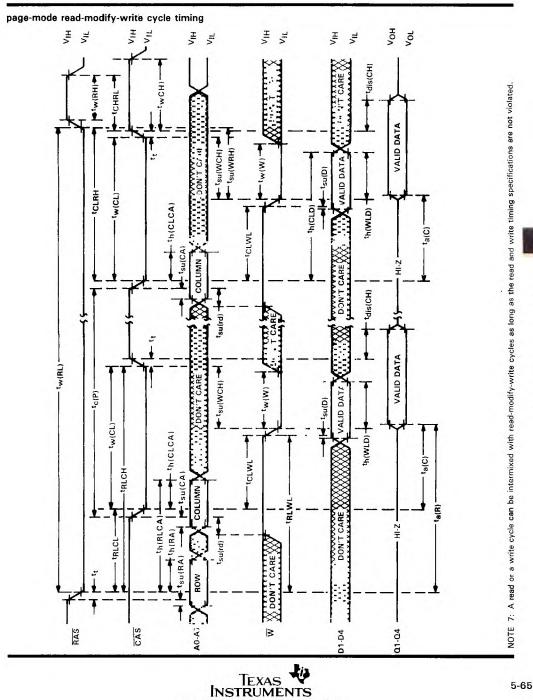
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page-mode write cycle timing



TEXAS W INSTRUMENTS POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

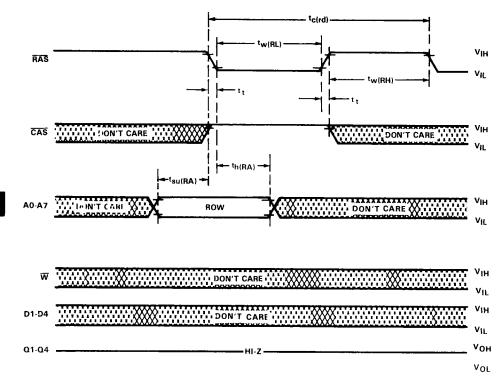


POST OFFICE BOX 1443 . HOUSTON, TEXAS 77001

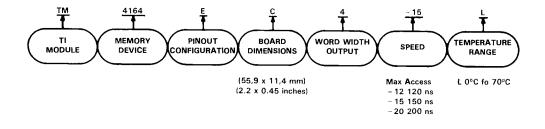
5-65

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RAS-only refresh timing



TI single-in-line package nomenclature





Dynamic RAM Modules

TM4164EL9, TM4164FM9 65,536 BY 9-BIT DYNAMIC RAM MODULES

TM4164EL9 . . . L SINGLE-IN-LINE PACKAGE[†]

NO. . REVISED NOVEMBER 1985

- 65,536 X 9 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
- Utilizes Nine 64K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

	ACCESS	ACCESS	READ
	TIME	TIME	OR
	ROW	COLUMN	WRITE
	ADDRESS	ADDRESS	CYCLE
	(MAX)	(MAX)	(MIN)
TM41649-12	120 ns	75 ns	230 ns
TM41649-15	150 ns	90 ns	260 ns
TM41649-20	200 ns	135 ns	326 ns

- Common CAS Control for Eight Common Data-In and Data-Out Lines
- Separate CAS Control for One Separate Pair of Data-In and Data-Out Lines
- Low Power Dissipation:

description

	OPERATING (TYP)	STANDBY (TYP)
TM41649-12	1800 mW	157.5 mW
TM4164 9-15	1575 mW	157.5 mW
TM4164 9-20	12 15 mW	157 5 mW

• Operating Free-Air Temperature . . . 0 °C to 70 °C

The TM4164__9 series are 576K, dynamic random-access memory modules organized as $65,536 \times 9$ bits [bit nine (D9, Q9) is generally used for parity and is controlled by CAS9] in a 30-pin single-in-line package comprising nine TMS4164FPL, $65,536 \times 1$ bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with nine 0.1 μ F decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior

TM4164FM9 . . . M SINGLE-IN-LINE PACKAGE (TOP VIEW) VDD (1) 5 CAS (2) = DQ1 (3) = AO (4) (5) < A1 DO2 (6) ⊂ A2 (7) c A3 (8) < (9) Vss DQ3 (10)c A4 (11) c A5 (12) = DQ4 (13)e A6 (14) -A7 (15) -DQ5 (16) = NC[‡] (17)⁵ NC (18)= NC (19)= DO6 (20) W (21)= VSS (22)= DQ7 (23)= NC (24)-DO8 (25) C Q9 (26)= RAS (27) CAS9 (28) D9 (29) VDD (30)

[†]TM4164EL9 package is shown.

[‡]Pin 17 of the 256K \times 9 SIP will be memory address A8.

PIN NOMENCLATURE							
A0-A7	Address Inputs						
CAS, CAS9	CAS, CAS9 Column-Address Strobes						
DQ1-DQ8 Data In/Data Out							
D9	Data In						
NC	No Connection						
Q9	Data Out						
RAS	Row-Address Strobe						
VDD	5-V Supply						
VSS	Ground						
W	Write Enable						

performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM4164__9 has a density of ten devices per square inch (approximately 4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

PRDDUCTIDN UA1A focuments - u information current as of util intion dato from its conform to specifications processing does not standard warrenty. Production processing does not necessarily include testing of all parameters.



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5-67

TM4164EL9, TM4164FM9 65,536 BY 9-BIT DYNAMIC RAM MODULES

The TM4164__9 features RAS access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation as low as 1215 mW typical operating and 157.5 mW typical standby.

Refresh period is extended to 4 mi · ...conds, and during this period each of the 256 rows must be strobed with RAS in order to retain data. • ...5 can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4164__9 is rated for operation from 0°C to 70°C.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations on each of the nine chips. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe (RAS). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobes (CAS for M1 thru M8 and CAS9 for M9). All addresses must be stable on or before the falling edges of RAS and CAS. RAS is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. CAS9 is used as a chip select activating the column decoder and the input and output buffers for M1-M8. CAS9 is used similarly for M9.

write enable (W)

The read or write mode is selected through the write-enable (\overline{W}) input. A logic high on the \overline{W} input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM4164__9 dictates the use of early write cycles to prevent contention on D and Q. When \overline{W} goes low prior to \overline{CAS} , the data outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ8, D9)

Data is written during a write cycle. The falling edge of \overline{CAS} or \overline{W} strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, \overline{W} is brought low prior to \overline{CAS} and the data is strobed in by \overline{CAS} with setup and hold times referenced to this signal.

data out (DQ1-DQ8, Q9)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state until \overline{CAS} is brought low. In a read cycle the outputs go active after the access time interval $t_a(C)$ that begins with the negative transition of \overline{CAS} as long as $t_a(R)$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while \overline{CAS} is low; \overline{CAS} going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state, a necessity due to the common I/O feature of the TM4164__9.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless \overline{CAS} is applied, the \overline{RAS} -only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with \overline{RAS} causes all bits in each row to be refreshed. \overline{CAS} can remain high (inactive) for this refresh sequence to conserve power.



page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on M1-M9, the row address and RAS are applied to multiple modules. CAS is then decoded to select the proper module.

power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, \overrightarrow{RAS} must remain high for 100 μ s immediately prior to initialization. Initialization consists of performing eight \overrightarrow{RAS} cycles before proper device operation is achieved.

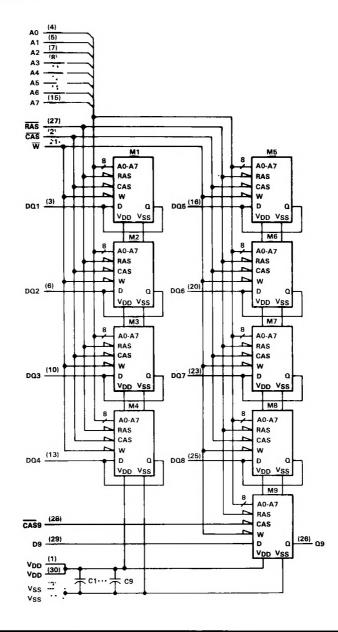
single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness Bypass capacitors: Multilayer ceramic Leads: Tin/lead solder coated over phosphor-bronze Contact area for socketable devices: Nickel plate and solder plate on top of copper



TM4164EL9, TM4164FM9 65,536 BY 9-BIT DYNAMIC RAM MODULES

functional block diagram





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Voltage range for any pin except VDD and data out (see Note 1)	-1.5 V to 10 V
Voltage range on VDD supply and data out with respect to VSS	
Short circuit output current for any output	50 mA
Power dissipation	9 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range6	5°C to 150°C

[†]Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to VSS.

recommended operating conditions

°			MIN	NOM	MAX	UNIT
VDD	Supply voltage		4.5	5	5.6	+
Vss	Supply voltage			0		V
2.00	18.1.1	V _{DD} = 4.5 V	2.4	1000	4.8	1 v
VIH	High-level input voltage	$V_{DD} = 5.5 V$	2.4		6	V
VIL	Low-level input voltage(see Note	Low-level input voltage(see Notes 2 and 3)			0.8	V
TA	Operating free-air temperature		0	-	70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

Due to input protection circuitry, the applied voltage may begin to clamp at -0.6 V. Test conditions should comprehend this
occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST		TM41649-12		TM4164 _9-15			
		CONDITIONS	MIN TYPT M		MAX	MAX MIN I		MAX	UNIT
VOH	High-level output voltage	$I_{OH} = -5 \text{ mA}$	2.4			2.4			v
VOL	Low-level output voltage	IOL = 4.2 mA	1.000		0.4			0.4	V
4	Input current (leakage)	$V_I = 0$ V to 5.8 V, $V_{DD} = 5$ V, All other pins = 0 V			±10			± 10	μA
ю	Output current (leakage)	$V_0 = 0.4 \text{ to } 5.5 \text{ V},$ $V_{DD} = 5 \text{ V},$ $\overline{CAS} \text{ high}$	1		±10			±10	μА
IDD1 [‡]	Average operating current during read or write cycle	t _C = minimum cycle, All outputs open		360	432		315	405	mA
IDD2 [‡]	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open		31.5	45		31.5	45	mA
DD3‡	Average refresh current	$t_c = minimum cycle,$ CAS high and RAS cycling, All outputs open		252	360		225	333	mA
IDD4 [‡]	Average page-mode current	t _{c(P)} = minimum cycle, RAS low and CAS cycling, All outputs open		252	360		225	333	mA

[†]All typical values are at T_A = 25°C and nominal supply voltages.

[‡]IDD1-IDD4 are measured with M1-M9 in the same mode (i.e., operating, standby, refresh or page mode).



TM4164EL9, TM4164FM9 65,536 BY 9-BIT DYNAMIC RAM MODULES

PARAMETER		PARAMETER		164	9-20	
	PARAMETER	CONDITIONS	MIN	TYP [†]	MAX	UNIT
VOH	High-level output voltage	$I_{OH} = -5 \text{ mA}$	2.4		- 25.	V
VOL	Low-level output voltage	$I_{OL} = 4.2 \text{ mA}$			0.4	V
կ	Input current (leakage)	$V_I = 0 V$ to 5.8 V, $V_{DD} = 5 V$ All other pins = 0 V			±10	μA
¹ 0	Output current (leakage)	$V_{O} = 0.4$ to 5.5 V, $V_{DD} = 5$ V, \overline{CAS} high			±10	μΑ
IDD1 [‡]	Average operating current during read or write cycle	t _C = minimum cycle, All outputs open		243	333	mA
¹ DD2 [‡]	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open	3	31.5	45	mA
IDD3‡	Average refresh current	t _C = minimum cycle, CAS high and RAS cycling, All outputs open		180	288	mA
I _{DD4} ‡	Average page-mode current	t _{c(P)} = minimum cycle, RAS low and CAS cycling, All outputs open		180	288	mA

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

[†]All typical values are at $T_A = 25 \,^{\circ}C$ and nominal supply voltages.

[‡]IDD1-IDD4 are measured with M1-M9 in the same mode (i.e., operating, standby, refresh or page mode).

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MAX	UNIT	
Ci(A)	Input capacitance, address inputs	45	• pF	
Ci(DQ)	Input capacitance, inputs	11	pF	
Ci(RAS)	Input capacitance, i 👫 input	72	pF	
Ci(W)	Input capacitance, W input	72	pF	
Ci(CAS9)	Input capacitance, CAS9 input	8	pF	
Ci(CAS)	Input capacitance, CAS input	72	pF	
Ci(D9)	Input capacitance, D9 input	5	pF	
Co(Q9)	Output capacitance, Q9 output	6	pF	

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		PARAMETER TEST CONDITIONS		TM4164 MIN	9-12 MAX	TM41649-15		UNIT
^t a(C)	Access time from CAS	CL = 100 pF, Load = 2 Series 74 TTL gates	^t CAC		75		90	ns
t _{a(R)}	Access time from RAS	tRLCL = MAX, Load = 2 Series 74 TTL gates	^t RAC		120		150	ns
^t dis(CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL gates	tOFF	0	40	0	40	ns



switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		PARAMETER TEST CONDITIONS		TM4164.9-20 MIN MAX	UNIT
^t a(C)	Access time from CAS	CL = 100 pF, Load = 2 Series 74 TTL gates	^t CAC	135	ns
^t a(R)	Access time from RAS	t _{RLCL} = MAX, Load = 2 Series 74 TTL gates	^t RAC	200	ns
^t dis(CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL gates	tOFF	0 50	ns



		ALT.	TM416	49-12	TM4164	9-15	
		SYMBOL	MIN	MAX	MIN	MAX	UNIT
tc(P)	Page-mode cycle time	tPC	130		160		ns
tc(rd)	Read cycle time [†]	tRC	230		260		ns
tc(W)	Write cycle time	tWC	:		260		ns
tw(CH)	Pulse duration, CAS high (precharge time) [‡]	tCP	50		50		ns
tw(CL)	Pulse duration, CAS low	tCAS	75	10,000	90	10,000	ns
tw(RH)	Pulse duration, RAS high (precharge time)	tRP	80	-	100		ns
tw(RL)	Pulse duration, RAS low	TRAS	120	10,000	150	10,000	ns
tw(W)	Write pulse duration	tWP	40		45		ns
tt	Transition times (rise and fall) for RAS and CAS	tŢ	10	50	10	50	ns
tsu(CA)	Column-address setup time	tASC	0		0		ns
tsu(RA)	Row-address setup time	tASR	0		0		ns
t _{su(D)}	Data setup time	tDS	0		0		ns
t _{su(rd)}	Read-command setup time	tRCS	0		0		ns
t _{su} (WCH)	Write-command setup time before CAS high	tCWL	50		50	_	ns
t _{su} (WRH)	Write-command setup time before RAS high	tRWL	50		50		ns
th(CLCA)	Column-address hold time after CAS low	tCAH	40		45		ns
th(RA)	Row-address hold time	^t RAH	20		25		ns
th(RLCA)	Column-address hold time after RAS low	tAR	90		100		ns
th(CLD)	Data hold time after CAS low	^t DHC	45		50		ns
th(RLD)	Data hold time after RAS low	^t DHR	90		100		ns
th(CHrd)	Read-command hold time after CAS high	^t RCH	o		0		ns
th(RHrd)	Read-command hold time after RAS high	tRRH	5		5		ns
th(CLW)	Write-command hold time after CAS low	tWCH	45		50		ns
th(RLW)	Write-command hold time after RAS low	tWCR	90		100		ns
TRLCH	Delay time, RAS low to CAS high	tCSH	120		150		ns
tCHRL	Delay time, CAS high to RAS low	tCRP	0	0	0		ns
TCLRH	Delay time, CAS low to RAS high	tRSH	60		100		ns
^t RLCL	Delay time, RAS low to CAS low (maximum value specified only) to guarantee access ···	^t RCD	25	45	30	60	ns
tWLCL	Delay time W low to in the second sec	twcs	0		0		ns
trf	Refresh time interval	TREF		4		4	ms

timing requirements over recommended supply voltage range and operating free-air temperature range

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, VIL max and VIH min must be met at the 10% and 90% points.

[†]All cycle times assume $t_t = 5$ ns. The specified t_t is due to testing limitations. Transition times may be as little as 3 ns in system use. [‡]Page mode only.



Dynamic RAM Modules

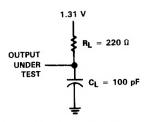
		ALT.	TM41649-20	UNIT
		SYMBOL	MIN MAX	
tc(P)	Page-mode cycle time	tPC	206	ns
tc(rd)	Read cycle time [†]	tRC	236	ns
tc(W)	Write cycle time	twc	326	ns
tw(CH)	Pulse duration, CAS high (precharge time) [‡]	tCP	80	ns
tw(CL)	Pulse duration, CAS low	tCAS	135 10,000	ns
tw(RH)	Pulse duration, RAS high (precharge time)	tRP	120	ns
tw(RL)	Pulse duration, RAS low	tRAS	200 10,000	ns
tw(W)	Write pulse duration	twp	55	ns
t _t	Transition times (rise and fall) for RAS and CAS	tŢ	10 50	ns
t _{su} (CA)	Column-address setup time	tASC	0	ns
^t su(RA)	Row-address setup time	tASR	0	ns
t _{su} (D)	Data setup time	tDS	0	ns
tsu(rd)	Read-command setup time	tRCS	0	ns
tsu(WCH)	Write-command setup time before CAS high	tCWL	60	ns
t _{su} (WRH)	Write-command setup time before RAS high	tRWL	60	ns
th(CLCA)	Column-address hold time after CAS low	^t CAH	55	ns
th(RA)	Row-address hold time	trah	30	лs
th(RLCA)	Column-address hold after RAS low	tAR	125	ns
th(CLD)	Data hold time after ':' ow	tDHC	60	ns
th(RLD)	Data hold time after RAS low	^t DHR	145	ns
th(CHrd)	Read-command hold time after CAS high	^t RCH	0	ns
th(RHrd)	Read-command hold time after RAS high	tRRH	5	ns
th(CLW)	Write-command hold time after CAS low	tWCH	60	ns
th(RLW)	Write-command hold time after RAS low	twcr	145	ns
TRLCH	Delay time, RAS low to CAS high	tCSH	200	ns
tCHRL	Delay time, CAS high to RAS low	tCRP	0	ns
tCLRH	Delay time, CAS low to RAS high	tRSH	135	ns
^t RLCL	Delay time, RAS low to ow (maximum value specified only to guarantee access time)	tRCD	35 65	ns
tWLCL	Delay time, W low to CAS low (early write cycle)	twcs	0	ns
t _{rf}	Refresh time interval	tREF	4	ms

timing requirements over recommended supply voltage range and operating free-air temperature range

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

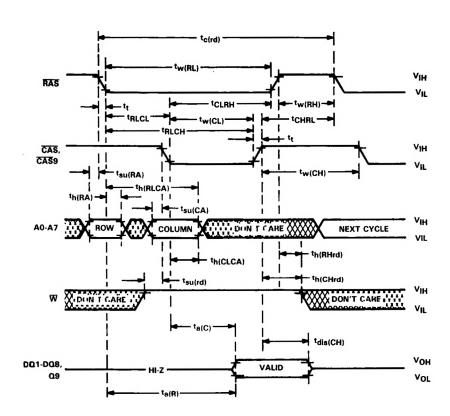
[†]All cycle times assume $t_t = 5$ ns. The specified t_t is due to testing limitations. Transition times may be as little as 3 ns in system use. [‡]Page mode only.

PARAMETER MEASUREMENT INFORMATION

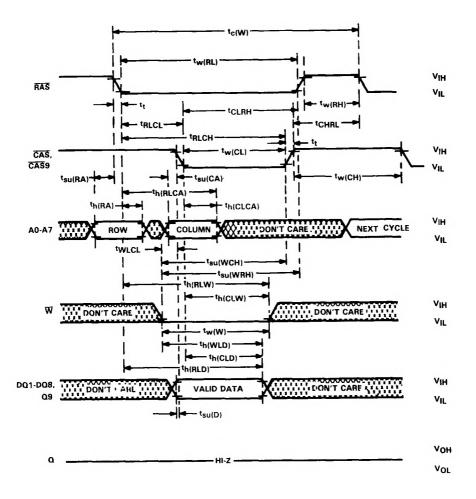




read cycle timing

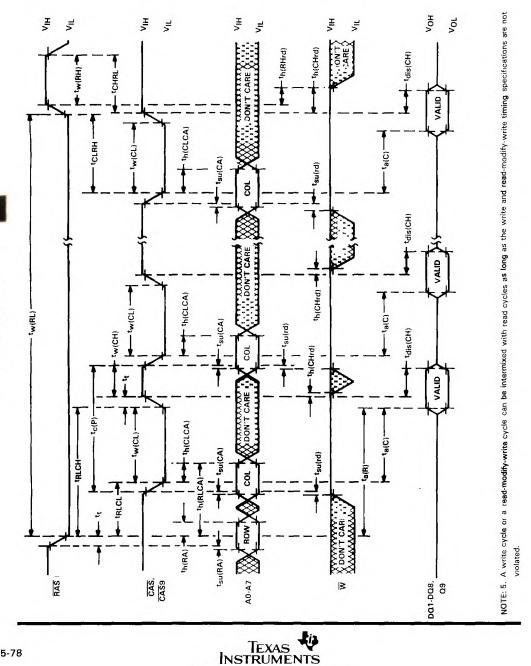


early-write cycle timing





page-mode read cycle timing



Dynamic RAM Modules

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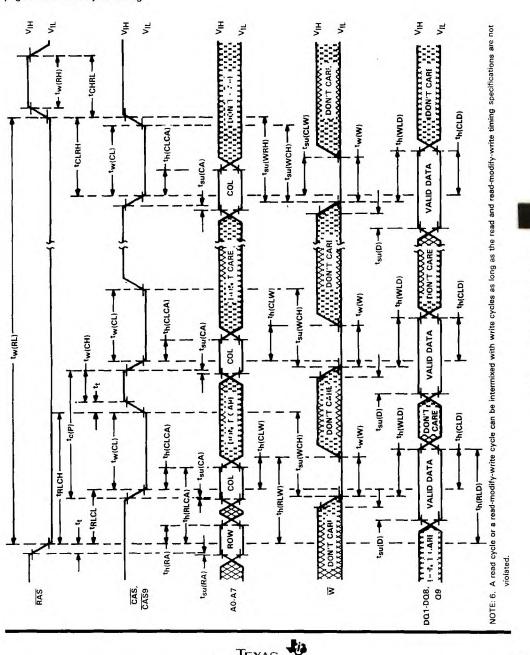
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Dynamic RAM Modules

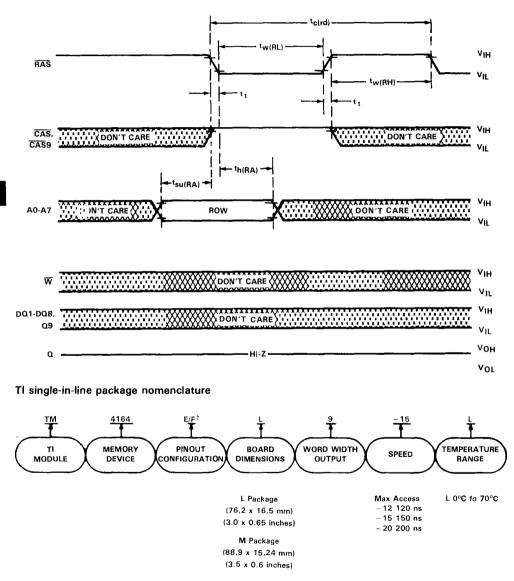
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TEXAS TO INSTRUMENTS

RAS-only refresh timing



[†]The E pinout configuration designator is used when specifying the L package; the F pinout configuration version designator is used when specifying the M package.



Dynamic RAM Modules

ADVANCE INFORMATION

TM4164EQ5 65,536 BY 5-BIT DYNAMIC RAM MODULE

NOVE

SEPTEMBER

- 65,536 X 5 Organization
- Single 5-V Supply (10% Tolerance)
- 24-Pin Single-in-Line Package (SIP)
- Utilizes Five 64K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

	ACCESS TIME ROW	ACCESS TIME COLUMN	READ OR WRITE	READ- MODIFY- WRITE
	ADDRESS (MAX)		CYCLE (MIN)	CYCLE (MIN)
TM4164EQ5-12	120 ns	75 ns	230 ns	260 ns
TM4164EQ5-15	150 ns	90 ns	260 ns	285 ns
TM4164EQ5-20	200 ns	135 ns	330 ns	345 ns

- Common CAS Control with Separate Data-In and Data-Out Lines with an "Early Write" Feature
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)	
TM4161EQ5-12	1000 mW	88 mW	
TM4164EQ5-15	875 mW	88 mW	
TM4164EQ5-20	675 mW	88 mW	

- Operating Free-Air Temperature . . . 0 °C to 70 °C
- Upward Compatible with 256K X 5 Singlein-Line Package

description

The TM4164EQ5 is a 320K, dynamic randomaccess memory module organized as 65,536 × 5 bits in a 24-pin single-in-line package comprising five TMS4164FPL, 65,536 × 1 bit

Q SINGLE-IN-LINE PACKAGE (TOP VIEW) NC (1) -VDD (2) D1 (3) Q1 (4) = CAS (5) A7 (6)= (7) 0 A5 A4 (8) D2 (9)= 02 (10) Ŵ (11) A1 (12) A3 (13)= A6 (14)= Q3 (15) D3 (16)= A2 (17)= AO (18) RAS (19) D4 (20) 04 (21)= VSS (22) = D5 (23) Q5 (24)

	PIN NOMENCLATURE
A0-A7	Address Inputs
CAS	Column-Address Strobe
D1-D5	Data Inputs
NC	No Connection
Q1-Q5	Data Outputs
RAS	Row-Address Strobe
VDD	5-V Supply
VSS	Ground
W	Write Enable

dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with five 0.1 μ F decoupling capacitors. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM4164EQ5 has a density of six devices per square inch (approximately 2.4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4164EQ5 is rated for operation from 0°C to 70°C.



upward compatibility

Future 256K × 5 memory modules in single-in-line packages will have identical pin functions and spacing, and will be directly upward compatible. Pin 1 of the TM4256EQ5 (256K × 5 SIP) module will be memory address A8.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations on each of the five chips. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe (\overline{RAS}). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe (\overline{CAS}). All addresses must be stable on or before the falling edges of \overline{RAS} and \overline{CAS} . \overline{RAS} is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. \overline{CAS} is used as a chip select activating the column decoder and the input and output buffers.

write enable (W)

The read or write mode is selected through the write-enable (\overline{W}) input. A logic high on the \overline{W} input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. When \overline{W} goes low prior to \overline{CAS} , the data-outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D1-D5)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of \overrightarrow{CAS} or \overrightarrow{W} strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early-write cycle, \overrightarrow{W} is brought low prior to \overrightarrow{CAS} and the data is strobed in by \overrightarrow{CAS} with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, \overrightarrow{CAS} will already be low, thus the data will be strobed in by \overrightarrow{W} with setup and hold times referenced to this signal.

data out (Q1-Q5)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state until CAS is brought low. In a read cycle the outputs go active after the access time interval $t_{a}(C)$ that begins with the negative transition of CAS as long as $t_{a}(R)$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while CAS is low; CAS going high returns them to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless \overline{CAS} is applied, the \overline{RAS} -only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with \overline{RAS} causes all bits in each row to be refreshed. \overline{CAS} can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single module, the row address and RAS are applied to multiple modules. CAS is then decoded to select the proper module.



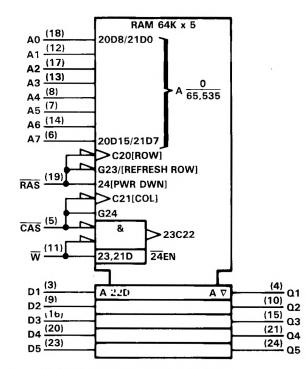
power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, \overline{RAS} must remain high for 100 μ s immediately prior to initialization. Initialization consists of performing eight \overline{RAS} cycles before proper device operation is achieved.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness Bypass capacitors: Multilayer ceramic Leads: Tin/lead solder coated over phosphor-bronze

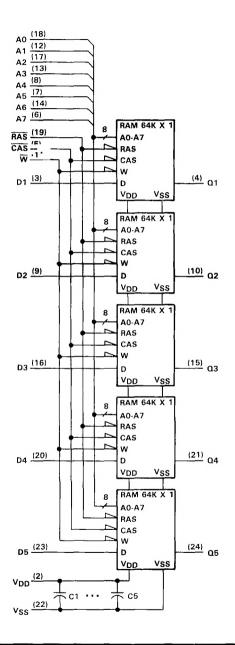
logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



functional block diagram



TEXAS INSTRIMENTS POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Voltage range on any pin except VDD and data out (see Note 1)
Voltage range on VDD supply and data out with respect to VSS $\dots - 1$ V to 6 V
Short circuit output current for any output
Power dissipation
Operating free-air temperature range
Storage temperature range

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to VSS.

recommended operating conditions

			MIN	NOM	MAX	UNIT
VDD	Supply voltage		4.5	5	5.5	v
VSS	Supply voltage			0		v
	High-level input voltage	$V_{DD} \approx 4.5 V$	2.4		4.8	v
VIH		$V_{DD} \approx 5.5 V$	2.4		6	v
VIL	Low-level input voltage (see Notes 2 and 3)		-0.6		0.8	v
TA	Operating free-air temperature		0		70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

Due to input protection circuitry, the applied voltage may begin to clamp at -0.6 V. Test conditions should comprehend this
occurrence. See application report entitled ''TMS4164A and TMS4416 Input Protection Diode'' on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST		4164EQ	5-12	TM4164EQ5-15			UNIT		
	FANAMICICN	CONDITIONS	MIN	TYP	MAX	MIN	TYP [†]	MAX	UNIT		
VOH	High-level output voltage	1 _{OH} = -5 mA	2.4	2.4	2.4			2.4			V
VOL	Low-level output voltage	OL = 4.2 mA			0.4			0.4	V		
ų	Input current (leakage)	$V_I = 0 V$ to 5.8 V, $V_{DD} = 5 V$, All other pins = 0 V			± 10			±10	μA		
lo	Output current (leakage)	Vo = 0.4 V to 5.5 V, Vn = 5 V, 'igh			±10			±10	μA		
IDD1	Average operating current during read or write cycle	t _C = minimum cycle, All outputs open		160	192		140	180	mA		
IDD2	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open		14	20		14	20	mA		
IDD3	Average refresh current	t _C = minimum cycle, CAS high and RAS cycling, All outputs open		112	160		100	148	mA		
IDD4	Average page-mode current	t _{c(P)} = minimum cycle, RAS low and CAS cycling, All outputs open		112	160		100	148	mA		

[†]All typical values are at $T_A = 25 \,^{\circ}C$ and nominal supply voltages.



PARAMETER		TEST		
		CONDITIONS	MIN TYP [†] MAX	UNIT
VOH	High-level output voltage	$I_{OH} = -5 \text{ mA}$	2.4	V
VOL	Low-level output voltage	I _{OL} = 4.2 mA	0.4	V
li –	Input current (leakage)	$V_{I} = 0 V$ to 5.8 V, $V_{DD} = 5 V$, All other pins = 0 V	±10	μΑ
ю	Output current (leakage)	$V_{O} = 0.4 V \text{ to } 5.5 V,$ $V_{DD} = 5 V,$ CAS high	. ±10	μΑ
DD1	Average operating current during read or write cycle	t _c = minimum cycle, All outputs open	108 148	mA
DD2	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open	14 20	mA
DD3	Average refresh current	t _c = minimum cycle, CAS high and RAS cycling, All outputs open	80 128	mA
DD4	Average page-mode current	t _{C(P)} = minimum cycle, RAS low and CAS cycling, All outputs open	80 128	mA

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

[†]All typical values are at $T_A = 25 \,^{\circ}C$ and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MAX	UNIT
Ci(A)	Input capacitance, address inputs	TBD	pF
Ci(D)	Input capacitance, data input	TBD	pF
Ci(RC)	Input capacitance strobe inputs	TBD	pF
Ci(W)	Input capacitance, write enable input	TBD	pF
Co	Output capacitance	TBD	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

	PARAMETER		ALT.	TM4164EQ5-12		TM4164EQ5-15					
	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	N MAX	MIN	MAX	UNIT			
ta(C)	Access time from CAS	$C_L = 100 \text{ pF},$ Load = 2 Series 74 TTL gates	¹ CAC	¹ CAC	1CAC	1CAC		75		90	ns
ta(R)	Access time from RAS	tRLCL = MAX, Load = 2 Series 74 TTL gates	^t RAC		120		150	ns			
tdis(CH)	Output disable time after CAS high	$C_L = 100 \text{ pF},$ Load = 2 Series 74 TTL gates	tOFF	0	40	0	40	ns			

Additional information on these products can be obtained from the factory as it becomes available.



switching characteristics over recommended supply voltage range and operating free-air temperature range

	PARAMETER	TEST CONDITIONS	ALT. SYMBOL tCAC	TM4164EQ5-20		UNIT
	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNIT
t _a (C)	Access time from CAS	C _L = 100 pF, Load = 2 Series 74 TTL gates	tCAC		135	ns
t _a (R)	Access time from RAS	t _{RLCL} = MAX, Load = 2 Series 74 TTL gates	^t RAC		200	ns
tdis(CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL gates	tOFF	0	50	ns



		ALT.	TM416	4EQ5-12	TM416	4EQ5-15	;	
		SYMBOL	MIN	MAX	MIN	MA	UNI	
t _{c(P)}	Page-mode cycle time	tPC	130		160		ns	
tc(rd)	Read cycle time [†]	^t RC	230		260		ns	
t _{c(W)}	Write cycle time	twc	230		260		ns	
^t c(rdW)	Read-write/read-modify-write cycle time	tRWC	260		285		ns	
tw(CH)	Pulse duration, CAS high (precharge time) [‡]	tCP	50		50		ns	
tw(CL)	Pulse duration, CAS low [§]	tCAS	75	10,000	90	10,000	ns	
tw(RH)_	Pulse duration, RAS high (precharge time)	tRP	80		100		ns	
t _{w(RL)}	Pulse duration, RAS low	^t RAS	120	10,000	150	10,000	ns	
tw(W)	Write pulse duration	twp	40		45		ns	
t _t	Transition times (rise and fall) for RAS and CAS	tŢ	5	50	5	50	ns	
tsu(CA)	Column-address setup time	tASC	0		0		ns	
t _{su(RA)}	Row-address setup time	tASR	0		0		ns	
t _{su(D)}	Data setup time	tDS	0		0		ns	
tsu(rd)	Read-command setup time	tRCS	0		0		ns	
t _{su(WCH)}	Write-command setup time before CAS high	t <u>CWL</u>	50		50		ns	
t _{su} (WRH)	Write-command setup time before RAS high	^t RWL	50		50		ns	
th(CLCA)	Column-address hold time after CAS low	^t CAH	40		45		ns	
th(RA)	Row-address hold time	^t RAH	. 20		25		ns	
th(RLCA)	Column-address hold time after RAS low	tAR	90		100		ns	
th(CLD)	Data hold time after CAS low	^t DHC	45		50		ns	
th(RLD)	Data hold time after RAS low	^t DHR	90		100		ns	
^t h(WLD)	Data hold time after \overline{W} low	^t DHW	40		45		ns	
th(CHrd)	Read-command hold time after CAS high	^t RCH	0		0		ns	
th(RHrd)	Read-command hold time after RAS high	tRRH	5		5		ns	
th(CLW)	Write-command hold time after CAS low	tWCH	45		50		ns	
th(RLW)	Write-comr nold time after RAS low	twcr	90		100		ns	
^t RLCH	Delay time, Iow to CAS high	tCSH	120		150		ns	
^t CHRL	Delay time, CAS high to RAS low	tCRP	0		0		ns	
^t CLRH	Delay time, CAS low to RAS high	tRSH	60		100		ns	
	Delay time, CAS low to W low							
tCLWL	(read-modify-write cycle only)	tCWD	50		60		n	
	Delay time, RAS low to CAS low		<u> </u>				T	
^t RLCL	(maximum value specified only	^t RCD	20	· 45	25	60	ns	
	to guarantee access time)							
	Delay time, RAS low to W low		110		120			
	(read-modify-write cycle only)	^t RWD			120		ns	
•••••	Delay time, W low to CAS		0		0			
twlcl	low (early write cycle)	twcs					ns	
t _{rf}	Refresh time interval	^t REF		4		4	m	

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, VIL max and VIH min must be met at the 10% and 90% points.

[†]All cycles times assume $t_t = 5$ ns.

[‡]Page mode only.

[§]In a read-modify-write cycle, t_{CLWL} and t_{su(WCH)} must be observed. Depending on the user's transition times, this may require additional CAS low time (t_{w(CL})). This applies to page mode read-modify-write also.

In a read-modify-write cycle, t_{RLWL} and t_{su(WRH)} must be observed. Depending on the user's transition times, this may require additional RAS low time (t_{w(RL)}).

		ALT.	TM4164EQ5-20	UNIT
		SYMBOL	MIN MAX	UNIT
tc(P)	Page-mode cycle time	tPC	206	ns
c(rd)	Read cycle time [†]	tRC		ns
c(W)	Write cycle time	twc	1.1	ns
c(rdW)	Read-write/read-modify-write cycle time	tRWC	345	ns
w(CH)	Pulse duration, CAS high (precharge time) [‡]	tCP	80	ns
w(CL)	Pulse duration, CAS low [§]	tCAS	135 10,000	ns
w(RH)	Pulse duration, RAS high (precharge time)	tRP	120	ns
w(RL)	Pulse duration, RAS low	tRAS	200 10,000	ns
tw(W)	Write pulse duration	twp	55	ns
tt	Transition times (rise and fall) for RAS and CAS	tτ	3 50	ns
su(CA)	Column-address setup time	tASC	ō	ns
su(RA)	Row-address setup time	tASR	0	ns
su(D)	Data setup time	tDS	0	ns
su(rd)	Read-command setup time	tRCS	0	ns
tsu(WCH)	Write-command setup time before CAS high	tCWL	60	ns
su(WRH)	Write-command setup time before RAS high	tRWL	60	ns
h(CLCA)	Column-address hold time after CAS low	tCAH	55	ns
th(RA)	Row-address hold time	tRAH	30	ns
h(RLCA)	Column-address hold time after RAS low	tAR	125	ns
th(CLD)	Data hold time after CAS low	^t DHC	60	ns
th(RLD)	Data hold time after RAS low	tDHR	145	ns
th(WLD)	Data hold time after W low	tDHW	55	ns
th(CHrd)	Read-command hold time after CAS high	^t RCH	0	ns
th(RHrd)	Read-command hold time after RAS high	tRRH	5	ns
th(CLW)	Write-command hold time after CAS low	twch	60	ns
th(RLW)	Write-command hold time after RAS low	tWCR	145	ns
tRLCH	Delay time, RAS low to CAS high	tCSH	200	ns
tCHRL	Delay time, CAS high to RAS low	tCRP	0	ns
tCLRH	Delay time, CAS low to RAS high	tRSH	135	ns
·CLRH	Delay time, CAS low to W low			
tCLWL	(read-modify-write cycle only)	tCWD	65	ns
	Delay time, RAS low to CAS low			
TRLCL	(maximum value specified only	tRCD	30 65	ns
HLUL	to guarantee access time)			
	Delay time, RAS low to W low	Company and the state of the	100	
^t RLWL	(read-modify-write cycle only)	tRWD	130	ns
2.50	Delay time, W low to CAS		0	
tWLCL	low (early write cycle)	twcs	0	ns
trf	Refresh time interval	tREF	4	m

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, VIL max and VIH min must be met at the 10% and 90% points.

[†]All cycles times assume $t_t = 5$ ns.

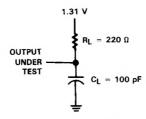
[‡]Page mode only.

§In a read-modify-write cycle, t_{CLWL} and t_{su}(WCH) must be observed. Depending on the user's transition times, this may require additional CAS low time (t_w(CL)). This applies to page mode read-modify-write also.

In a read-modify-write cycle, tRLWL and t_{su(WRH)} must be observed. Depending on the user's transition times, this may require additional RAS low time (tw(RL)).



PARAMETER MEASUREMENT INFORMATION





VIH

VIL

VIH

VIL

VIH

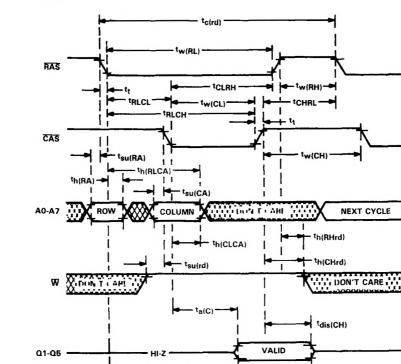
VIL

VIH

VIL

VOH

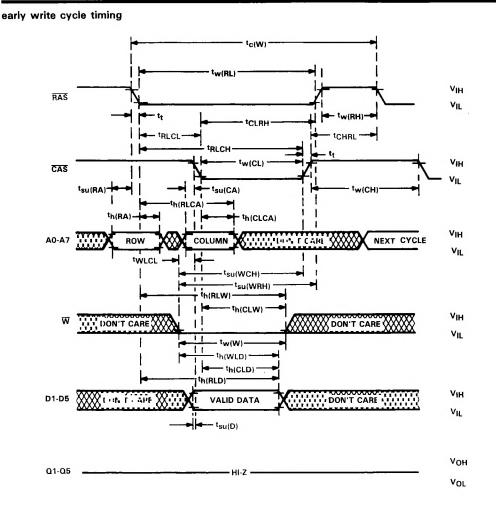
VOL



- ta(R)

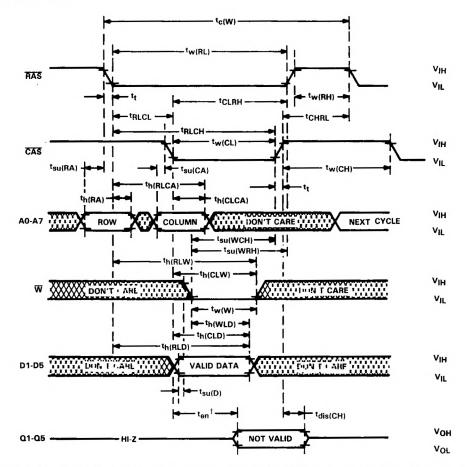
read cycle timing

Dynamic RAM Modules



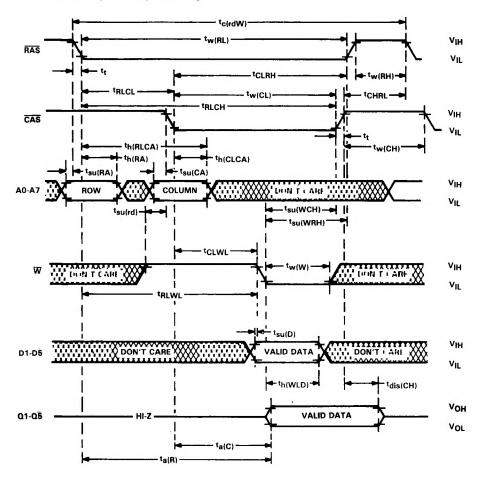


write cycle timing



[†] The enable time (t_{en}) for a write cycle is equal in duration to the access time from CAS (t_{a(C)}) in a read cycle; but the active levels at the output are invalid.



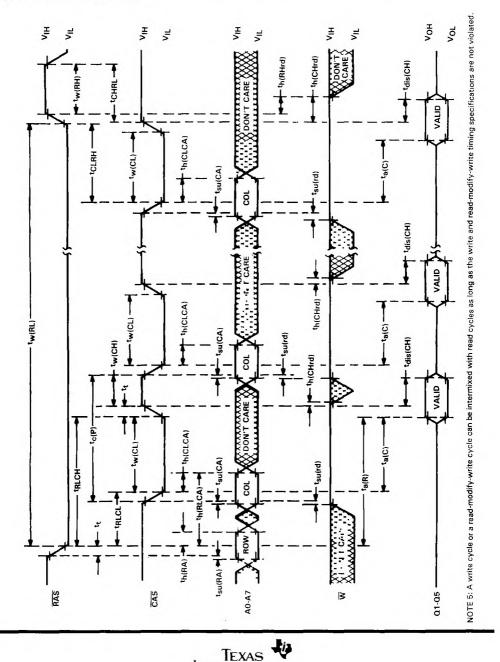


read-write/read-modify-write cycle timing



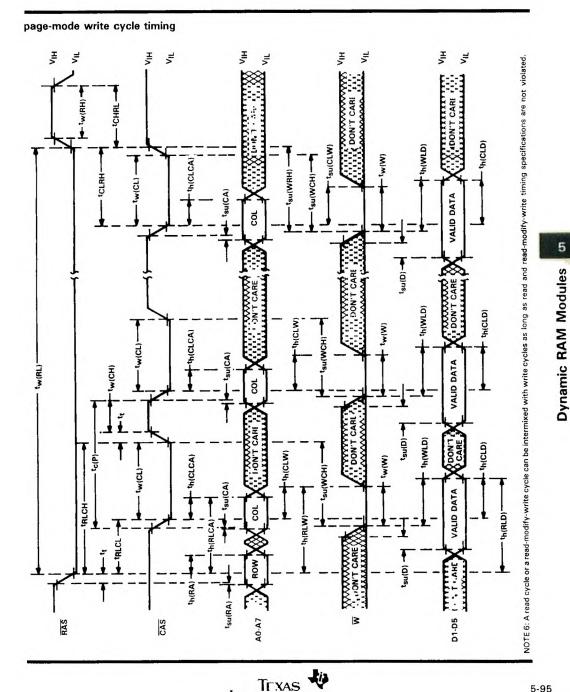
Dynamic RAM Modules

page-mode read cycle timing

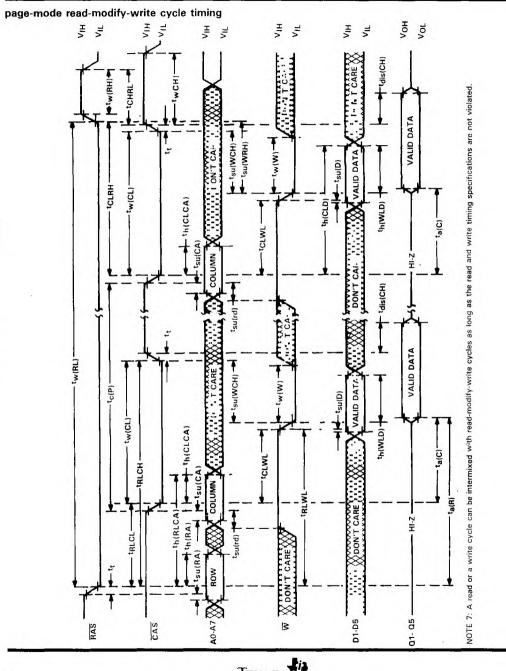


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Dynamic RAM Modules

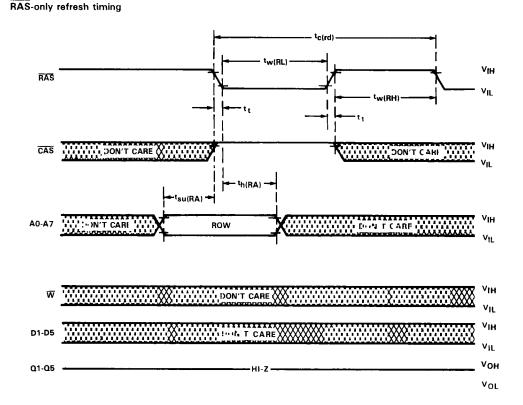


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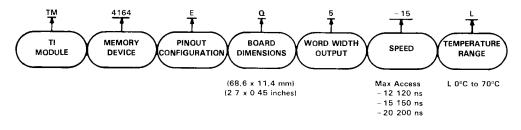


TEXAS TO INSTRUMENTS

Dynamic RAM Modules



TI single-in-line package nomenclature





NC. 👯

985

65,536 X 8 Organization TM4164FL8 TM4164FM8 Single 5-V Supply (10% Tolerance) (TOP VIEW) 30-Pin Single-in-Line Package (SIP) V_{DD} (1) **CAS** (2) Utilizes Eight 64K Dynamic RAMs in Plastic DQ1 (3) Chip Carrier A0 (4) Long Refresh Period . . . 4 ms (256 Cycles) A1 (5) DO2 (6) All Inputs, Outputs, Clocks Fully TTL A2 (7) Compatible A3 (8) **3-State Outputs** VSS (9) DQ3 (10) Performance Ranges: A4 (11) ACCESS ACCESS READ A5 (12) c TIME TIME OR DQ4 (13) ROW COLUMN WRITE A6 (14) ADDRESS ADDRESS CYCLE A7 (15) (MAX) (MAX) (MIN) TM4164__8-12 120 ns 75 ns 230 ns DQ5 (16) TM4164__8-15 150 ns 90 ns 260 ns NC‡ (17) = TM4164__8-20 200 ns 135 ns 326 ns NC (18) = Common CAS Control for Eight Common NC (19) **Data-In and Data-Out Lines** DQ6 (20) W (21) • Low Power Dissipation: VSS (22) ODED A TINO DQ7 (23) OTANDON NC (24) DQ8 (25)

(TYP)	ITYP)
1600 mW	140 mW
1400 mW	140 mW
1080 mW	140 mW
	(TYP) 1600 mW 1400 mW

The TM4164__8 series are 512K, dynamic random-access memory modules organized as 65,536 × 8-bits in a 30-pin single-in-line package comprising eight TMS4164FPL, 65, 536 × 1-bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with eight 0.1 µF decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board

Operating Free-Air Temperature . . . 0 °C to 70°C

L SINGLE IN-LINE PACKAGET . M SINGLE-IN-LINE PACKAGE

., NO

PIN NOMENCLATURE				
A0-A7	Address Inputs			
CAS	Column-Address Strobe			
DQ1-DQ8	Data In/Data Out			
NC	No Connection			
RAS	Row-Address Strobe			
V _{DD}	5-V Supply			
∨ss	Ground			
W	Write Enabla			

[‡]Pin 17 of the 256K x 8 SIP is memory address A8.

NC (26) RAS (27)

NC (28)

NC (29) (30)VDD

[†]TM4164FL8 package is shown.

spacing the TM4164...8 has a density of 8.5 devices per square inch (approximately 3.5X the density of of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

PRODUCTION DATA decuments centain infermation current as ef publication date. Preducts conform to specifications per the terms of Texas instruments standard warranty. Preduction processing does net necessarily include testing ef all parameters.

description



TM4164FL8, TM4164FM8 65,536 By 8-Bit Dynamic Ram Modules

The TM4164__8 features RAS access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation as low as 1080 mW typical operating and 140 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with RAS in order to retain data. CAS can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4164__8 is rated for operation from 0°C to 70°C.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations on each of the eight chips. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe (RAS). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobes. All addresses must be stable on or before the falling edges of RAS and CAS. RAS is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. CAS is used as a chip select activating the column decoder and the input and output buffers for M1-M8.

write enable (W)

The read or write mode is selected through the write-enable (\overline{W}) input. A logic high on the \overline{W} input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM4164___8 dictates the use of early write cycles to prevent contention on D and Q. When \overline{W} goes low prior to \overline{CAS} , the data outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ8)

Data is written during a write cycle. The falling edge of \overline{CAS} or \overline{W} strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, \overline{W} is brought low prior to \overline{CAS} and the data is strobed in by \overline{CAS} with setup and hold times referenced to this signal.

data out (DQ1-DQ8)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. In a read cycle the outputs go active after the access time interval $t_a(C)$ that begins with the negative transition of \overline{CAS} as long as $t_a(R)$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while \overline{CAS} is low; \overline{CAS} going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state, a necessity due to the common I/O feature of the TM4164_8.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless CAS is applied, the RAS-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with RAS causes all bits in each row to be refreshed. CAS can remain high (inactive) for this refresh sequence to conserve power.



page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on M1-M8, the row address and \overline{RAS} are applied to multiple modules. \overline{CAS} is then decoded to select the proper module.

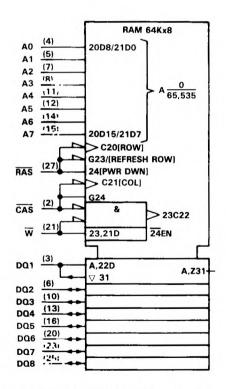
power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, \overline{RAS} must remain high for 100 μ s immediately prior to initialization. Initialization consists of performing eight \overline{RAS} cycles before proper device operation is achieved.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness Bypass capacitors: Multilayer ceramic Leads: Tin/lead solder coated over phosphor-bronze Contact area for socketable devices: Nickel plate and solder plate on top of copper

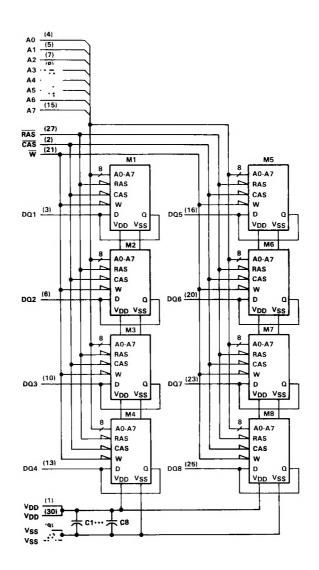
logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.



functional block diagram





Dynamic RAM Modules

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Voltage range on any pin except V _{DD} and data out (see Note 1) $\ldots \ldots \ldots \ldots -1.5$ V to 10 V
Voltage range on VDD supply and data out with respect to VSS
Short circuit output current for any output
Power dissipation
Operating free-air temperature range
Storage temperature range

[†]Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to ebsolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to VSS.

recommended operating conditions

			MIN	NOM	MAX	UNIT
VDD	Supply voltage	oply voltage		5	5.5	v
Vss	Supply voltage			0		V
		V _{DD} = 4.5 V	2.4		4.8	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
∨н	High-level input voltage	V _{DD} = 5.5 V	2.4		6	v
VIL	Low-level input voltage (see f	Low-level input voltage (see Notes 2 and 3)			0.8	V
TA	Operating free-air temperature		0		70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

Due to input protection circuitry, the applied voltage may begin to clamp at -0.6 V. Test conditions should comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

	DADAMETED		Т	M4164_	_8-12	TM41648-15			
PARAMETER		TEST CONDITIONS	MIN		мах	MIN	TYP	MAX	UNIT
Voн	High-level output voltage	IOH = -5 mA	2.4			2.4			V
VOL	Low-level output voltage	I _{OL} = 4.2 mA			0.4			0.4	V
 lį	Input current (leakage)	$V_I = 0 V$ to 5.8 V, $V_{DD} = 5 V$, All other pins = 0 V			± 10			± 10	μΑ
ю	Output current (leakage)	$V_D = 0.4 V$ to 5.5 V, $V_{DD} = 5 V$, \overline{CAS} high			± 10			± 10	μΑ
^I DD1 [‡]	Average operating current during read or write cycle	t _C = minimum cycłe, All outputs open		320	384		280	360	mA
	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open		28	40		28	40	mA
^I DD3 [‡]	Average refresh current	t _C = minimum cycle, CAS high and RAS cycling, All outputs open		224	320		200	296	mA
IDD4 [‡]	Average page-mode current	$t_{C(P)} = minimum cycle,RAS low and CAS cycling,All outputs open$		224	320		200	296	mA

[†] All typical values are at $T_A = 25$ °C and nominal supply voltages.

[‡] IDD1-IDD4 are measured with M1-M8 in the same mode (i.e., operating, standby, refresh or page mode).



	DADAMETER	TEAT COMPLETIONS	TM41648-20				
-	PARAMETER	TEST CONDITIONS	MIN TYP [†]		MAX	UNIT	
VOH	High-level output voltage	$I_{OH} = -5 \text{ mA}$	2.4			v	
VOL	Low-level output voltage	I _{OL} = 4.2 mA			0.4	V	
h	Input current (leakage)	$V_I = 0 V$ to 5.8 V, $V_{DD} = 5 V$, All other pins = 0 V			±10	μA	
0	Output current (leakage)	V _O = 0.4 V to 5.5 V, V _{DD} = 5 V, CAS high			±10	μΑ	
too1 [‡]	Average operating current during read or write cycle	t _C = minimum cycle, All outputs open		216	296	mA	
DD2 [‡]	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open		28	40	mA	
[‡] 500	Average refresh current	t _c = minimum cycle, CAS high and RAS cycling, All outputs open		160	256	mA	
	Average page-mode current	t _{c(P)} = minimum cycle, RAS low and CAS cycling, All outputs open		160	256	mA	

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

[†] All typical values are at T_A = 25 °C and nominal supply voltages.

[‡] IDD1-IDD4 are measured with M1-M8 in the same mode (i.e., operating, standby, refresh or page mode).

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MAX	UNIT
Ci(A)	Input capacitance, address inputs	40	pF
Ci(DQ)	Input capacitance, Lite nputs	11	pF
Ci(RAS)	Input capacitance, TE nput	64	pF
Ci(W)	Input capacitance, W input	64	pF
Ci(CAS)	Input capacitance, CAS input	64	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER			ALT.	TM4164	8-12	TM41648-15		
		TEST CONDITIONS	SYMBOL	SYMBOL MIN		MIN	MAX	UNIT
t _a (C)	Access time from CAS	$C_L = 100 \text{ pF},$ Load = 2 Series 74 TTL gates	^t CAC		75		90	ns
^t a(R)	Access time from RAS	tRLCL = MAX, Load = 2 Series 74 TTL gates	^t RAC		120		150	ns
^t dis(CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL gates	tOFF	o	40	0	40	ns



switching characteristics over recommended supply voltage range and operating free-air temperature range

_			ALT.	TM4164	8-20	1.00.07
	PARAMETER	TEST CONDITIONS	SYMBOL	MIN MAX		UNIT
^t a(C)	Access time from CAS	CL = 100 pF, Load = 2 Series 74 TTL gates	tCAC		135	ns
^t a(R)	Access time from RAS	t _{RLCL} = MAX, Load = 2 Series 74 TTL gates	^t RAC		200	ns
^t dis(CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL gates	toff	0	50	ns



		ALT. SYMBOL	TM41648-12		TM41648-15		
			MIN	MAX	MIN	MAX	UNIT
tc(P)	Page-mode cycle time	tPC	130		160		ns
tc(rd)	Read cycle time [†]	tRC	230		260		ns
tc(W)	Write cycle time	twc	230	1	260	1.1	ns
tw(CH)	Pulse duration, CAS high (precharge time) [‡]	tCP	50		50		ns
tw(CL)	Pulse duration, CAS low	tCAS	75	10,000	90	10,000	ns
tw(RH)	Pulse duration, RAS high (precharge time)	tRP	80		100		ns
tw(RL)	Pulse duration, RAS low	^t RAS	120	10,000	150	10,000	ns
tw(W)	Write pulse duration	tWP	40		45		ns
tt	Transition times (rise and fall) for RAS and CAS †	tT	10	50	10	50	ns
tsu(CA)	Column-address setup time	tASC	0	4.55	0		ns
t _{su} (RA)	Row-address setup time	tASR	0		0		ns
t _{su(D)}	Data setup time	tDS	0		0	1	ns
t _{su(rd)}	Read-command setup time	tRCS	0		0		ns
t _{su} (WCH)	Write-command setup time before CAS high	tCWL	50	1.00	50	1.2.1.1	ns
t _{su} (WRH)	Write-command setup time before RAS high	tRWL	50		50		ns
th(CLCA)	Column-address hold time after CAS low	^t CAH	40		45		ns
th(RA)	Row-address hold time	^t RAH	20		25		ns
th(RLCA)	Column-address hold time after RAS low	tAR	85		100		ns
th(CLD)	Data hold time after CAS low	†DHC	45		50		ns
th(RLD)	Data hold time after I ow	^t DHR	90		100		ns
th(CHrd)	Read-command hold turne after CAS high	^t RCH	0		0		ns
th(RHrd)	Read-command hold time after RAS high	^t RRH	5		5		ns
th(CLW)	Write-command hold time after CAS low	tWCH	45		50		ns
th(RLW)	Write-command hold time after RAS low	tWCR	90	10	100		ns
TRLCH	Delay time, RAS low to CAS high	tCSH	120		150		ns
tCHRL	Delay time, CAS high to RAS low	tCRP	0		0		ns
tCLRH	Delay time, CAS low to RAS high	tRSH	60		100		ns
1.2.2.1	Delay, time, RAS low to CAS low	^t RCD	25	45	30	60	ns
^t RLCL	(maximum value specified only						
	to guarantee access time)						
tWLCL	Delay time, W low to CAS	twcs	0		0	1	
	low (early write cycle)				0		ns
trf	Refresh time interval	tREF		4		4	ms

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, VIL max and VIH min must be met at the 10% and 90% points.

[†]All cycle times assume $t_t = 5$ ns. The specified $t_t = is$ due to testing limitations. Transition times may be as little as 3 ns in system use. [‡]Page mode only.



		ALT.	ALT. TM41648-20	
_		SYMBOL	MIN MAX	UNIT
t _{c(P)}	Page-mode cycle time	tPC	206	ns
tc(rd)	Read cycle time [†]	tRC	326	ns
tc(W)	Write cycle time	tWC	326	ns
tw(CH)	Pulse duration, CAS high (precharge time) [‡]	tCP	80	ns
tw(CL)	Pulse duration, CAS low	tCAS	135 10,000	ns
tw(RH)	Pulse duration, RAS high (precharge time)	tRP	120	ns
tw(RL)	Pulse duration, RAS low	tRAS	200 10,000	ns
tw(W)	Write pulse duration	twp	55	ns
tt	Transition times (rise and fall) for RAS and CAS [†]	tŢ	10 50	ns
t _{su(CA)}	Column-address setup time	tASC	0	ns
t _{su(RA)}	Row-address setup time	tASR	0	ns
t _{su(D)}	Data setup time	tDS	0	ns
t _{su(rd)}	Read-command setup time	tRCS	0	ns
t _{su} (WCH)	Write-command setup time before CAS high	tCWL	60	ns
t _{su} (WRH)	Write-command setup time before RAS high	tRWL	60	ns
th(CLCA)	Column-address hold time after CAS low	^t CAH	55	ns
th(RA)	Row-address hold time	tRAH	30	ns
th(RLCA)	Column-address hold time after RAS low	tAR	125	ns
th(CLD)	Data hold time after CAS low	^t DHC	60	ns
th(RLD)	Data hold time after RAS low	tDHR	145	ns
th(CHrd)	Read-command hold time after CAS high	tRCH	0	ns
th(RHrd)	Read-command hold time after RAS high	tRRH	5	ns
th(CLW)	Write-command hold time after CAS low	tWCH	60	ns
th(RLW)	Write-command hold time after RAS low	tWCR	145	ns
tRLCH	Delay time, RAS low to CAS high	tCSH	200	ns
^t CHRL	Delay time, CAS high to RAS low	tCRP	0	ns
tCLRH	Delay time, CAS low to RAS high	tRSH	135	ns
^t RLCL	Delay, time, RAS low to CAS low			ns
	(maximum value specified only	^t RCD	35 65	
	to guarantee access time)			
tWLCL	Delay time, W low to CAS	1		ns
	low (early write cycle)	twcs	0	
t _{rf}	Refresh time interval	tREF	4	ms

timing requirements over recommended supply voltage range and operating free-air temperature range

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, VIL max and VIH min must be met at the 10% and 90% points.

[†]All cycle times assume $t_t = 5$ ns. The specified $t_t = i$ s due to testing limitations. Transition times may be as little as 3 ns in system use. [‡]Page mode only.



Dynamic RAM Modules on

PARAMETER MEASUREMENT INFORMATION

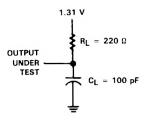
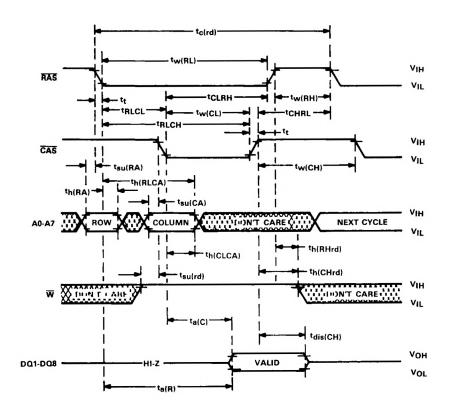


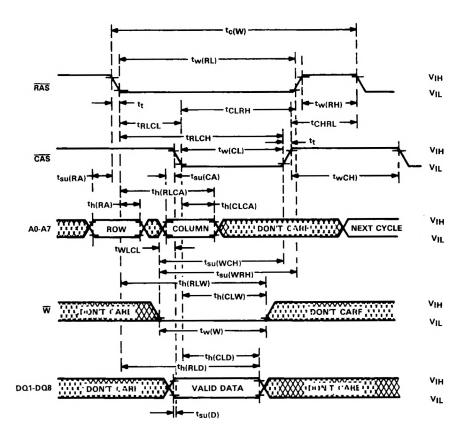
FIGURE 1. LOAD CIRCUIT





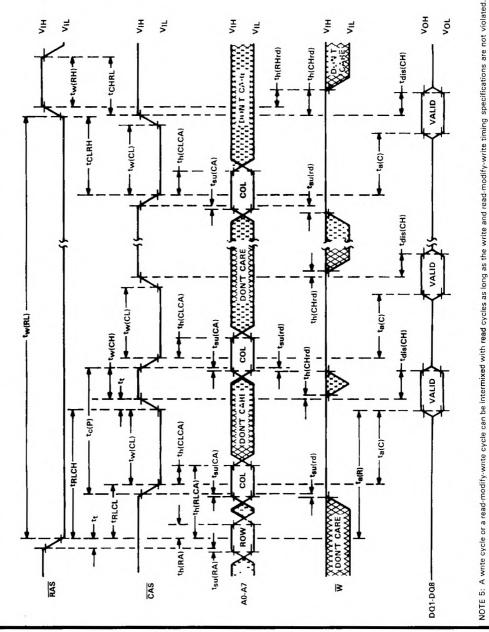


early write cycle timing





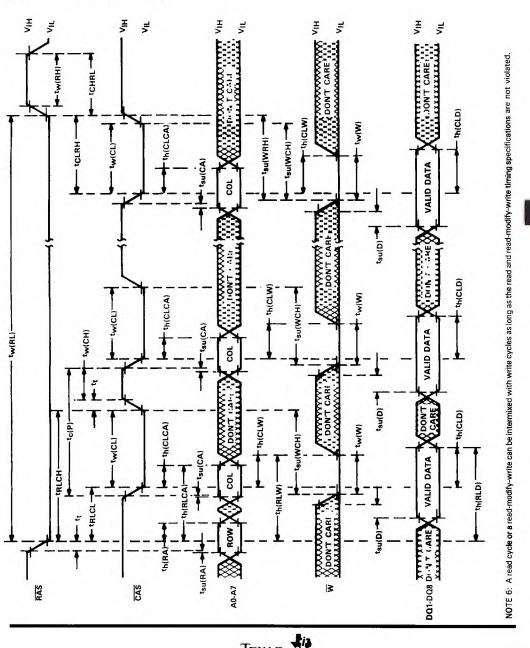
page-mode read cycle timing





Dynamic RAM Modules

page-mode write cycle timing

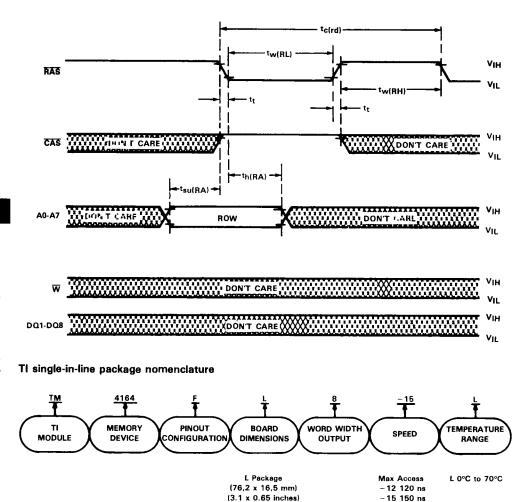


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5

Dynamic RAM Modules

RAS-only refresh timing



Dynamic RAM Modules

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5-112



M Package

(88,9 x 15,24 mm) (3.5 x 0.60 inchas) - 20 200 ns

SEPTEMBER 9185 - REVISED NOVEMBER 1985

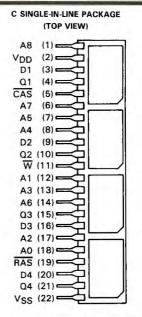
- 262,144 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- 22-Pin Single-in-Line Package (SIP)
- Utilizes Four 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

	ACCESS	ACCESS	READ	READ- MODIFY-
	ROW	COLUMN	WRITE	WRITE
	ADDRESS	ADDRESS	CYCLE	CYCLE
	(MAX)	(MAX)	(MIN)	(MIN)
TM425_EC4-12	120 ns	60 ns	230 ns	275 ns
TM425_EC4-15	150 ns	75 ns	260 ns	305 ns
TM425_EC4-20	200 ns	100 ns	330 ns	370 ns

- Common CAS Control with Separate Data Input and Output Lines
- Operating Free-Air Temperature . . . 0 °C to 70 °C
- Downward Compatible with 64K X 4 Singlein-Line Package (TM4164EC4)

description

The TM425_EC4 is a 1024K, dynamic randomaccess memory module organized as 262,144 × 4 bits in a 22-pin single-in-line package comprising four TMS425_FML, 262,144 × 1 bit dynamic RAM's in 18-lead plastic chip carriers



	PIN NOMENCLATURE
A0-A8	Address Inputs
CAS	Column-Address Strobe
D1-D4	Data Inputs
NC	No Connection
01-04	Data Outputs
RAS	Row-Address Strobe
VDD	5-V Supply
VSS	Ground
$\overline{\mathbf{w}}$	Write Enable

mounted on top of a substrate together with decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM425_EC4 has a density of ten devices per square inch (approximately 4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

The TM425_EC4 features RAS access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation as low as 900 mW typical operating and 50 mW typical standby.

Refresh period is extended to $4 \text{ m}(1) \cdots$ conds, and during this period each of the 256 rows must be strobed with $\overrightarrow{\text{RAS}}$ in order to retain data. $\overrightarrow{::::S}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM425_EC4 is rated for operation from 0°C to 70°C.

TM4256EC4, TM4257EC4 262,144 by 4-bit dynamic ram modules

operation

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations on each of the four chips. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe (RAS). Then the nine column-address bits are set up on pins A0 through A8 and latched ont<u>o the</u> chip by the column-address strobe. All addresses must be stable on or before the falling edges of RAS and CAS. RAS is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. CAS is used as a chip select activating the column decoder and the input and output buffers.

write enable (W)

The read or write mode is selected through the write-enable (\overline{W}) input. A logic high on the \overline{W} input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. When \overline{W} goes low prior to \overline{CAS} , the data outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D1-D4)

Data is written during a write cycle. The falling edge of \overline{CAS} or \overline{W} strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, \overline{W} is brought low prior to \overline{CAS} and the data is strobed in by \overline{CAS} with setup and hold times referenced to this signal.

data out (Q1-Q4)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state until CAS is brought low. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of CAS as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while CAS is low; CAS going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless \overline{CAS} is applied, the \overline{RAS} -only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with \overline{RAS} causes all bits in each row to be refreshed. \overline{CAS} can remain high (inactive) for this refresh sequence to conserve power.

CAS-before-RAS refresh

The CAS-before-RAS refresh is utilized by bringing CAS low earlier than RAS (see parameter t_{CLRL}) and holding it low after RAS falls (see p $\cdots \cdot$ ter t_{RLCHR}). For successive CAS-before-RAS refresh cycles, CAS can remain low while cycling $\cdots \cdot \cdot$ The external address is ignored and the refresh address is generated internally.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by hole a CAS at VIL after a read operation and cycling RAS after a specified precharge period, similar to a CAS only refresh cycle. The external address is also ignored during the hidden refresh cycles.

page mode (TM4256EC4)

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated.



nibble mode (TM4257EC4)

Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. The next sequential nibble bits can be read or written by cycling \overrightarrow{CAS} while \overrightarrow{RAS} remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Column A8 and row A8 (CA8, RA8) provide the two binary bits for initial selection of the nibble addresses. Thereafter, the falling edge of \overrightarrow{CAS} will access the next bit of the circular 4-bit nibble in the following sequence:



In nibble-mode, all normal memory operations (read, write, or ready-modify-write) may be performed in any desired combination.

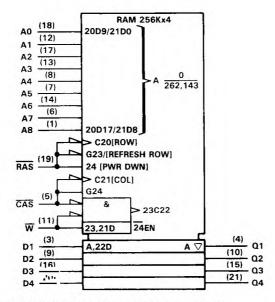
power up

To achieve proper device operation, an initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness Bypass capacitors: Multilayer ceramic Leads: Tin/lead solder coated over phosphor-bronze

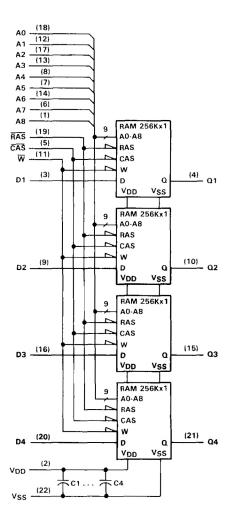
logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



functional block diagram





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Voltage range for any pin except VDD and data out (see Note 1)	1.5 V to 10 V
Voltage range on VDD supply and data out with respect to VSS	-1 V to 7 V
Short circuit output current for any output	50 mA
Power dissipation	4 W
Operating free-air temperature range	
Storage temperature range6	5°C to 150°C

[†] Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to VSS.

recommended operating conditions

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	4.5	5	5.5	V
VSS	Supply voltage		0		٧
VIH	High-level input voltage	2.4		6.5	V
VIL	Low-level input voltage (see Note 2)	-1		0.8	V
TA	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

	BADAMETER	TEST	TM	425_EC	4-12	TM425_EC4-15			
	PARAMETER	CONDITIONS	MIN	TYPT	MAX	MIN	TYP [†]	MAX	UNIT
VOH	High-level output voltage	IOH = -5 mA	2.4		VDD	2.4		VDD	V
VOL	Low-level output voltage	IOL = 4.2 mA	0		0.4	0		0.4	V
ц	Input current (leakage)	$V_I = 0 V$ to 6.5 V, $V_{DD} = 5 V$, All other pins = 0 V	18		± 10			±10	μΑ
10	Output current (leakage)	$V_O = 0.4 V$ to 5.5 V, $V_{DD} = 5 V$, CAS high			± 10			± 10	μA
IDD1	Average operating current during read or write cycle	t _C = minimum cycle, All outputs open	Ċ.	260	312		220	272	mA
IDD2	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open		10	18		10	18	mA
IDD3	Average refresh current	t _c = minimum cycle, CAS high and RAS cycling, All outputs open		180	240		160	212	mA
IDD4	Average page-mode current	$t_{C(P)} = minimum cycle,RAS low and CAS cycling,All outputs open$		140	192		120	172	mA
IDD5	Average nibble-mode current	 minimum cycle, ow and CAS cycling, All outputs open 		128	176		108	156	mA

[†]All typical values are at $T_A = 25$ °C and nominal supply voltages.



	PARAMETER	TEST	TM425_1	C4-20	UNIT
	PANAMETER	CONDITIONS	MIN TYP	MAX	
VOH	High-level output voltage	1 _{0H} = -5 mA	2.4	VDD	V
VOL	Low-level output voltage	IOL = 4.2 mA	0	0.4	V
4	Input current (leakage)	$V_1 = 0 V$ to 6.5 V, $V_{DD} = 5 V$, All other pins = 0 V		±10	μA
10	Output current (leakage)	V _O = 0.4 V to 5.5 V, V _{DD} = 5 V, CAS high		± 10	μA
IDD1	Average operating current during read or write cycle	t _c = minimum cycle, All outputs open	18	232	mA
IDD2	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open	1	0 18	mA
IDD3	Average refresh current	t _C = minimum cycle, CAS high and RAS cycling, All outputs open	14	0 192	mA
IDD4	Average page-mode current	t _{c(P)} = minimum cycle, RAS low and CAS cycling, All outputs open	10	0 140	mA
DD5	Average nibble-mode current	= minimum cycle, =.:. ⁻ ow and CAS cycling, All outputs open	8	3 128	mA

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

[†]All typical values are at $T_A = 25$ °C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, $f\,=\,1\,\,\text{MHz}$

	PARAMETER	MIN MAX	UNIT
Ci(A)	Input capacitance, address inputs	28	pF
Ci(D)	Input capacitance, : · · nputs	28	pF
Ci(RAS)	Input capacitance, nput	32	pF
Ci(W)	Input capacitance, W input	32	pF
Ci(CAS)	Input capacitance, CAS input	32	pF
Co(Q)	Output capacitance, data outputs	40	pF
Co(VDD)	Decoupling capacitance	0.4	μF

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switching characteristics over recommended supply voltage range and operating free-air temperature range

				TM425_EC4-12		TM425_EC4-15		
	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	MIN	MAX	UNIT
ta(C)	Access time from CAS	$C_L = 100 \text{ pF},$ Load = 2 Series 74 TTL gates	^t CAC		60		75	ns
t _a (R)	Access time from RAS	t _{RLCL} = MAX, Load = 2 Series 74 TTL gates	^t RAC		120		150	ns
^t dis(CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL gates	tOFF	0	35	0	35	ns

		TECT CONDITIONS	ALT. SYMBOL	r. TM425_EC4		UNIT
	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNIT
t _{a(C)}	Access time from CAS	C _L = 100 pF, Load = 2 Series 74 TTL gates	^t CAC		100	ns
t _{a(R)}	Access time from RAS	t _{RLCL} = MAX, Load = 2 Series 74 TTL gates	^t RAC		200	ns
^t dis(CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL gates	tOFF	0	35	ns



		ALT.	TM425_EC4-12	
		SYMBOL	MIN MAX	UNIT
tc(P)	Page-mode cycle time (read or write cycle)	tPC	1.00	ns
tc(PM)	Page-mode cycle time (read-modify-write cycle)	^t PCM	165	ns
tc(rd)	Read cycle time [†]	tRC	230	ns
tc(W)	Write cycle time	tWC	230	ns
tc(rdW)	Read-write/read-modify-write cycle time	tRWC	275	ns
tw(CH)P	Pulse duration, CAS high (page mode)	tCP	50	ns
tw(CH)	Pulse duration, CAS high (non-page mode)	1CPN	25	ns
tw(CL)	Pulse duration, CAS low [‡]	tCAS	60 10,000	ns
tw(RH)	Pulse duration, RAS high	tRP	100	ns
tw(RL)	Pulse duration, RAS low [§]	tRAS	120 10,000	ns
tw(W)	Write pulse duration	twp	40	ns
tt	Transition times (rise and fall) for RAS and CAS	tŢ	3 50	ns
t _{su(CA)}	Column-address setup time	tASC	0	ns
tsu(RA)	Row-address setup time	tASR	0	ns
t _{su(D)}	Data setup time	tDS	0	ns
tsu(rd)	Read-command setup time	tRCS	0	ns
t _{su} (WCL)	Early write-command setup time before CAS low	twcs	. 0	лѕ
tsu(WCH)	Write-command setup time before CAS high	tCWL	40	ns
t _{su} (WRH)	Write-command setup time before RAS high	tRWL	40	ns
th(CLCA)	Column-address hold time after CAS low	tCAH	20	ns
th(RA)	Row-address hold time	tRAH	15	ns
th(RLCA)	Column-address hold · · after RAS low	tAR	80	ns
th(CLD)	Data hold time after ow	^t DHC	35	ns
th(RLD)	Data hold time after RAS low	^t DHR	95	ns
th(WLD)	Data hold time after W low	tDHW	35	ns
th(CHrd)	Read-command hold time after CAS high	tRCH	0	ns
th(RHrd)	Read-command hold time after RAS high	^t RRH	10	ns
th(CLW)	Write-command hold time after CAS low	tWCH	35	ns
th(RLW)	Write-command hold time after RAS low	tWCR	95	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

Continued next page.

NOTE 3: Timing measurements are referenced to VIL max and VIH min.

[†]All cycle times assume $t_t = 5$ ns.

[‡]In a read-modify-write cycle, t_{CLWL} and t_{su(WCH)} must be observed. Depending on the user's transition times, this may require additional CAS low time t_{w(CL)}). This applies to page-mode read-modify-write also.

In a read-modify-write cycle, tRLWL and tsu(WRH) must be observed. Depending on the user's transition times, this may require additional RAS low time (tw(RL)).



		ALT.	TMS425_EC4-12	
		SYMBOL	MIN MAX	UNIT
RLCH	Delay time, RAS low to CAS high	tCSH	120	ns
CHRL	Delay time, CAS high to RAS low	tCRP	0	ns
CLRH	Delay time, CAS low to RAS high	trsh	60	ns
RLCHR	Delay time, RAS low to CAS high	^t CHR	25	ns
CLRL	Delay time, CAS low to RAS low	tCSR	25	ns
RHCL	Delay time, RAS high to CAS low	tRPC	20	ns
CLWL	Delay time, CAS low to W low (read-modify-write cycle only)	tCWD	60	ns
^t rlcl	Delay time, RAS low to CAS low (maximum value specified only to guarantee access time)	trcd	25 60	ns
^t RLWL	Delay time, RAS low to W low (read-modify-write cycle only)	^t RWD	120	ns
t _{rf}	Refresh time interval	tREF	4	ms

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

Continued next page.

NOTE 3: Timing measurements are referenced to VIL max and VIH min.

ICAS-before-RAS refresh only.



timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT.	TM425_EC4-1	5 TM425_EC4-20	UNIT
	and the state of the state of the	SYMBOL	MIN MA	X MIN MAX	UNIT
tc(P)	Page-mode cycle time (read or write cycle)	tPC	145	190	ns
tc(PM)	Page-mode cycle time (read-modify-write cycle)	^t PCM	190	245	ns
tc(rd)	Read cycle time [†]	tRC	260	330	ns
t _{c(W)}	Write cycle time	tWC	260	330	ns
tc(rdW)	Read-write/read-modify-write cycle time	tRWC	305	370	ns
tw(CH)P	Pulse duration, CAS high (page mode)	tCP	60	80	ns
tw(CH)	Pulse duration, CAS high (non-page mode)	^t CPN	25	30	ns
tw(CL)	Pulse duration, CAS low [‡]	tCAS	75 10,00	0 100 10,000	ns
tw(RH)	Pulse duration, RAS high	tRP	100	120	ns
tw(RL)	Pulse duration, RAS low [§]	tRAS	150 10,00	0 200 10,000	ns
tw(W)	Write pulse duration	twp	45	55	ns
tt	Transition times (rise and fall) for RAS and CAS	tŢ	3 5	0 3 50	ns
t _{su(CA)}	Column-address setup time	tASC	0	0	ns
tsu(RA)	Row-address setup time	tASR	0	0	ns
t _{su(D)}	Data setup time	tDS	0	0	ns
t _{su(rd)}	Read-command setup time	tRCS	0	0	ns
tsu(WCL)	Early write-command setup time before CAS low	twcs	0	0	ns
tsu(WCH)	Write-command setup time before CAS high	tCWL	45	60	ns
t _{su} (WRH)	Write-command setup time before RAS high	tRWL	45	60	ns
th(CLCA)	Column-address hold time after CAS low	^t CAH	25	30	ns
th(RA)	Row-address hold time	tRAH	15	20	ns
th(RLCA)	Column-address hold time after RAS low	tAR	100	130	ns
th(CLD)	Data hold time after CAS low	^t DHC	45	55	ns
th(RLD)	Data hold time after RAS low	^t DHR	120	155	ns
th(WLD)	Data hold time after W low	tohw	45	55	ns
th(CHrd)	Read-command hold time after CAS high	^t RCH	0	0	ns
th(RHrd)	Read-command hold time after RAS high	tRRH	10	15	ns
th(CLW)	Write-command hold time after CAS low	tWCH	45	55	ns
th(RLW)	Write-command hold time after RAS low	tWCR	120	. 155	ns

Continued next page.

NOTE 3: Timing measurements are referenced to VIL max and VIH min.

[†]All cycle times assume $t_t = 5$ ns.

⁺In a read-modify-write cycle, t_{CLWL} and t_{su(WCH)} must be observed. Depending on the user's transition times, this may require additional CAS low time t_{w(CL)}). This applies to page-mode read-modify-write also.

[§]In a read-modify-write cycle, t_{RLWL} and t_{su(WRH)} must be observed. Depending on the user's transition times, this may require additional RAS low time (t_{w(RL)}).



		ALT.	TM425_	EC4-15	TM425_	EC4-20	
		SYMBOL	MIN	MAX	MIN	MAX	UNIT
TRLCH	Delay time, RAS low to CAS high	tCSH	150		200		ns
tCHRL	Delay time, CAS high to RAS low	tCRP	0		0		ns
^t CLRH	Delay time, CAS low to RAS high	tRSH	75		100		ns
TRLCHR	Delay time, RAS low to CAS high	^t CHR	30		35		ns
tCLRL	Delay time, CAS low to RAS low 1	tCSR	30		35		ns
TRHCL	Delay time, RAS high to CAS low	tRPC	20	The second	25		ns
tCLWL	Delay time, \overline{CAS} low to \overline{W} low (read-modify-write cycle only)	tCWD	70		90		ns
^t RLCL	Delay time, RAS low to CAS low (maximum value specified only to guarantee access time)	tRCD	25	75	30	100	ns
^t RLWL	Delay time, RAS low to W low (read-modify-write cycle only)	tRWD	145		190		ns
t _{rf}	Refresh time interval	tREF		4		4	ms

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min. $\{\overline{CAS}\)$ -before- \overline{RAS} refresh only.

NIBBLE-MODE CYCLE

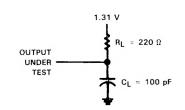
switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT.	TM425	7EC4-12	TM425	7EC4-15	TM425	7EC4-20	UNIT
		SYMBOL	MIN MAX		MIN MAX		MIN MAX		UNIT
ta(CN)	Nibble-mode access time from CAS	^t NCAC		30		40		50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM425	MAX	TM425 MIN	7EC4-15 MAX	TM4257	EC4-20 MAX	UNIT
t _{c(N)}	Nibble-mode cycle time	tNC	60		75		90		
c(rdWN)	Nibble-mode read-modify-write cycle time	^t NRMW	85		105		130		
CLRHN	Nibble-mode delay time, CAS low to RAS high	^t NRSH	30		40		50		
CLWLN	Nibble-mode delay time, CAS to W delay	tNCWD	25		30		40		
tw(CLN)	Nibble-mode pulse duration, CAS low	^t NCAS	30		40		50		ns
w(CHN)	Nibble-mode pulse duration, CAS high	^t NCP	20		25		30		
tw(CRWN)	Nibble-mode read-modify-write pulse duration, CAS low	^t NCRW	55		70		90		
t _{su} (WCHN)	Nibble-mode write command setup time before CAS high	^t NCWL	25		35		45		

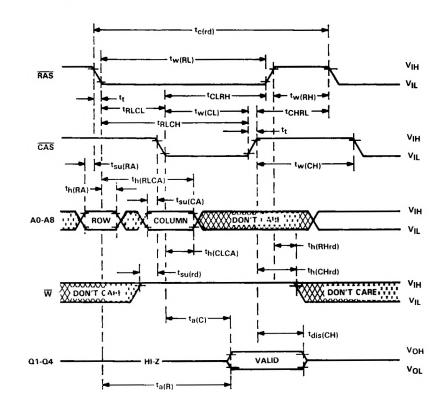




PARAMETER MEASUREMENT INFORMATION

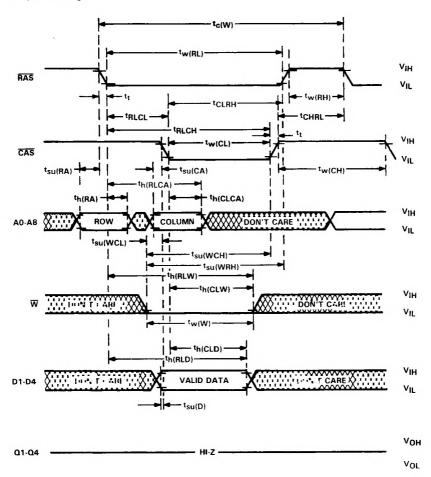






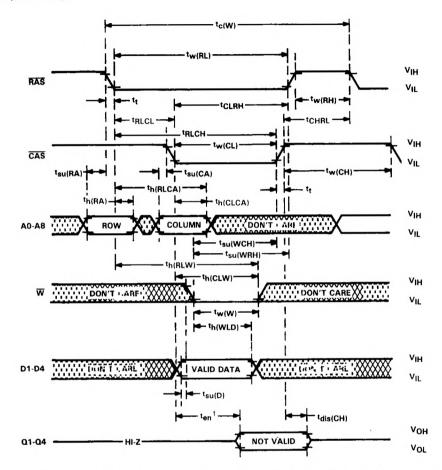


early write cycle timing





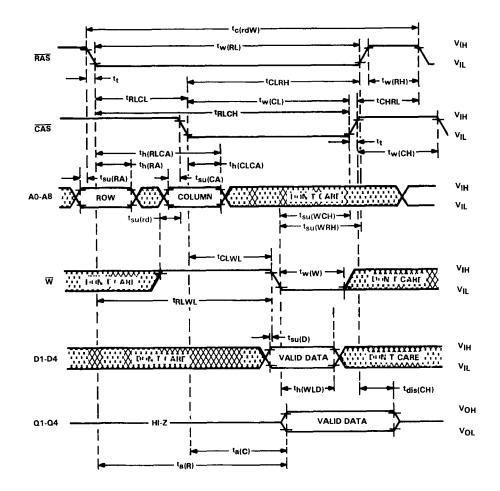
write cycle timing



[†]The enable time (t_{en}) for a write cycle is equal in duration to the access time from CAS (t_{a(C)}) in a read cycle; but the active levels at the output are invalid.



Dynamic RAM Modules

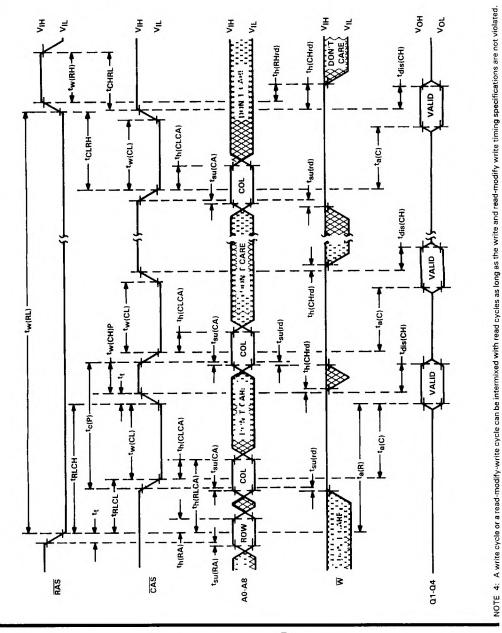


read-write/read-modify-write cycle timing



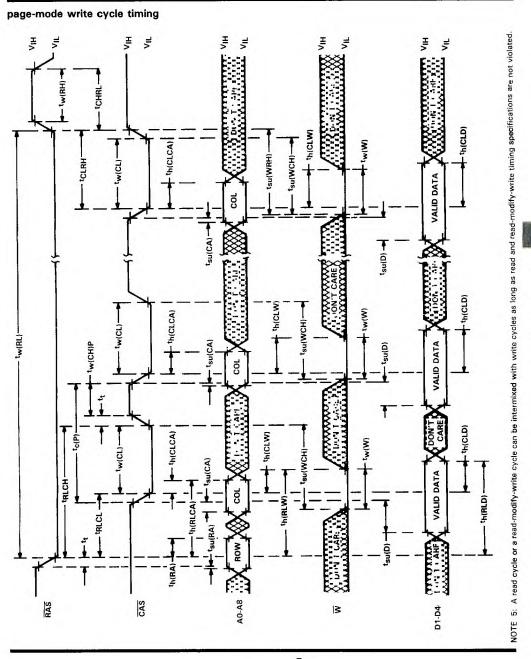
TM4256EC4 262,144 BY 4-BIT DYNAMIC RAM MODULE

page-mode read cycle timing





Dynamic RAM Modules



TM4256EC4 262,144 BY 4-BIT DYNAMIC RAM MODULE

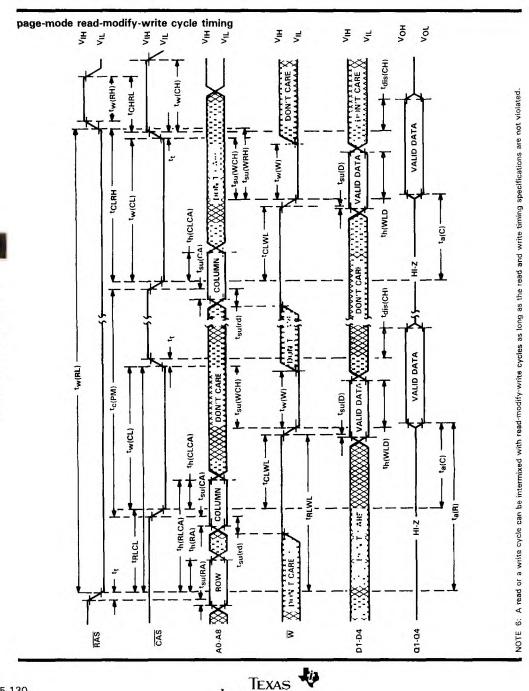
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Dynamic RAM Modules

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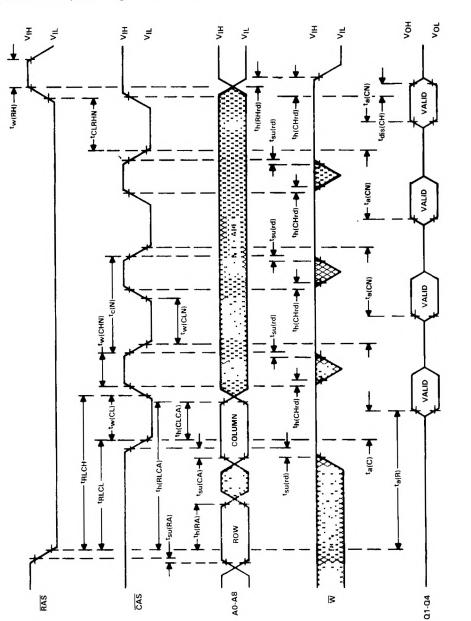
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TM4256EC4 262,144 BY 4-BIT DYNAMIC RAM MODULE

Dynamic RAM Modules



TM4257EC4 262,144 BY 4-BIT DYNAMIC RAM MODULE

nibble-mode read cycle timing

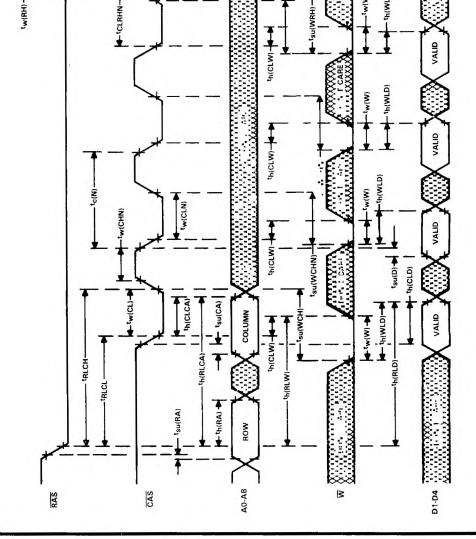
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Dynamic RAM Modules

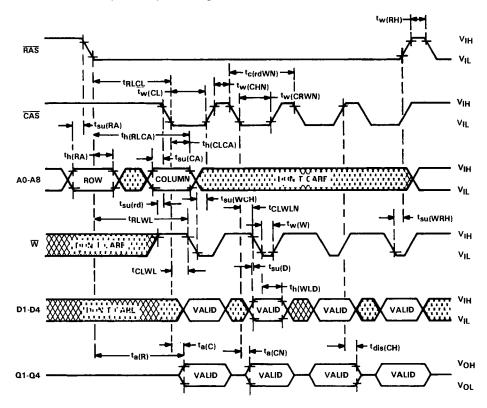
TM4257EC4 262,144 BY 4-BIT DYNAMIC RAM MODULE nibble-mode write cycle timing HI, ۲IH Ť Ę **VIH** Ϋ́Γ HIN ZEL N ľ + tsu(WCHN) tw(RH) (MLD) -tw(W) -tcLRHN-HU(MRH) -

ž

Dynamic RAM Modules



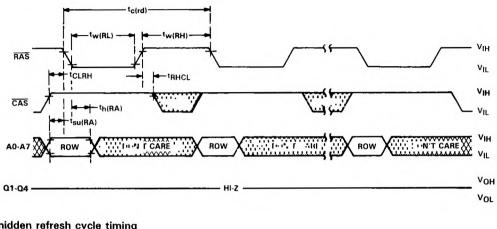


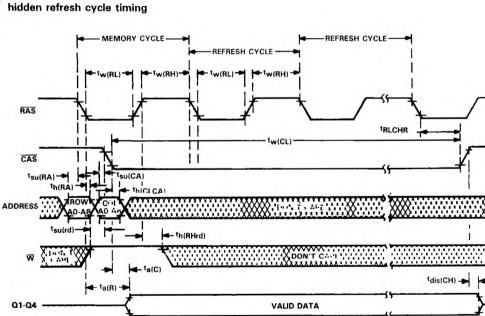


nibble-mode read-modify-write-cycle timing









VIH

VIL

VIH

VIL

VIH

VIL

VIH

VOH

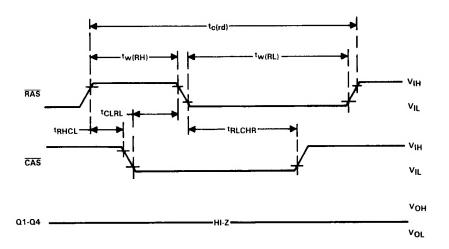
VOL

VIL

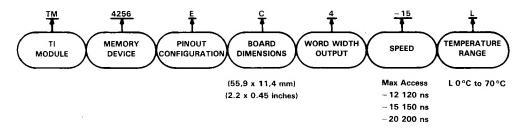
5

Dynamic RAM Modules





TI single-in-line package nomenclature





Dynamic RAM Modules

SEPTEMBER 1985 - REVISED NOVEMBER 1985

- 262,144 X 9 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP) — Pinned Module for Through-Hole Insertion (TM425_EL9)
 - -Leadless Module for Use with Sockets (TM425_GU9)
- Utilizes Nine 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

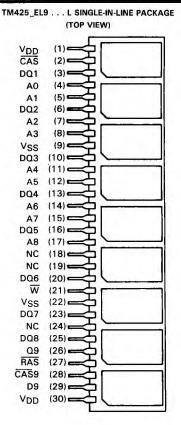
		ACCESS	ACCESS	READ
		TIME	TIME	OR
		ROW	COLUMN	WRITE
		ADDRESS	ADDRESS	CYCLE
		(MAX)	(MAX)	(MIN)
TM425	9-12	120 ns	60 ns	230 ns
TM425	9-15	150 ns	75 ns	260 ns
TM425	_9-20	200 ns	100 ns	330 ns

- Common CAS Control for Eight Common Data-In and Data-Out Lines
- Separate CAS Control for One Separate Pair of Data-In and Data-Out Lines
- Low Power Dissipation
- Operating Free-Air Temperature . . . 0 °C to 70 °C
- Downward Compatible with 64K X 9 SIP (TM4164EL9, TM4164FM9)

description

The TM425___9 series are 2304K, dynamic random-access memory modules organized as 262,144 \times 9 bits [bit nine (D9, Q9) is \cdots rally used for parity and is controlled by \cdots right a 30-pin single-in-line package comprising nine TMS425_FML, 262,144 \times 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3

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Pi	N NOMENCLATURE TM425_EL9
A0-A8	Address Inputs
CAS, CAS9	Column-Address Strobes
DQ1-DQ8	Data in/Data Out
D9	Data In
NC	No Connection
Q9	Data Out
RAS	Row-Address Strobe
VDD	5-V Supply
VSS	Ground
W	Write Enable

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inch board spacing the TM425____9 has a density of ten devices per square inch (approximately 4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

The TM425___9 features RAS access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation as low as 2025 mW typical operating and 115 mW typical standby for 200 ns devices.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with \overrightarrow{RAS} in order to retain data. \overrightarrow{CAS} can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM425___9 is rated for operation from 0°C to 70°C.

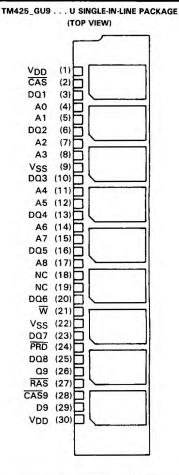
presence detect

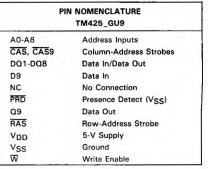
This feature is included on the TM425_GU9 to allow for hardware processed detection of the memory module. The Fir2 pin for each module in the system should be pulled high through a pull-up resistor, resulting in a logic one when no realle is present. When a module is present, Fir3 is a logic zero as this pin is connected to VSS on the module. PRD can only be used to detect a modules' presence, not its functionality. In a system not requiring presence detect, it is recommended that this pin be left as a no connect; this allows the use of either type of module without adverse effects.

operation

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262, 144 storage cell locations on each of the nine chips. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe (\overline{RAS}). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the







column-address strobes (CAS for M1 thru and CAS9 for M9). All addresses must be stable on or before the falling edges of RAS and CAS. into is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. CAS is used as a chip select activating the column decoder and the input and output buffers for M1-M8. CAS9 is used similarly for M9.

write enable (W)

The read or write mode is selected through the write-enable (\overline{W}) input. A logic high on the \overline{W} input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM425___9 dictates the use of early write cycles to prevent contention on D and Q. When \overline{W} goes low prior to \overline{CAS} , the data outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ8, D9)

Data is written during a write cycle. The falling edge of \overline{CAS} strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, \overline{W} is brought low prior to \overline{CAS} and the data is strobed in by \overline{CAS} with setup and hold times referenced to this signal.

data out (DQ1-DQ8, D9)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state until \overrightarrow{CAS} is brought low. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of \overrightarrow{CAS} as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while \overrightarrow{CAS} is low: \overrightarrow{CAS} going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the highimpedance state, a necessity due to the common I/O feature of the TM425____9.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless \overline{CAS} is applied, the \overline{RAS} -only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with \overline{RAS} causes all bits in each row to be refreshed. \overline{CAS} can remain high (inactive) for this refresh sequence to conserve power.

CAS-before-RAS refresh

The CAS-before-RAS refresh is utilized by bringing CAS low earlier than RAS (see parameter t_{CLRL}) and holding it low after RAS falls (see parameter t_{RLCHR}). For successive CAS-before- \overline{F} refresh cycles, CAS can remain low while cycling RAS. The external address is ignored and the refresh address is generated internally.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding CAS at VIL after a read operation and cycling RAS after a specified precharge period, similar to a "RAS-only" refresh cycle. The external address is also ignored during the hidden refresh cycles.

page-mode (TM4256__9)

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated.



nibble mode (TM4257__9)

Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. The next sequential nibble bits can be read or written by cycling \overrightarrow{CAS} while \overrightarrow{RAS} remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Column A8 and row A8 (CA8, RA8) provide the two binary bits for initial selection of the nibble addresses. Thereafter, the falling edge of \overrightarrow{CAS} will access the next bit of the circular 4-bit nibble in the following sequence:

▶(0,0) → (0,1) → (0,1)	► (1,0)	►(`	1,1)	
------------------------	---------	-----	-----	---	--

In nibble-mode, all normal memory operations (read, write, or ready-modify-write) may be performed in any desired combination.

power up

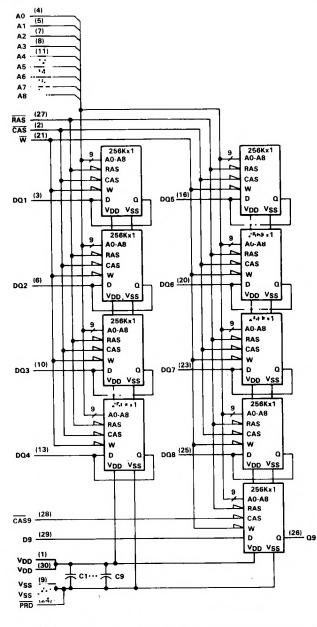
To achieve proper operation, an initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness Bypass capacitors: Multilayer ceramic Leads: Tin/lead solder coated over phosphor-bronze Contact area for socketable devices: Nickel plate and solder plate on top of copper



functional block diagram



[†]TM425_GU9 only.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Voltage range for any pin except VDD and data out (see Note 1) $\ldots \ldots \ldots \ldots -1.5$ V to 10 V
Voltage range on VDD supply and data out with respect to VSS
Short circuit output current for any output
Power dissipation
Operating free-air temperature range
Storage temperature range

[†] Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to VSS.

recommended operating conditions

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	4.5	5	5.5	v
Vss	Supply voltage		0		v
VIH	High-level input voltage	2.4		6.5	V
VIL	Low-level input voltage (see Note 2)	-1		0.8	v
Τ _A	Operating free-air temperature	- 0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST	тм	425!	9-12	ΤM	425	9-15	UNIT
	(ARAMETER	CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VOH	High-level output voltage	IOH = -5 mA	2.4		VDD	2.4		VDD	v
Vol	Low-level output voltage	IOL = 4.2 mA	0		0.4	0		0.4	v
ij	Input current (leakage)	$V_{I} = 0 V$ to 6.5 V, $V_{DD} = 5 V$, All other pins = 0 V			± 10			±10	μA
ю	Output current (leakage)	$V_0 = 0.4 V$ to 5.5 V, $V_{DD} = 5 V$, CAS high			± 10			±10	μΑ
^I DD1 [‡]	Average operating current during read or write cycle	t _C = minimum cycle, All outputs open		585	702		495	612	mA
^I DD2 [‡]	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open		23	41		23	41	mA
¹ DD3 [‡]	Average refresh current	t _c = minimum cycle, CAS high and RAS cycling, All outputs open		405	540		360	477	mA
	Average page-mode current	t _{c(P)} = minimum cycle, RAS low and CAS cycling, All outputs open		315	432		270	387	mA
	Average nibble-mode current	$t_{C(N)} = minimum cycle,RAS low and CAS cycling,All outputs open$		288	396		243	351	mA

[†]All typical values are at $T_A = 25 \,^{\circ}C$ and nominal supply voltages.

[‡]IDD1-IDD5 are measured with M1-M9 in the same mode (i.e., operating, standby, refresh, page mode, nibble mode).



RADAMETER		TEST	TM4259-20			UNIT
	PARAMETER	CONDITIONS	MIN	TYP [†]	MAX	UNIT
Vон	High-level output voltage	IOH = -5 mA	2.4		VDD	V
VOL	Low-level output voltage	loL = 4.2 mA	0		0.4	V
4	Input current (leakage)	$V_{I} = 0 V$ to 6.5 V, $V_{DD} = 5 V$, All other pins = 0 V			±10	μA
ю	Output current (leakage)	V _O = 0.4 V to 5.5 V, V _{DD} = 5 V, CAS high			±10	μA
DD1 [‡]	Average operating current during read or write cycle	t _c = minimum cycle, All outputs open		405	522	mA
	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open		23	41	mA
¹ DD3 [‡]	Average refresh current	t _c = minimum cycle, CAS high and RAS cycling, All outputs open		315	432	mA
IDD4 [‡]	Average page-mode current	t _{c(P)} = minimum cycle, RAS low and CAS cycling, All outputs open		225	315	mA
IDD5 [‡]	Average nibble-mode current	t _{C(N)} = minimum cycle, RAS low and CAS cycling, All outputs open		198	288	mA

ectrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

[†]All typical values are at $T_A = 25$ °C and nominal supply voltages.

[‡]IDD1-IDD5 are measured with M1-M9 in the same mode (i.e., operating, standby, refresh, page mode, nibble mode).

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

	PARAMETER	MIN MAX	UNIT
Ci(A)	Input capacitance, address inputs	63	pF
Ci(DQ)	Input capacitance, data inputs	17	pF
Ci(RAS)	Input capacitance, RAS input	72	pF
Ci(W)	Input capacitance, W input	72	pF
Ci(CAS9)	Input capacitance, CAS9 input	8	pF
Ci(CAS)	Input capacitance, CAS input	64	pF
Ci(D9)	Input capacitance, D9 input	7	pF
Co(Q9)	Output capacitance, Q9 output	10	pF
Co(VDD)	Decoupling capacitance	0.8	μF



switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4259-12		TM4259-15		UNIT
				MIN	MAX	MIN	MAX	UNIT
ta(C)	Access time from \overline{CAS}	C _L = 100 pF, Load = 2 Series 74 TTL gates	tCAC		60		75	ns
ta(R)	Access time from RAS	t _{RLCL} = MAX, Load = 2 Series 74 TTL gates	^t RAC		120		150	ns
^t dis(CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL gates	tOFF	0	35	0	35	ns

	PARAMETER	TEST CONDITIONS	ALT. SYMBOL	TM425_ MIN	9-20 MAX	UNIT
^t a(C)	Access time from CAS	C _L = 100 pF, Load = 2 Series 74 TTL gates	tCAC		100	ns
t _{a(R)}	Access time from RAS	t _{RLCL} = MAX, Load = 2 Series 74 TTL gates	^t RAC		200	ns
^t dis(CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL gates	tOFF	0	35	ns



		ALT. SYMBOL	TM4259-12 MIN MAX	UNIT
t _{c(P)}	Page-mode cycle time (read or write cycle)	tPC	120	ns
tc(rd)	Read cycle time [†]	tRC	230	ns
t _{c(W)}	Write cycle time	twc	230	ns
tw(CH)P	Pulse duration, CAS high (page mode)	tCP	50	ПS
tw(CH)	Pulse duration, CAS high (non-page mode)	tCPN	25	ns
tw(CL)	Pulse duration, CAS low	tCAS	60 10,000	ns
tw(RH)	Pulse duration, RAS high (precharge time)	tRP	100	ns
tw(RL)	Pulse duration, RAS low	tRAS	120 10,000	ns
tw(W)	Write pulse duration	twp	40	ns
tt	Transition times (rise and fall) for RAS and CAS	tŢ	3 50	ns
tsu(CA)	Column-address setup time	tASC	0	ns
t _{su(RA)}	Row-address setup time	tASR	0	ns
t _{su(D)}	Data setup time	tDS	0	ns
t _{su(rd)}	Read-command setup time	tRCS	0	ns
tsu(WCL)	Early write-command setup time before CAS low	twcs	0	ns
t _{su} (WCH)	Write-command setup time before CAS high	tCWL	40	กร
t _{su} (WRH)	Write-command setup time before RAS high	tRWL	40	ns
th(CLCA)	Column-address hold time after CAS low	tCAH	20	ns
th(RA)	Row-address hold time	tRAH	15	ns
th(RLCA)	Column-address hold time after RAS low	tAR	80	ns
th(CLD)	Data hold time after CAS low	tDH	35	ns
th(RLD)	Data hold time after RAS low	tDHR	95	ns
th(CHrd)	Read-command hold time after CAS high	tRCH	0	ns
th(RHrd)	Read-command hold time after RAS high	tRRH	10	ns
th(CLW)	Write-command hold time after CAS low	tWCH	35	ns
th(RLW)	Write-command hold time after RAS low	tWCR	95	ns
TRLCH	Delay time, RAS low to CAS high	tCSH	120	ns
*CHRL	Delay time, CAS high to RAS low	^t CRP	0	ns
tCLRH	Delay time, CAS low to RAS high	tRSH	60	ns
TRLCHR	Delay time, RAS low to CAS high [‡]	tCHR	25	ns
tCLRL	Delay time, CAS low to RAS low [‡]	tCSR	25	ns
TRHCL	Delay time, RAS high to CAS low [‡]	tRPC	20	ns
^t RLCL	Delay time, RAS low to CAS low (maximum value specified only to guarantee access time)	^t RCD	30 60	ns
trf	Refresh time interval	tREF	'4	m

Dynamic RAM Modules

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min. [†]All cycle times assume t_t = 5 ns. [‡]CAS-before-RAS refresh only.



		ALT.	TM4259-15	TM4259-20	UNIT
		SYMBOL	MIN MAX	MIN MAX	UNIT
tc(P)	Page-mode cycle time (read or write cycle)	tPC	145	· · · · · · · · · · · · · · · · · · ·	ns
tc(rd)	Read cycle time [†]	tRC	260	330	ns
tc(W)	Write cycle time	tWC	260	330	ns
tw(CH)P	Pulse duration, CAS high (page mode)	tCP	60	80	ns
tw(CH)	Pulse-duration, CAS high (non-page mode)	^t CPN	25	30	ns
tw(CL)	Pulse duration, CAS low	tCAS	75 10,000	100 10,000	ns
tw(RH)	Pulse duration, RAS high (precharge time)	tRP	100	120	ns
tw(RL)	Pulse duration, RAS low	TRAS	150 10,000	200 10,000	ns
tw(W)	Write pulse duration	twp	45	55	ns
tt	Transition times (rise and fall) for RAS and CAS	ţТ	3 50	3 50	пѕ
t _{su(CA)}	Column-address setup time	tASC	0	0	ns
tsu(RA)	Row-address setup time	tASR	0	0	ns
tsu(D)	Data setup time	tDS	0	0	ns
tsu(rd)	Read-command setup time	tRCS	0	0	ns
t _{su} (WCL)	Early write-command setup time before CAS low	twcs	0	0	ns
tsu(WCH)	Write-command setup time before CAS high	tCWL	45	60	ns
tsu(WRH)	Write-command setup time before RAS high	tRWL	45	60	ns
th(CLCA)	Column-address hold time after CAS low	^t CAH	25	30	ns
th(RA)	Row-address hold time	^t RAH	15	20	ns
th(RLCA)	Column-address hold time after RAS low	tAR	100	130	ns
th(CLD)	Data hold time after CAS low	tDH	45	55	ns
th(RLD)	Data hold time after RAS low	^t DHR	120	155	ns
th(CHrd)	Read-command hold time after CAS high	^t RCH	0	0	ns
th(RHrd)	Read-command hold time after RAS high	tRRH	10	15	ns
th(CLW)	Write-command hold time after CAS low	tWCH	45	55	ns
th(RLW)	Write-comi nold time after RAS low	tWCR	120	155	ns
tRLCH	Delay time, ow to CAS high	tCSH	150	200	ns
tCHRL	Delay time, CAS high to RAS low	tCRP	0	0	ns
tCLRH	Delay time, CAS low to RAS high	tRSH	75	100	ns
TRLCHR	Delay time, RAS low to CAS high [‡]	tCHR	30	35	ns
tCLRL	Delay time, CAS low to RAS low [‡]	tCSR	30	35	ns
	Delay time, RAS high to "" low [‡]	tRPC	20	25	ns
^t RHCL	Delay time, RAS low to CAS low	- nru			
^t RLCL	(maximum value specified only to guarantee access time)	¹ RCD	30 75	30 100	ns
trf	Refresh time interval	tREF	4	4	ms

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min. [†]All cycle times assume t_t = 5 ns.

*CAS-before-RAS refresh only.

ti3 TEXAS INSTRUMENTS POST OFFICE BOX 1443 . HOUSTON, TEXAS 77001

TM4257EL9, TM4257GU9 262,144 BY 9-BIT DYNAMIC RAM MODULES

NIBBLE-MODE CYCLE

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT.	TM4257	9-12	TM425	79-15	TM4257	9.20	UNIT
		SYMBOL	MIN MAX		MIN	MAX	MIN	MA	OM11
ta(CN)	Nibble-mode access time from CAS	^t NCAC		30		40		50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT.			TM4257				UNIT
		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	
tc(N)	Nibble-mode cycle time	tNC	60		75		90		
^t CLRHN	Nibble-mode delay time, CAS low to RAS high	^t NRSH	30		40		50		
tCLWLN	Nibble-mode delay time, CAS to W delay	tNCWD	25		30		40		
tw(CLN)	Nibble-mode pulse duration, CAS low	t NCAS	30		40		50		ns
tw(CHN)	Nibble-mode pulse duration, CAS high	^t NCP	20		25		30		
^t su(WCHN)	Nibble-mode write command setup time before CAS high	^t NCWL	25		35		45		



PARAMETER MEASUREMENT INFORMATION

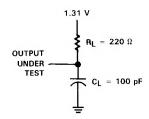
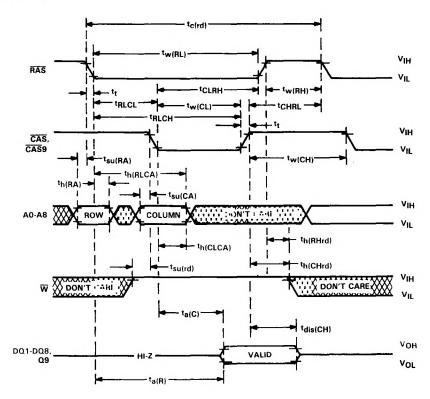


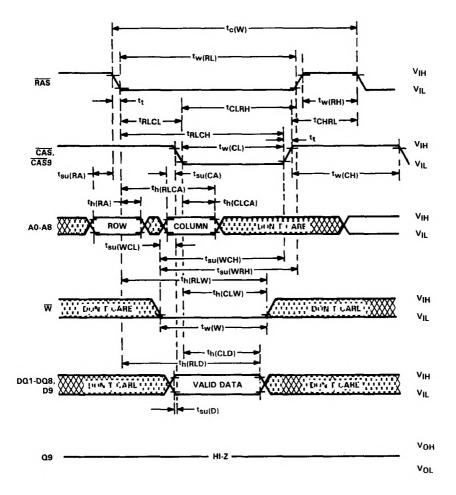
FIGURE 1. LOAD CIRCUIT







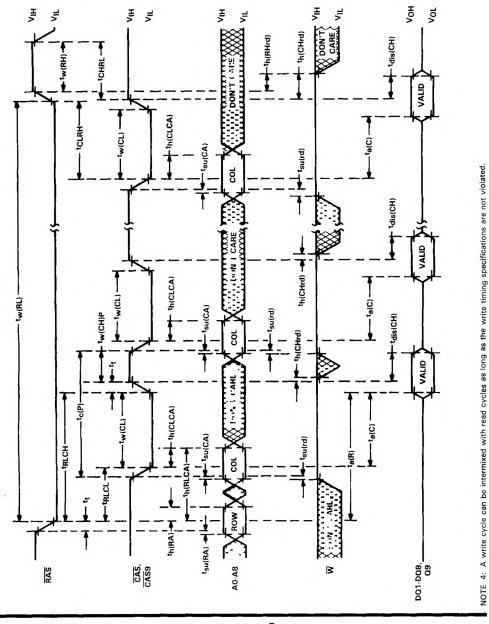
early write cycle timing





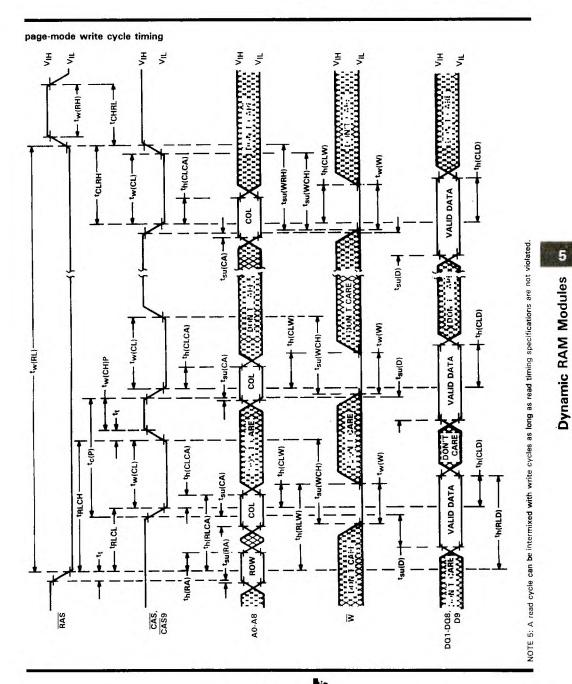
TM4256EL9, TM4256GU9 262,144 BY 9-BIT DYNAMIC RAM MODULES

page-mode read cycle timing





Dynamic RAM Modules



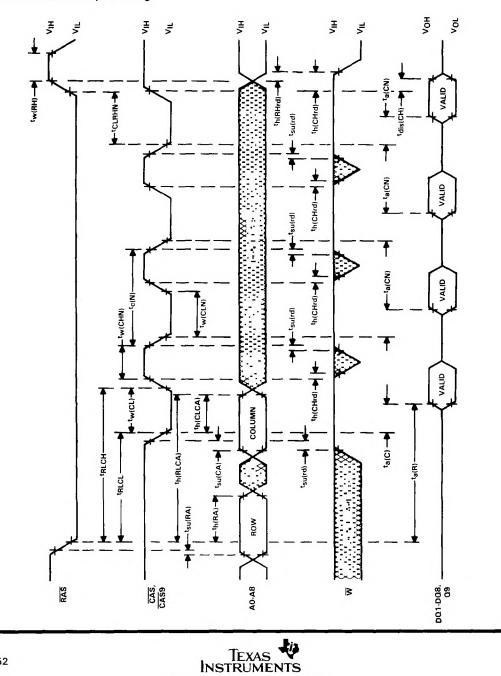
TM4256EL9, TM4256GU9 262,144 BY 9-BIT DYNAMIC RAM MODULES

TEXAS W INSTRUMENTS

5-151

TM4257EL9, TM4257GU9 262,144 BY 9 BIT DYNAMIC RAM MODULES

nibble-mode read cycle timing



5-152

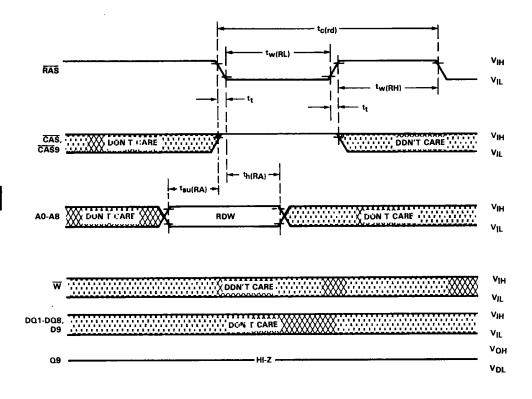
POST OFFICE BOX 1443 . HOUSTON, TEXAS 77001

nibble-mode write cycle timing YIH V H ž ۲IH ž **HIN** ۲F NH N 1 Ę + -tsu(WCHN) tw(RH) ---th(WLD) -tsu(WRH) -tcLRHN-W(W) VALID +(CLW)th(WLD) (M) M1 VALID -(MTO)4 12 (MLD) · (N)· (NICLN) (NHC)M1 VALID (h(CLW) su(WCHN) tsu(D)+ th(CLD) -tw(CL)-(PCLCA) tsu(CA) COLUMN VALID su(WCF th(WLD) + (M)m1+ -(M)-)H TRLCH-(h(RLCA) Ī (HLD) (h(RLW) FRLCL-+ th(RA) + - tsu(RA) ROW 2 Ŧ CAS, A0-A8 DQ1-DQ8 D9 RAS 3

TEXAS VI INSTRUMENTS POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001 5

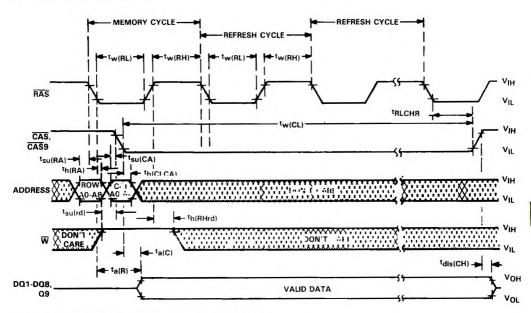
Dynamic RAM Modules

RAS-only refresh timing

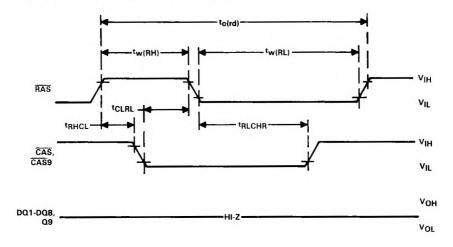


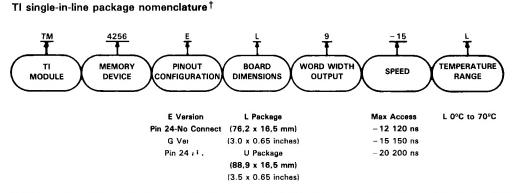


hidden refresh cycle timing



automatic (CAS-before-RAS) refresh cycle timing





[†]The E pinout configuration designator is used when specifying the L package; the G pinout configuration version designator is used when specifying the U package.



OCTOBER 1985- REVISED NOVEMBER 1985

- 262,144 X 5 Organization
- Single 5-V Supply (10% Tolerance)
- 24-Pin Single-in-Line Package (SIP)
- Utilizes Five 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

	ACCESS	ACCESS	READ	READ-
	TIME	TIME	OR	MODIFY-
	ROW	COLUMN	WRITE	WRITE
	ADDRESS	ADDRESS	CYCLE	CYCLE
	(MAX)	(MAX)	(MIN)	(MIN)
TM425 EQ5-12	120 ns	60 ns	230 ns	275 ns
TM425_EQ5-15	150 ns	75 ns	260 ns	305 ns
TM425_EQ5-20	200 ns	100 ns	330 ns	370 ns

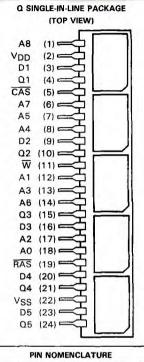
- Common CAS Control with Separate Data-Input and Output Lines
- Low Power Dissipation:

	OPERATING	STANDBY
	(TYP)	(TYP)
TM425_EQ5-12	1625 mW	65 mW
TM425_EQ5-15	1375 mW	65 mW
TM425_EQ5-20	1125 mW	65 mW

- Operating Free-Air Temperature . . . 0 °C to 70 °C
- Downward Compatible with 64K X 5 Singlein-Line Package (TM4164EQ5)

description

The TM425_EQ5 is a 1280K, dynamic randomaccess memory module organized as 262,144 × 5 bits in a 24-pin single-in-line package



· · · · · · · · · · · · · · · · · · ·	PIN NOMENCLATURE	
A0-A8	Address inputs	
CAS	Column-Address Strobe	
D1-D5	Data Inputs	
NC	No Connection	
Q1-Q5	Data Outputs	
RAS	Row-Address Strobe	
VDD	5-V Supply	
VSS	Ground	
$\mathbf{\nabla}$	Write Enable	

comprising five TMS425_FML, 262,144 \times 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with five 0.1 μ F decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM425_EQ5 has a density of ten devices per square inch (approximately 4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

The TM425_EQ5 features RAS access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation as low as 1125 mW typical operating and 65 mW typical standby.

Refresh period is extended to 4 minus conds, and during this period each of the 256 rows must be strobed with RAS in order to retain data. CAS can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM425_EQ5 is rated for operation from 0°C to 70°C.

operation

address (A0 through A8)

Eight address bits are required to decode 1 of 262,144 storage cell locations on each of the five chips. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe (\overline{RAS}). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe. All addresses must be stable on or before the falling edges of \overline{RAS} and \overline{CAS} . \overline{RAS} is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. \overline{CAS} is used as a chip select activating the column decoder and the input and output buffers.

write enable (W)

The read or write mode is selected through the write-enable (\overline{W}) input. A logic high on the \overline{W} input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. When \overline{W} goes low prior to \overline{CAS} , the data-outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (D1-D5)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of \overline{CAS} or \overline{W} strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, \overline{W} is brought low prior to \overline{CAS} and the data is strobed in by \overline{CAS} with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, \overline{CAS} will already be low, thus the data will be strobed in by \overline{W} with setup and hold times referenced to this signal.

data-out (Q1-Q5)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state until CAS is brought low. In a read cycle the outputs go active after the access time interval $t_{a}(C)$ that begins with the negative transition of CAS as long as $t_{a}(R)$ is satisfied. The outputs become valid after the access time has elapsed and remain valid while CAS is low; CAS going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless \overline{CAS} is applied, the \overline{RAS} -only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with \overline{RAS} causes all bits in each row to be refreshed. \overline{CAS} can remain high (inactive) for this refresh sequence to conserve power.

CAS-before-RAS refresh

The \overline{CAS} -before \overline{RAS} refresh is utilized by bringing \overline{CAS} low earlier than \overline{RAS} (see parameter t_{CLRL}) and holding it low after \overline{RAS} falls (see parameter t_{RLCHR}). For successive \overline{CAS} -before \overline{RAS} refresh cycles, \overline{CAS} can remain low while cycling \overline{RAS} . The external address is ignored and the refresh address is generated internally.



hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding CAS at VIL after a read operation and cycling RAS after a specified precharge period, similar to a "RAS-only" refresh cycle. The external address is also ignored during the hidden refresh cycles.

page-mode (TM4256EQ5)

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single module, the row address and RAS are applied to multiple modules. CAS is then decoded to select the proper module.

nibble mode (TM4257EQ5)

Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. The next sequential nibble bits can be read or written by cycling CAS while RAS remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Column A8 and row A8 (CA8, RA8) provide the two binary bits for initial selection of the nibble addresses. Thereafter, the falling edge of \overline{CAS} will access the next bit of the circular 4-bit nibble in the following sequence:

► (0,0)	 	

In nibble-mode, all normal memory operations (read, write, or read-modify-write) may be performed in any desired combination.

power up

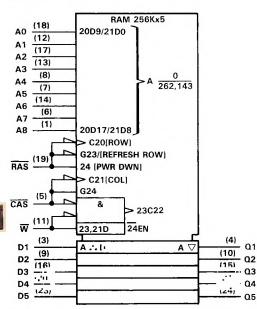
To achieve proper device operation, an initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness Bypass capacitors: Multilayer ceramic Leads: Tin/lead solder coated over phosphor-bronze



logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

(18)A0 (12) A1 (17) A2 (13) A3 (8) A4 (7) Α5 (14) A6 (6) Α7 (1) **RAM 256Kx1** A8 (19) q A0-A8 RAS (5) CAS RAS (11) w CAS w (4) (3) D1 D - 01 a VDD Vss **RAM 256Kx1** c A0-A8 RAS CAS w D2 (9) (1<u>0)</u> 02 D ۵ VDD Vss RAM 256Kx1 A0-A8 RAS CAS w (15) (16) D 03 D3 ۵ VDD Vss **RAM 256Kx1** A0-A8 RAS CAS w (20) (21) D 04 D4 -۵ Vss VDD RAM 256Kx1 A0-A8 RAS CAS w (24) Q5 (23) D5 D a Vss VDD (2) VDD C5 CI (22) 0.1 µF 01 µF Vss

functional block diagram



Dynamic RAM Modules

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Voltage range for any pin except V _{DD} and data out (see Note 1) $\dots \dots \dots \dots \dots -1.5$ V to 10 V
Voltage range on V _{DD} supply and data out with respect to V _{SS} $\dots \dots \dots \dots \dots \dots - 1$ V to 6 V
Short circuit output current for any output
Power dissipation
Operating free-air temperature range
Storage temperature range

[†]Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Dperating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NDTE 1: All voltage values in this data sheet are with respect to VSS.

recommended operating conditions

-		MIN	NOM	MAX	UNIT
VDD	Supply voltage	4.5	5	5.5	V
VSS	Supply voltage		0		V
VIH	High-level input voltage	2.4		6.5	V
VIL	Low-level input voltage (see Note 2)	-1		0.8	V
Тд	Dperating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST	TM	TM425_EQ5-12		TM	425_EQ	5-15	UNIT
		CONDITIONS	MIN TYP [†]		MAX	MIN	TYP	MAX	UNI
Voн	High-level output voltage	IOH = -5 mA	2.4		VDD	2.4		VDD	v
VOL	Low-level output voltage	I _{OL} = 4.2 mA	0		0.4	0		0.4	V
il -	Input current (leakage)	$V_{I} = 0 V \text{ to } 6.5 V, V_{DD} = 5 V,$ All other pins = 0 V			±10			±10	μΑ
۱D	Dutput current (leakage)	$V_D = 0.4 V$ to 5.5 V, $V_{DD} = 5 V$, CAS high			±10			± 10	μA
IDD1	Average operating current during read or write cycle	t _C = minimum cycle, All outputs open		325	390		275	340	mA
IDD2	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open		13	23		13	23	mA
IDD3	Average refresh current	t _C = minimum cycle, CAS high and RAS cycling, All outputs open		225	300		200	265	mA
IDD4	Average page-mode current	t _{c(P)} = minimum cycle, RAS low and CAS cycling, All outputs open		175	240		150	215	mA
lDD5	Average nibble-mode current	t _{c(N)} = minimum cycle, RAS low and CAS cycling, All outputs open		160	220		135	160	mA

[†]All typical values are at $T_A = 25 \,^{\circ}$ C and nominal supply voltages.



PARAMETER		TEST	TM4	TM425_EQ5-20			
		CONDITIONS	MIN	TYP [†]	MAX	UNIT	
VOH	High-level output voltage	I _{OH} = -5 mA	2.4		VDD	v	
VOL	Low-level output voltage	i _{OL} = 4.2 mA	0		0.4	V	
4	Input current (leakage)	$V_{I} = 0 V$ to 6.5 V, $V_{DD} = 5 V$, All other pins = 0 V			±10	μΑ	
1 ₀	Output current (leakage)	V _O = 0.4 V to 5.5 V, V _{DD} = 5 V, CAS high			± 10	μΑ	
IDD1	Averege operating current during read or write cycle	t _c = minimum cycle, All outputs open		225	290	mA	
ⁱ DD2	Standby current	After 1 memory cycle, RAS and CAS high,		13	23	mA	
IDD3	Average refresh current	All outputs open t _c = minimum cycle, CAS high and RAS cycling, All outputs open		175	240	mA	
I _{DD4}	Average page-mode current	t _c (p) = minimum cycle, RAS low and CAS cycling, All outputs open		125	175	mA	
IDD5	Average nibble-mode current			110	160	mA	

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

[†]All typical values are at $T_A = 25$ °C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, $f\,=\,1\,\,\text{MHz}$

	PARAMETER	MIN MAX	UNIT
C _{i(A)}	Input capacitance, address inputs	35	pF
C _{i(D)}	input capacitance, data inputs	35	pF
C _{i(RAS)}	Input capacitance, RAS input	40	pF
C _{i(W)}	Input capacitance, W input	40	рF
Ci(CAS)	Input capacitance, CAS input	40	pf
C _{o(Q)}	Output capacitance, data outputs	10	рF
Co(VDD)	Decoupling capacitance	0.6	μ۴

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switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		PARAMETER TEST CONDITIONS		TM425_EQ5-12		TM425 EQ5-15		UNIT
				MIN	MAX	MIN	MAX	UNIT
t _{a(C)}	Access time from CAS	C _L = 100 pF, Load = 2 Series 74 TTL gates	^t CAC		60		75	ns
t _{a(R)}	Access time from RAS	t _{RLCL} = MAX, Load = 2 Series 74 TTL gates	^t RAC		120		150	ns
t _{dis} (CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL getes	tOFF	0	35	0	35	ns

	DADAMETER	TEGT CONDITIONS	ALT. TM4		ALT. TM425_EQ5-2		EQ5-20	
	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNIT		
t _{a(C)}	Access time from CAS	C _L = 100 pF, Load = 2 Series 74 TTL gates	†CAC		100	ns		
t _{a(R)}	Access time from RAS	t <mark>RLCL ≕</mark> MAX, Load ≕ 2 Series 74 TTL gates	^t RAC		200	ns		
^t dis(CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL gates	tOFF	0	35	ns		



		ALT. SYMBOL	TM425_E05-12 MIN ****	UNIT
tc(P)	Page-mode cycle time (read or write cycle)	tPC	120	ns
tc(PM)	Page-mode cycle time (read-modify-write cycle)	^t PCM	165	ns
tc(rd)	Read cycle time [†]	tRC	230	ns
tc(W)	Write cycle time	twc	230	ns
tc(rdW)	Read-write/read-modify-write cycle time	tRWC	275	ns
tw(CH)P	Pulse duration, CAS high (page mode)	tCP	50	ns
tw(CH)	Pulse duration, CAS high (non-page mode)	tCPN	25	ns
tw(CL)	Pulse duration, CAS low [‡]	tCAS	60 10,000	ns
tw(RH)	Pulse duration, RAS high	tRP	100	ns
tw(RL)	Pulse duration, RAS low [§]	tRAS	120 10,000	ns
tw(W)	Write pulse duration	twp	40	ns
tt	Transition times (rise and fall) for RAS and CAS	tŢ	3 50	ns
t _{su} (CA)	Column-address setup time	tASC	0	ns
t _{su} (RA)	Row-address setup time	tASR	0	ns
tsu(D)	Data setup time	tDS	0	ns
tsu(rd)	Read-command setup time	tRCS	0	ns
t _{su} (WCL)	Early write-command setup time before CAS low	twcs	0	ns
t _{su} (WCH)	Write-command setup time before CAS high	tCWL	40	ns
t _{su} (WRH)	Write-command setup time before RAS high	tRWL	40	ns
th(CLCA)	Column-address hold time after CAS low	tCAH	20	ns
th(RA)	Row-address hold time	tRAH	15	ns
th(RLCA)	Column-address hold time after RAS low	tAR	80	ns
th(CLD)	Data hold time after CAS low	†DHC	35	ns
th(RLD)	Data hold time after RAS low	^t DHR	95	ns
th(WLD)	Data hold time after W low	tDHW	35	ns
th(CHrd)	Read-command hold time after CAS high	^t RCH	0	ns
th(RHrd)	Read-command hold time after RAS high	tRRH	10	ns
th(CLW)	Write-command hold time after CAS low	tWCH	35	ns
th(RLW)	Write-command hold time after RAS low	tWCR	95	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

Continued next page.

NOTE 3: Timing measurements are referenced to VIL max and VIH min.

[†]All cycle times assume $t_t = 5$ ns.

⁺In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional CAS low time $t_{w(CL)}$. This applies to page-mode read-modify-write also.

[§]In a read-modify-write cycle,t_{RLWL} and t_{su(WRH)} must be observed. Depending on the user's transition times, this may require additional RAS low time (t_{w(RL)}).



		ALT. SYMBOL	TM\$425_F05-12 MIN MA	UNIT
RLCH	Delay time, RAS low to CAS high	tCSH	120	ns
CHRL	Delay time, CAS high to RAS low	tCRP	0	ns
CLRH	Delay time, CAS low to RAS high	trsh	60	ns
TRLCHR	Delay time, RAS low to CAS high	tCHR	25	ns
CLRL	Delay time, CAS low to RAS low	tCSR	25	ns
RHCL	Delay time, RAS high to CAS low	tRPC	20	ns
CLWL	Delay time, CAS low to W low (read-modify-write cycle only)	tCWD	60	ns
TRLCL	Delay time, RAS low to CAS low (maximum value specified only to guarantee access time)	^t RCD	30 60	កន
TRLWL	Delay time, RAS low to W low (read-modify-write cycle only)	tRWD	120	ns
t _{rf}	Refresh time interval	tREF	4	ms

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min. ICAS-before-RAS refresh only.



timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT.	TM425_EQ	5-15	TM425	EQ5-20	
	4	SYMBOL	MIN P	XAN	MIN	MAX	UNIT
tc(P)	Page-mode cycle time (read or write cycle)	^t PC	145		190		ns
t _{c(PM)}	Page-mode cycle time (read-modify-write cycle)	^t PCM	190		245	Sec 1	ns
tc(rd)	Read cycle time [†]	^t RC	260		330		ns
tc(W)	Write cycle time	twc	260	a. di	330		ns
tc(rdW)	Read-write/read-modify-write cycle time	^t RWC	305		370		ns
tw(CH)P	Pulse duration, CAS high (page mode)	tCP	60		80		ns
tw(CH)	Pulse duration, CAS high (non-page mode)	tCPN	25		30		ns
tw(CL)	Pulse duration, CAS low [‡]	tCAS	75 10	,000	100	10,000	ns
tw(RH)	Pulse duration, RAS high	tRP	100		120		ns
tw(RL)	Pulse duration, RAS low [§]	tRAS	150 10	,000	200	10,000	ns
tw(W)	Write pulse duration	tWP	45	_	55		ns
tt	Transition times (rise and fall) for RAS and CAS	ţт	3	50	3	50	ns
t _{su(CA)}	Column-address setup time	tASC	0		0		ns
t _{su(RA)}	Row-address setup time	tASR	0		0		ns
tsu(D)	Data setup time	tDS	0		0	1	ns
t _{su(rd)}	Read-command setup time	tRCS	0		0		ns
t _{su} (WCL)	Early write-command setup time before CAS low	twcs	0		0		ns
t _{su} (WCH)	Write-command setup time before CAS high	tCWL	45		60		ns
t _{su} (WRH)	Write-command setup time before RAS high	tRWL	45		60	-	ns
th(CLCA)	Column-address hold time after CAS low	^t CAH	25		30		ns
th(RA)	Row-address hold time	tRAH	15		20		ns
th(RLCA)	Column-address hold time after RAS low	tAR	100		130		ns
th(CLD)	Data hold time after " ow	^t DHC	45		55		ns
th(RLD)	Data hold time after RAS low	^t DHR	120		155		ns
th(WLD)	Data hold time after W low	tDHW	45		55		ns
th(CHrd)	Read-command hold time after CAS high	^t RCH	0		0		ns
th(RHrd)	Read-command hold time after RAS high	tRRH	10		15		ns
th(CLW)	Write-command hold time after CAS low	tWCH	45		55		ns
th(RLW)	Write-command hold time after RAS low	tWCR	120	1.10	155	(ns

Continued next page.

NOTE 3: Timing measurements are referenced to VIL max and VIH min.

[†]All cycle times assume t_t = 5 ns.

ad-modify-write cycle, t_{CLWL} and t_{su(WCH)} must be observed. Depending on the user's transition times, this may require additional
 ow time t_{w(CL)}). This applies to page-mode read-modify-write also.

³In a read-modify-write cycle, t_{RLWL} and t_{su(WRH)} must be observed. Depending on the user's transition times, this may require additional RAS low time (t_{w(RL)}).



		ALT.	TM425_	EQ5-15	TM425_	EQ5-20	
		SYMBOL	MIN	MAX	MIN	MAX	UNIT
RLCH	Delay time, RAS low to CAS high	tCSH	150		200		ns
tCHRL	Delay time, CAS high to RAS low	tCRP	0		0		ns
tCLRH	Delay time, CAS low to RAS high	tRSH	75		100		ns
TRLCHR	Delay time, RAS low to CAS high	tCHR	30		35		ns
tCLRL	Delay time, CAS low to RAS low 1	tCSR	30		35		ns
TRHCL	Delay time, RAS high to CAS low	tRPC	20		25		ns
tCLWL	Delay time, \overline{CAS} low to \overline{W} low (read-modify-write cycle only)	tCWD	70		90		ns
^t RLCL	Delay time, RAS low to CAS low (maximum value specified only to guarantee access time)	tRCD	30	75	30	100	ns
^t RLWL	Delay time, \overline{RAS} low to \overline{W} low (read-modify-write cycle only)	tRWD	145		190		ns
trf	Refresh time interval	tREF		4		4	ms

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

NOTE 3: Timing measurements are referenced to V_{1L} max and V_{1H} min. \P_{CAS}^{T} before RAS refresh only.

NIBBLE-MODE CYCLE

switching characteristics over recommended supply voltage range and operating free-air temperature range

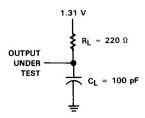
PARAMETER		ALT.	TM425	7EQ5-12	TM425	7EQ5-15	TM425	7EQ5-20	UNIT
		SYMBOL	MIN MAX		MIN MAX		MIN MAX		UNIT
ta(CN)	Nibble-mode access time from CAS	^t NCAC		30		40		50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM425 MIN	7EQ5-12 MAX	TM425 MIN	7EQ5-15 MAX	TM4257 MIN	EQ5-20 MAX	UNIT
t _{c(N)}	Nibble-mode cycle time	tNC	60		75	_	90		
tc(rdWN)	Nibble-mode read-modify-write cycle time	^t NRMW	85	1.1.1.1	105		130		
^t CLRHN	Nibble-mode delay time, CAS low to RAS high	tNRSH	30		40		50		
tCLWLN	Nibble-mode delay time, CAS to W delay	^t NCWD	25		30		40		
tw(CLN)	Nibble-mode pulse duration, CAS low	INCAS	30		40		50		ns
tw(CHN)	Nibble-mode pulse duration, CAS high	^t NCP	20		25		30		
tw(CRWN)	Nibble-mode read-modify-write pulse duration, CAS low	^t NCRW	55		70		90		
t _{su} (WCHN)	Nibble-mode write command setup time before CAS high	^t NCWL	25		35		45		

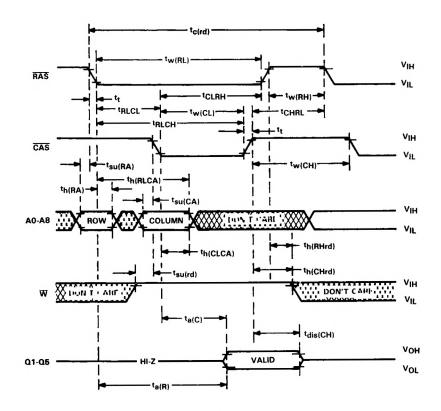


PARAMETER MEASUREMENT INFORMATION





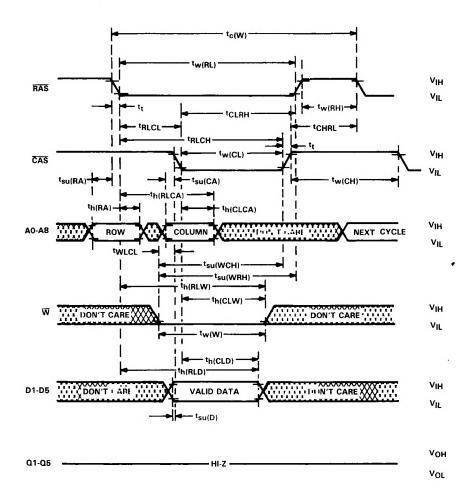






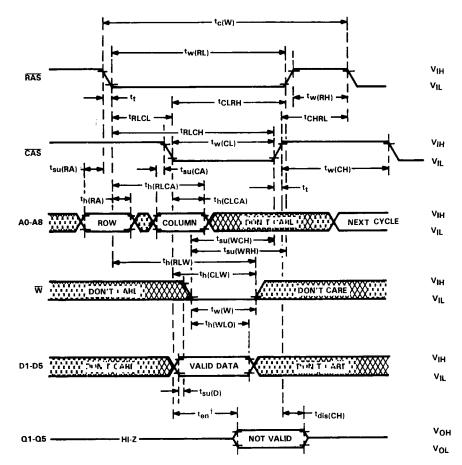
Dynamic RAM Modules

early write cycle timing



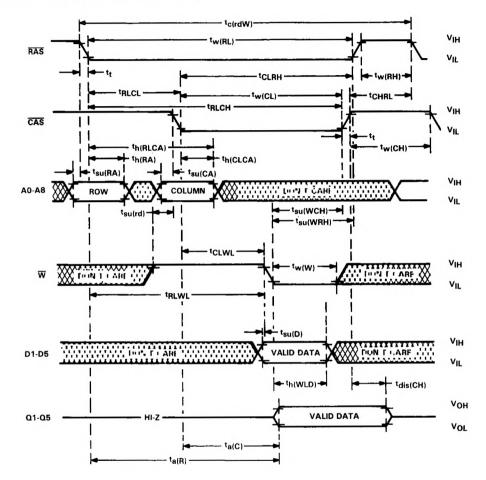


write cycle timing



[†]The enable time (t_{en}) for a write cycle is equal in duration to the access time from CAS (t_{a(C)}) in a read cycle; but the active levels et the output are invalid.



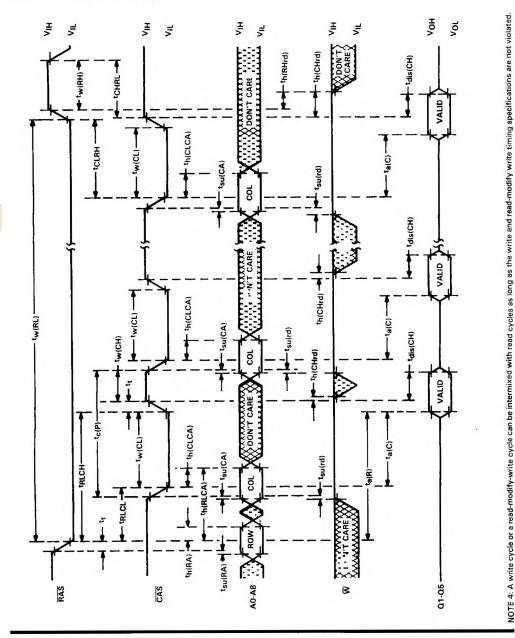


read-write/read-modify-write cycle timing



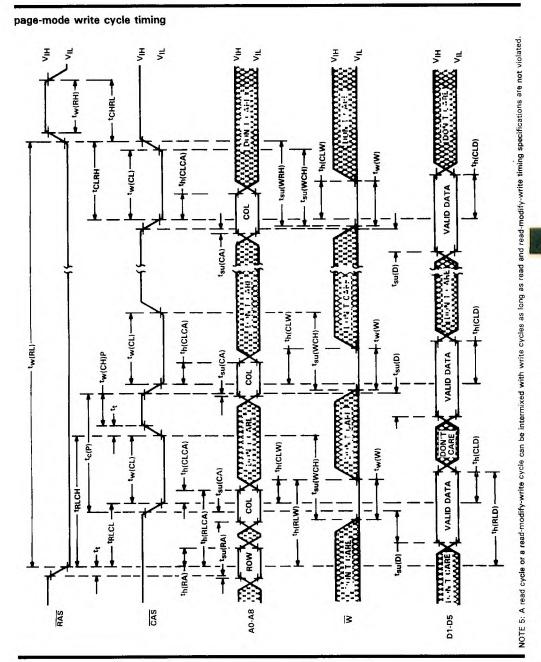
TM4256EQ5 262,144 BY 5-BIT DYNAMIC RAM MODULE

page-mode read cycle timing



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Dynamic RAM Modules



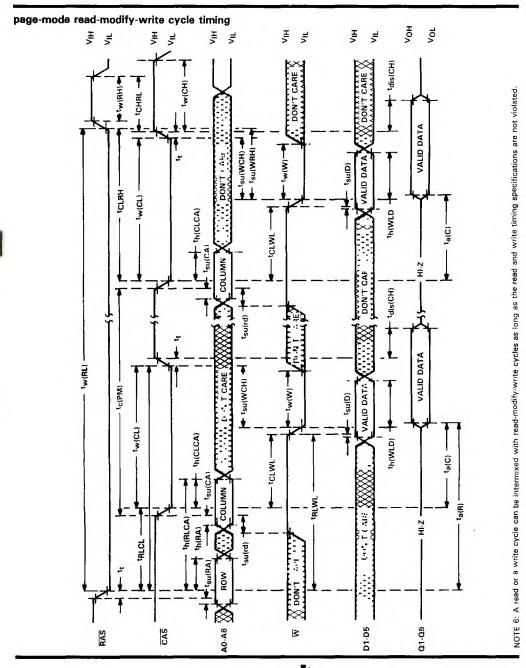
262,144 BY 5-BIT DYNAMIC RAM MODULE

TM4256EQ5

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Dynamic RAM Modules

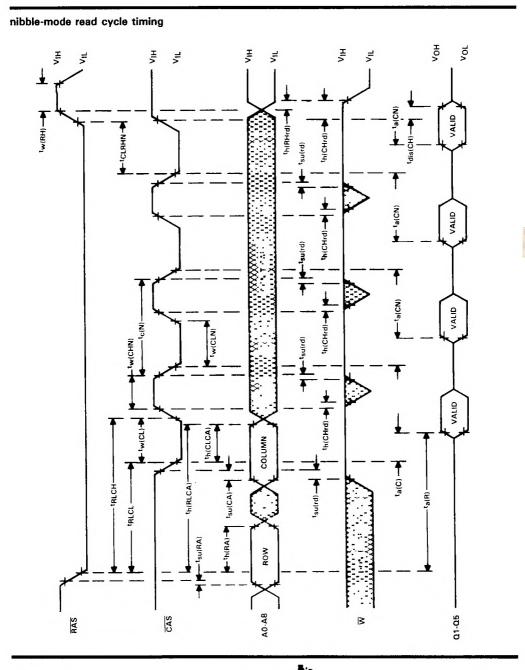


TM4256EQ5 262,144 BY 5-BIT DYNAMIC RAM MODULE

Dynamic RAM Modules

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TEXAS VI INSTRUMENTS POST OFFICE BOX 1443 • HOUSTON TEXAS 77001



TM4257EQ5 262,144 BY 5-BIT DYNAMIC RAM MODULE

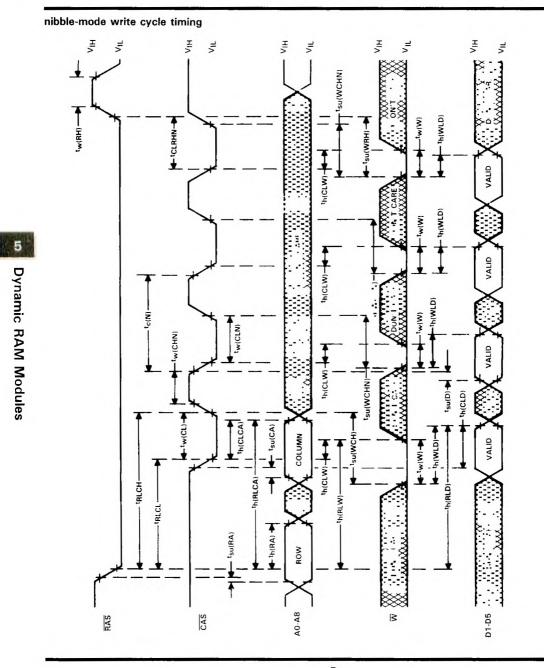
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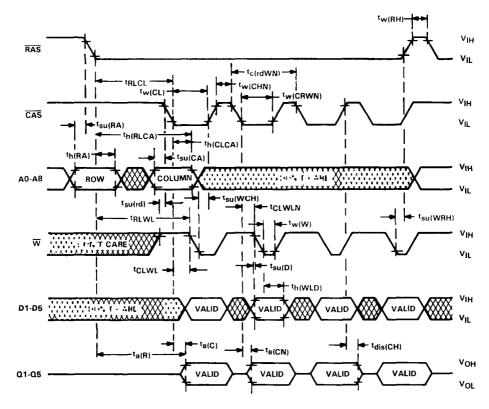
Dynamic RAM Modules

TEXAS INSTRUMENTS

TM4257EQ5 262,144 BY 5-BIT DYNAMIC RAM MODULE



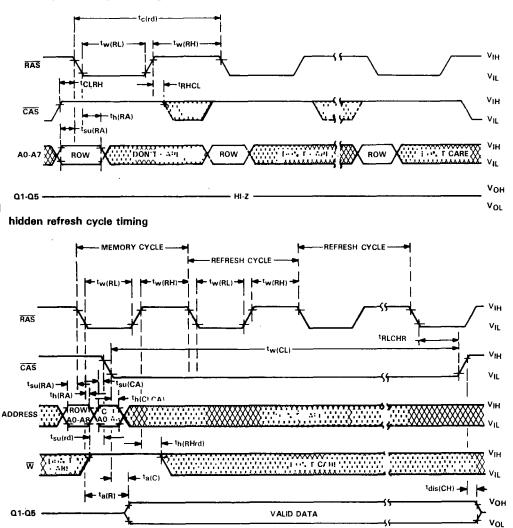




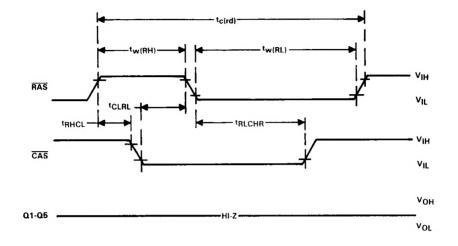
nibble-mode read-modify-write-cycle timing



RAS-only refresh cycle timing

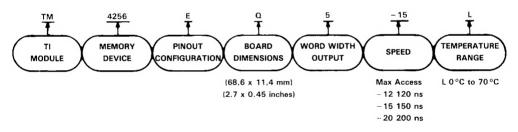






automatic (CAS-before-RAS) refresh cycle timing

TI single-in-line package nomenclature





Dynamic RAM Modules

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OCTOBER 1985 - REVISED NOVEMBER 1985

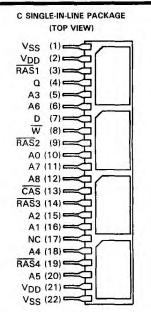
- 1,048,576 X 1 Organization
- Single 5-V Supply (10% Tolerance)
- 22-Pin Single-in-Line Package (SIP)
- Utilizes Four 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Range:

	ACCESS TIME	ACCESS TIME	READ	READ-
	ROW	COLUMN	WRITE	WRITE
	ADDRESS	ADDRESS	CYCLE	CYCLE
	(MAX)	(MAX)	(MIN)	(MIN)
TM425_FC1-12	120 ns	60 ns	230 ns	275 ns
TM425_FC1-15	150 ns	75 ns	260 ns	305 ns
-TM425_FC1-20	200 ns	100 ns	330 ns	370 ns

- Common CAS Control with Separate Data Input and Output Lines
- Operating Free-Air Temperature . . . 0 °C to 70 °C

description

The TM425_FC1 series are 1024K, dynamic random-access memory modules organized as 1,048,576 \times 1 bit in a 22-pin single-in-line package comprising four TMS425_FML, 262,144 \times 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance



Pir	NOMENCLATURE	
A0-A8	Address Inputs	
CAS	Column-Address Strobe	
D	Data Input	
NC	No Connection	
٥	Data Output	
RAS1-RAS4	Row-Address Strobes	
VDD	5-V Supply	
VSS	Ground	
W	Write Enable	

over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM425_FC1 has a density of ten devices per square inch (approximately 4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

The TM425_FC1 features RAS access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation as low as 225 mW typical operating and 50 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with RAS in order to retain data. CAS can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM425_FC1 is rated for operation from 0°C to 70°C.

5

Dynamic RAM Modules

TM4256FC1, TM4257FC1 1,048,576 By 1-Bit Dynamic Ram Modules

operation

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262, 144 storage cell locations on each of the four chips. Nine row-1.1: ess bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobes (\overline{R} .:: i- $\overline{R}AS4$). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe. All addresses must be stable on or before the falling edges of $\overline{R}AS$ and $\overline{C}AS$. $\overline{R}AS$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{C}AS$ is used as a chip select activating the column decoder and the input and output buffers.

write enable (W)

The read or write mode is selected through the write-enable (\overline{W}) input. A logic high on the \overline{W} input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a w.l up resistor. The data inputs are disabled when the read mode is selected. When \overline{W} goes low prior to v.k, the data outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write cycle. The falling edge of \overline{CAS} or \overline{W} strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, \overline{W} is brought low prior to \overline{CAS} and the data is strobed in by \overline{CAS} with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until CAS is brought low. In a read cycle the output goes active after the access time interval $t_a(C)$ that begins with the negative transition of CAS as long as $t_a(R)$ is \cdots sfied. The output becomes valid after the access time has elapsed and remains valid while CAS is low: $\vec{C} \rightarrow \cdots$ going high returns it to a high-impedance state. In the early write cycle, the output is always in the high-impedance state.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless \overline{CAS} is applied, the \overline{RAS} -only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with \overline{RAS} causes all bits in each row to be refreshed. \overline{CAS} can remain high (inactive) for this refresh sequence to conserve power. All four devices may be refreshed together by enabling $\overline{RAS}1$ - $\overline{RAS}4$ simultaneously.

CAS-before-RAS refresh

The \overline{CAS} -before- \overline{RAS} refresh is utilized by bringing \overline{CAS} low earlier than \overline{RAS} (see parameter t_{CLRL}) and holding it low after \overline{RAS} falls (see parameter t_{RLCHR}). For successive \overline{CAS} -before- \overline{RAS} refresh cycles, \overline{CAS} can remain low while cycling \overline{RAS} . The external address is ignored and the refresh address is generated internally.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding CAS at V_{IL} after a read operation and cycling RAS after a specified precharge period, similar to a "RAS-only" refresh cycle. The external address is also ignored during the hidden refresh cycles.

page mode (TM4256FC1)

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated.

nibble mode (TM4257FC1)

Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. The next sequential nibble bits can be read or written by cycling CAS while RAS remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Column A8 and row A8 (CA8, RA8) provide the two binary bits for initial selection of the nibble addresses. Thereafter, the falling edge of \overline{CAS} will access the next bit of the circular 4-bit nibble in the following sequence:

• (0,0)-			 (1,1)	<u> </u>
----------	--	--	---------------	----------

In nibble-mode, all normal memory operations (read, write, or ready-modify-write) may be performed in any desired combination.

power up

To achieve proper operation, an initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles.

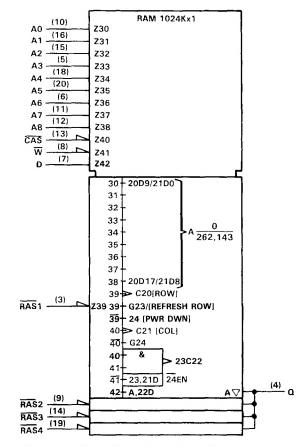
single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness Bypass capacitors: Multilayer ceramic Leads: Tin/lead solder coated over phosphor-bronze



logic symbol[†]

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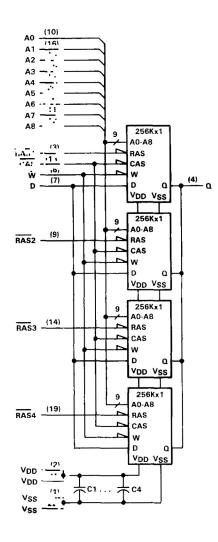


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



Dynamic RAM Modules

functional block diagram





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Voltage range for any pin except VDD and data out (see Note 1)	-1.5 V to 10 V
Voltage range on VDD supply and data out with respect to VSS	. -1 V to 7 V
Short circuit output current for any output	50 mA
Power dissipation	4 W
Operating free-air temperature range	. 0°C to 70°C
Storage temperature range	65°C to 150°C

[†]Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to VSS.

recommended operating conditions

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	4.5	5	5.5	V
VSS	Supply voltage		0		V
VIH	High-level input voltage	2.4	-	6.5	v
VIL	Low-level input voltage (see Note 2)	-1		0.8	V
TA	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

TEST TM425_FC1-12 TM425_FC1-15 PARAMETER UNIT CONDITIONS TYPT MAX MIN TYPT MIN MAX 10H = -5 mA 2.4 2.4 V VOH High-level output voltage VDD VDD Low-level output voltage 0.4 0.4 V VOL IOL = 4.2 mA 0 0 $V_1 = 0 V$ to 6.5 V, $V_{DD} = 5 V$, h. Input current (leakage) ±10 ±10 μA All other pins = 0 V $V_0 = 0.4 \text{ V to 5.5 V},$ ±10 10 Output current (leakage) ±10 μA VDD = 5 V, CAS high tc = minimum cycle, Average operating current 78 65 55 68 mA IDD1 during read or write cycle Output open[‡] After 1 memory cycle. RAS and CAS high, 18 Standby current 10 10 18 DD2 mA Output open t_c = minimum cycle, Average refresh current CAS high and RAS cycling, 180 240 160 212 IDD3 mA Output open t_{c(P)} = minimum cycle, RAS low and CAS cycling, 35 30 1004 Average page-mode current 48 43 mA Output open[‡] • • = minimum cycle, Average nibble-mode ow and CAS cycling. IDD5 32 44 27 39 mA current Output open[‡]

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

[†]All typical values are at T_A = 25 °C and nominal supply voltages.

[‡]Assuming standard operation of one device access.

	TEST		TM425_FC	1-20	UNIT
PARAMETER		CONDITIONS	MIN TYP [†]	MAX	UNIT
Vон	High-level output voltage	I _{OH} = -5 mA	2.4	VDD	V
VOL	Low-level output voltage	$I_{OL} = 4.2 \text{ mA}$	0	0.4	V
4	Input current (leakage)	$V_{I} = 0 V$ to 6.5 V, $V_{DD} = 5 V$, All other pins = 0 V		±10	μA
ю	Output current (leakage)	V _O = 0.4 V to 5.5 V V _{DD} = 5 V, CAS high		±10	μΑ
IDD1	Average operating current during read or write cycle	t _c = minimum cycle, Output open [‡]	45	58	mA
IDD2	Standby current	After 1 memory cycle, RAS and CAS high, Output open	10	18	mA
IDD3	Average refresh current	t _c = minimum cycle, CAS high and RAS cycling, Output open	140	192	mA
IDD4	Average page-mode current	t _{c(P)} = minimum cycle, RAS low and CAS cycling, Output open [‡]	25	35	mA
IDD5	Average nibble-mode current	t _{c(N)} = minimum cycle, RAS low and CAS cycling, Output open [‡]	22	32	mA

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

[†]All typical values are at $T_A = 25 \,^{\circ}$ C and nominal supply voltages.

‡Assuming standard operation of one device access.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

	PARAMETER	MIN MAX	UNIT
Ci(A)	Input capacitance, address inputs	28	pF
C _{i(D)}	Input capacitance, inputs	28	pF
Ci(RAS)	Input capacitance, inputs	8	pF
Ci(W)	Input capacitance, W input	32	pF
Ci(CAS)	Input capacitance, CAS input	32	pF
C _o (Q)	Output capacitance, data output	40	pF
Co(VDD)	Decoupling capacitance	0.4	μF



switching characteristics over recommended supply voltage range and operating free-air temperature range

	PARAMETER	TEST CONDITIONS	ALT.	TM425_	FC1-12	TM425_	FC1-15	UNIT
	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	MIN	MAX	0.111
t _{a(C)}	Access time from CAS	C _L = 100 pF, Load = 2 Series 74 TTL gates	^t CAC		60		75	ns
ta(R)	Access time from RAS	t _{RLCL} = MAX, Load = 2 Series 74 TTL gates	^t RAC		120		150	ns
^t dis(CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL gates	toff	0	30	0	30	ns

	PARAMETER	TEST CONDITIONS	ALT. SYMBOL	TM425_ MIN	FC1-20 MAX	UNIT
^t a(C)	Access time from CAS	$C_L = 100 \text{ pF},$ Load = 2 ··s 74 TTL gates	^t CAC		100	ns
t _a (R)	Access time from RAS	tRLCL = Load = 2 Series 74 TTL gates	^t RAC		2 0 0	ns
^t dis(CH)	Output disable time after CAS high	C _L = 100 pF, Load = 2 Series 74 TTL gates	toff	0	35	ns



		ALT. SYMBOL	TM425_FC1-12 MIN MAX	UNIT
+	Page-mode cycle time (read or write cycle)	tPC	1.	ns
t _{c(P)}	Page-mode cycle time (read-modify-write cycle)	tPCM	165	ns
t _{c(PM)}	Read cycle time to add the any write cycle,		230	ns
tc(rd)	Write cycle time	tRC tWC	230	ns
tc(W)	Read-write/read-modify-write cycle time	tRWC	275	ns
tc(rdW)	Pulse duration, CAS high (page mode)	tCP	50	ns
tw(CH)P	Pulse duration, CAS high (non-page mode)	tCPN	25	ns
tw(CH)	Pulse duration, CAS low [‡]		60 10.000	ns
tw(CL)		tCAS		-
tw(RH)	Pulse duration, RAS high	tRP	100	ns
tw(RL)	Pulse duration, RAS low [§]	tRAS	120 10,000	ns
tw(W)	Write pulse duration	twp	40	ns
tt	Transition times (rise and fall) for RAS and CAS	tŢ	3 50	ns
t _{su(CA)}	Column-address setup time	tASC	0	ns
t _{su(RA)}	Row-address setup time	tASR	0	ns
tsu(D)	Data setup time	tDS	0	ns
tsu(rd)	Read-command setup time	tRCS	. 0	ns
tsu(WCL)	Early write-command setup time before CAS low	twcs	o	ns
t _{su} (WCH)	Write-command setup time before CAS high	tCWL	40	ns
t _{su} (WRH)	Write-command setup time before RAS high	tRWL	40	ns
th(CLCA)	Column-address hold time after CAS low	tCAH	20	ns
th(RA)	Row-address hold time	tRAH	15	ns
th(RLCA)	Column-address hold time after RAS low	tAR	80	ns
th(CLD)	Data hold time after CAS low	tDH	35	ns
th(RLD)	Data hold time after RAS low	tDHR	95	ns
th(WLD)	Data hold time after W low	tDH	35	ns
th(CHrd)	Read-command hold time after CAS high	tRCH	0	ns
th(RHrd)	Read-command hold time after RAS high	tRRH	10	ns
th(CLW)	Write-command hold time after CAS low	tWCH	35	ns
th(RLW)	Write-command hold time after RAS low	twcR	95	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

Continued next page.

NOTE 3: Timing measurements are referenced to VIL max and VIH min.

[†]All cycle times assume $t_t = 5$ ns.

*In a read-modify-write cycle, t_{CLWL} and t_{su(WCH)} must be observed. Depending on the user's transition times, this may require additional CAS low time t_{w(CL)}). This applies to page-mode read-modify-write also.

[§]In a read-modify-write cycle, tRLWL and t_{su(WRH)} must be observed. Depending on the user's transition times, this may require additional RAS low time (t_{w(RL)}).



timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TM425_1	C1-12	UNIT
TRLCH	Delay time, RAS low to CAS high	tCSH	120		ns
^t CHRL	Delay time, CAS high to RAS low	tCRP	0		ns
tCLRH	Delay time, CAS low to RAS high	trish	60		ns
TRLCHR	Delay time, RAS low to CAS high	tCHR	25		ns
tCLRL.	Delay time, CAS low to RAS low 1	tCSR	25		ns
TRHCL	Delay time, RAS high to CAS low	tRPC	20		пs
tCLWL	Delay time, \overline{CAS} low to \overline{W} low (read-modify-write cycle only)	tCWD	60		ns
^t RLCL	Delay time, RAS low to CAS low (maximum value specified only to guarantee access time)	tRCD	30	60	ns
^t RLWL	Delay time, \overrightarrow{RAS} low to \overrightarrow{W} low (read-modify-write cycle only)	tRWD	120		ns
t _{rf}	Refresh time interval	tREF		4	ms

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min. <code>ICAS-before-RAS</code> refresh only.

timing requirements over recommended supply voltage ran	ge and operating free-air temperature range
(continued)	양 에너지 않는 것 같은 것 같

		ALT.	TM425	FC1-15	TM425	FC1-20	UNIT
	and the second of the second of the	SYMBOL	MIN	MAX	MIN	MAX	UNIT
t _{c(P)}	Page-mode cycle time (read or write cycle)	tPC	145		- · · ·		ns
tc(PM)	Page-mode cycle time (read-modify-write cycle)	^t PCM	190		245		ns
tc(rd)	Read cycle time [†]	tRC	260		330		ns
tc(W)	Write cycle time	tWC	260		330		ns
t _{c(rdW)}	Read-write/read-modify-write cycle time	TRWC	305		370		ns
tw(CH)P	Pulse duration, CAS high (page mode)	tCP	60		80		ns
tw(CH)	Pulse duration, CAS high (non-page mode)	tCPN	25		30		ns
tw(CL)	Pulse duration, CAS low [‡]	tCAS	75	10,000	100	10,000	ns
tw(RH)	Pulse duration, RAS high	tRP	100		120		ns
tw(RL)	Pulse duration, RAS low [§]	tRAS	150	10,000	200	10,000	ns
tw(W)	Write pulse duration	tWP	45		55	1	ns
t _t .	Transition times (rise and fall) for RAS and CAS	tŢ	3	50	3	50	ns
tsu(CA)	Column-address setup time	tASC	0		0		ns
tsu(RA)	Row-address setup time	tASR	0		0		ns
t _{su(D)}	Data setup time	tDS	0		0		ns
tsu(rd)	Read-command setup time	tRCS	0		0		ns
^t su(WCL)	Early write-command setup time before CAS fow	twcs	0		0		ns
t _{su} (WCH)	Write-command setup time before CAS high	tCWL	45		60	-	ns
t _{su} (WRH)	Write-command setup time before RAS high	tRWL	45		60		ns
th(CLCA)	Column-address hold time after CAS low	tCAH	25		30		ns
th(RA)	Row-address hold time	tRAH	15		20	1.1	ns
th(RLCA)	Column-address hold time after RAS low	tAR	100		130		ns
th(CLD)	Data hold time after CAS low	tDH	45		55		ns
th(RLD)	Data hold time after RAS low	^t DHR	120		155		ns
th(WLD)	Data hold time after W low	tDH	45		55		ns
th(CHrd)	Read-command hold time after CAS high	TRCH	0		0		ns
th(RHrd)	Read-command hold time after RAS high	tRRH	10		15		ns
th(CLW)	Write-command hold time after CAS low	tWCH	45		55		ns
th(RLW)	Write-command hold time after RAS low	tWCR	120	1000	155		ns

Continued next page

NOTE 3: Timing measurements are referenced to VIL max and VIH min.

[†]All cycle times assume $t_t = 5$ ns.

⁺In a read-modify-write cycle, t_{CLWL} and t_{SU(WCH)} must be observed. Depending on the user's transition times, this may require additional CAS low time t_{w(CL)}). This applies to page-mode read-modify-write also.

[§]In a read-modify-write cycle, tRLWL and t_{su(WRH)} must be observed. Depending on the user's transition times, this may require additional RAS low time (t_{w(RL)}).

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT.	TM425_FC	1-15	TM425_F	C1-20	UNIT
		SYMBOL	MIN	MAX	MIN	MAX	UNIT
TRLCH	Delay time, RAS low to CAS high	^t CSH	150		200		ns
tCHRL	Delay time, CAS high to RAS low	tCRP	0		0		ns
^t CLRH	Delay time, CAS low to RAS high	tRSH	75		100		ns
TRLCHR	Delay time, RAS low to CAS high	[‡] CHR	30		35		ns
CLRL	Delay time, CAS low to RAS low 1	tCSR	30		35		ns
TRHCL	Delay time, RAS high to CAS low 1	tRPC	20		25		ns
tCLWL	Delay time, \overline{CAS} low to \overline{W} low (read-modify-write cycle only)	tCWD	70		90		ns
^t RLCL	Delay time, RAS low to CAS low (maximum value specified only to guarantee access time)	^t RCD	30	75	30	100	ns
^t RLWL	Delay time, RAS low to W low (read-modify-write cycle only)	tRWD	145		190		ns
trf	Refresh time interval	tREF		4		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min. $\{CAS\text{-before-}RAS\text{ refresh only.}\}$

NIBBLE-MODE CYCLE

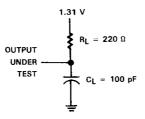
switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT.	TM425	7FC1-12	TM425	7FC1-15	TM425	7FC1-20	UNIT
		SYMBOL	MIN	MIN MAX	MIN	MAX	MIN	MAX	UNIT
ta(CN)	Nibble-mode access time from CAS	^t NCAC	T	30		40		50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

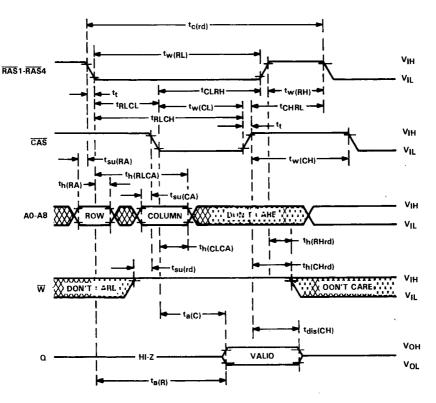
		ALT. SYMBOL	TM4257FC1-12	TM4257FC1-15	TM4257FC1-20 MIN MAX	UNIT
t _{c(N)}	Nibble-mode cycle time	tNC	00	75	90	
tc(rdWN)	Nibble-mode read-modify-write cycle time	^t NRMW	85	105	130	
tCLRHN	Nibble-mode delay time, CAS low to RAS high	^t NRSH	30	40	50	
tCLWLN	Nibble-mode delay time, CAS to W delay	tNCWD	25	30	40	
tw(CLN)	Nibble-mode pulse duration, CAS low	TNCAS	30	40	50	ns
tw(CHN)	Nibble-mode pulse duration, CAS high	^t NCP	20	25	30	
tw(CRWN)	Nibble-mode read-modify-write pulse duration, CAS low	^t NCRW	55	70	90	
t _{su} (WCHN)	Nibble-mode write command setup time before CAS high	^t NCWL	25	35	45	

PARAMETER MEASUREMENT INFORMATION

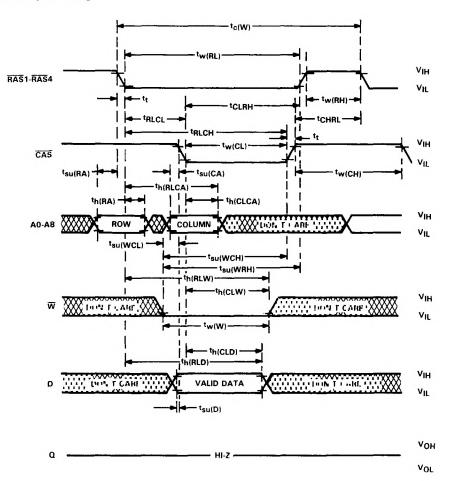




read cycle timing



early write cycle timing



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Dynamic RAM Modules



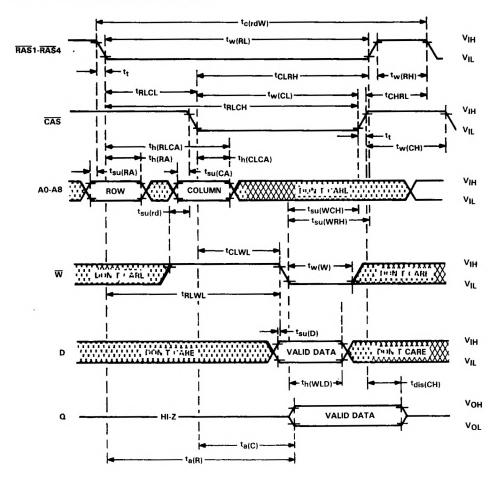
tc(W) tw(RL) ViH RAS1-RAS4 VIL tw(RH) · tı tCLRH - tRLCL ^tCHRL н **tRLCH** VIH tw(CL) CAS 11 VIL t_{su(RA)} ^tw(CH) h tsu(CA) ī th(RLCA) - t_t th(RA) th(CLCA) Чн A0-A8 RDW CDLUMN DDN 'n CARL VIL П t_{su}(WCH) t_{su}(WRH) 1 hIRLW h h(CLW) ٧н W DON F CARL XXXXX I DIN T CARL 🔆 VIL tw(W) th(WLD) 🗕 ٧н 10 N T - 40L D TON TO ARE 1 VALID DATA VIL t_{su}(D) 11 t_{en}† tdis(CH) VDH Q NDT VALID HI-Z VOL

write cycle timing

[†]The enable time (t_{en}) for a write cycle is equal in duration to the access time from CAS ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.







read-write/read-modify-write cycle timing



Dynamic RAM Modules

HON Ηľ VOL ۲H HIN ž ۲ ž ۲ ž - th(CHrd) DON'T -th(RHrd) tdis(CH) 1 tw(RH)-- tCHRL DUN F CARE TIXIT VALID th(CLCA) tCLRH-(CL) ta(C) (BU(CA) tsu(rd) COL NOTE 4: A write cycle can be intermixed with read cycles as long as the write timing specifications are not violated. tdis(CH) + XXXXXXXXXXX HA - L.NOO VALID ł トンシン th(CHrd) th(CLCA) tw(RL) - tw(CL) -ta(C) (Su(CA) (pu(rd) W(CHIP tdis(CH) COL th(CHrd) ٩ VALID * **X DON'T CARE** XXXXXXXXX C(P) (PCLCA) w(CL) (C) (C) (C) (C) su(CA (su(rd) FILCH -B(R) COL h(RLCA) -tRLCL 5 Ę DON 1 1 AF ROW th(RA)tsu(RA) + CAS **A0-A8** à ₿ RAS1-RAS4

page-mode read cycle timing

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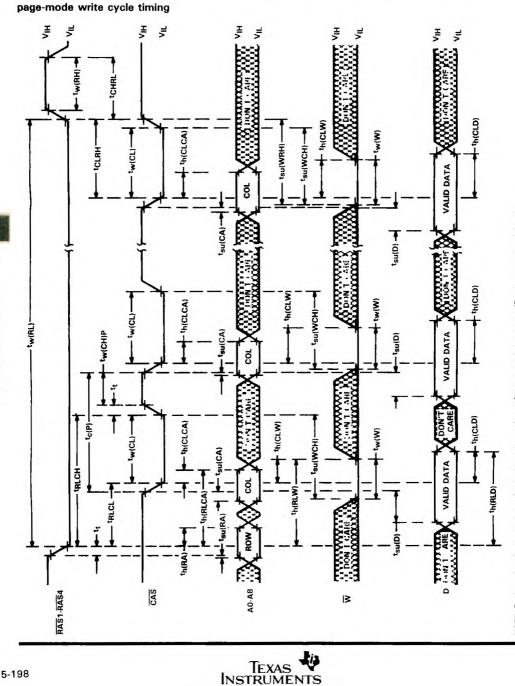
Dynamic RAM Modules

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5-197

TM4256FC1 1,048,576 BY 1-BIT DYNAMIC RAM MODULE

TM4256FC1 1,048,576 BY 1-BIT DYNAMIC RAM MODULE



5-198

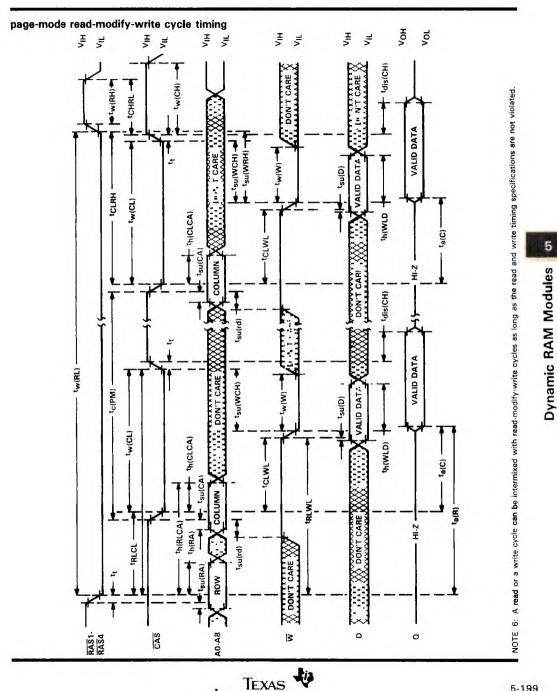
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Dynamic RAM Modules

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NOTE 5: A read cycle can be intermixed with write cycles as long as read timing specifications are not violated.

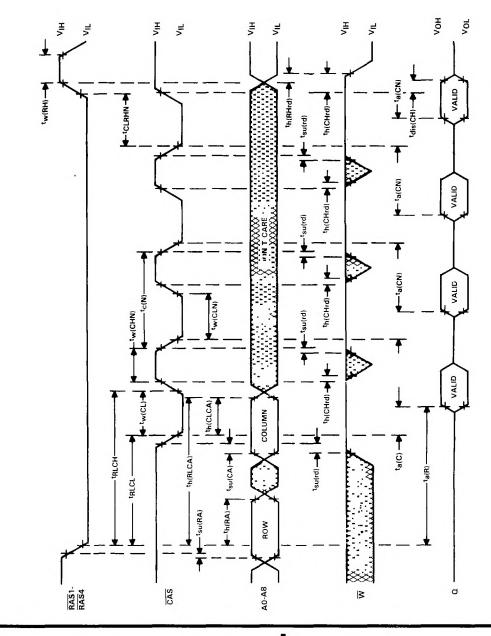
TM4256FC1 1.048.576 BY 1-BIT DYNAMIC RAM MODULE



INSTRUMENTS POST OFFICE BOX 1443 . HOUSTON, TEXAS 77001 5-199

TM4257FC1 1,048,576 BY 1-BIT DYNAMIC RAM MODULE

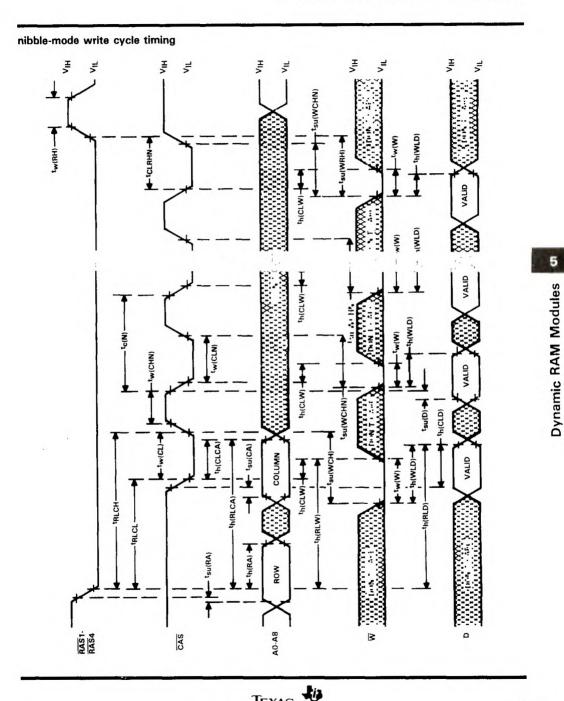
nibble-mode read cycle timing





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Dynamic RAM Modules



TM4257FC1 1,048,576 BY 1-BIT DYNAMIC RAM MODULE

5-201

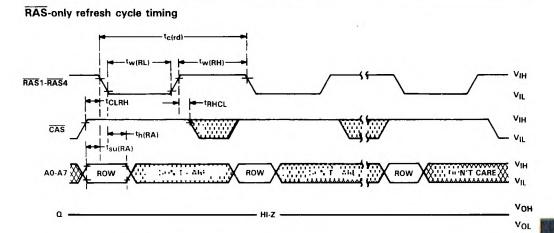
TEXAS TEXAS INSTRUMENTS POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

TM4257FC1 1,048,576 BY 1-BIT DYNAMIC RAM MODULE

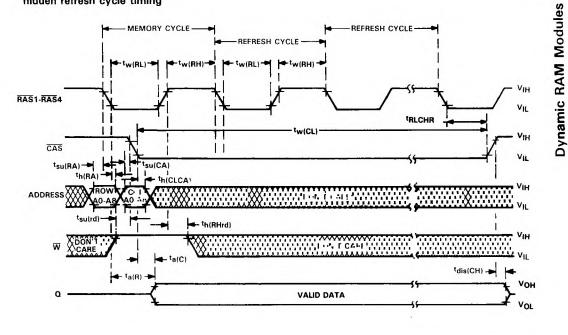
tw(RH)-٧н RAS1-RAS4 VIL -tc(rdWN) TRLCL w(CHN) tw(CL) tw(CRWN) VIH 11 CAS +t_{su(RA)} VIL th(RLCA) th(CLCA) tsu(CA) th(RA) VIH COLUMN A0-A8 ROW DON'T CARL VIL sutWCH) tsu(rd) ^tCLWLN + t_{su}(WRH) **tRLWI** 1 tw(W) VIH X w VIL tsu(D) **†CLWL** th(WLD) VIH TO N F CARE VALID D VALID VALID VIL ta(C) + tdis(CH) ta(CN) ta(R) VOH VALID ٥ VALID VALID VALID VOL

nibble-mode read-modify-write-cycle timing





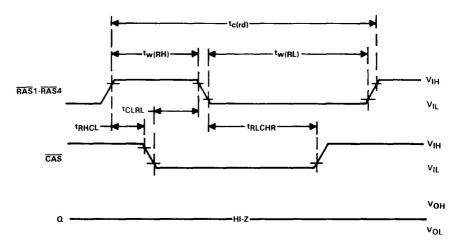
hidden refresh cycle timing



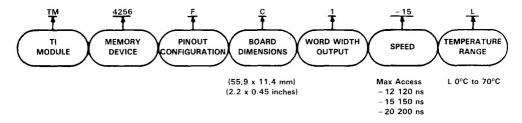


5-203

automatic (CAS-before-RAS) refresh cycle timing



TI single-in-line package nomenclature





ADVANCE INFORMATION

TM4256FL8, TM4256GU8, TM4257FL8, TM4257GU8 262,144 BY 8-BIT DYNAMIC RAM MODULES

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TM425_FL8 . . . L SINGLE-IN-LINE PACKAGE (TOP VIEW)

OCTOBER 1985 - REVISED NOVEMBER 1985

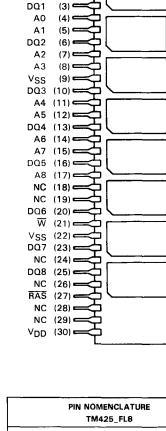
- 262,144 X 8 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
 - Pinned Module for Through-Hole Insertion (TM425_FL8)
 Leadless Module for Use with Sockets
 - (TM425_GU8)
- Utilizes Eight 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TM4258-12	120 ns	60 ns	230 ns
TM4258-15	150 ns	75 ns	260 ns
TM4258-20	200 ns	100 ns	330 ns

- Common CAS Control for Eight Common Data-In and Data-Out Lines
- Low Power Dissipation
- Operating Free-Air Temperature . . . 0 °C to 70 °C
- Downward Compatible with 64K X 8 SIP (TM4164FL8, TM4164FM8)

description

The TM425___8 series are 2048K, dynamic random-access memory modules organized as 262,144×8 bits in a 30-pin single-in-line package comprising eight TMS425_FML, 262,144×1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM425___8 has a density of ten devices per square inch (approximately 4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC



P	IN NOMENCLATURE TM425_FL8
A0-A8	Address Inputs
CAS	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
RAS	Row-Address Strobe
V _{DD}	5-V Supply
VSS	Ground
w	Write Enable

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board size, and fewer plated-through holes, a cost savings can be realized.

The TM425___8 features RAS access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation as low as 2200 mW typical operating and 100 mW typical standby for 200 ns devices.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with \overrightarrow{RAS} in order to retain data. \overrightarrow{CAS} can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM425___8 is rated for operation from 0°C to 70°C.

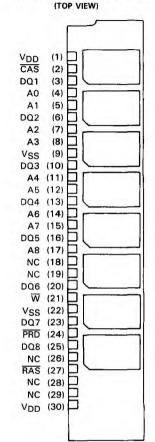
presence detect

This feature is included on the TM425_GU8 to allow for hardware p: $\cdot \cdot$ ce detection of the memory module. The $\cdot \cdot \cdot I$ pin for each module in the system should be pulled high through a pull-up resistor, resulting in a logic one when no module is present. When a module is present, PRD is a logic zero as this pin is connected to VSS on the module. PRD can only be used to detect a modules' presence, not its functionality. In a system not requiring presence detect, it is recommended that this pin be left as a no connect; this allows the use of either type of module without adverse effects.

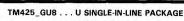
operation

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262, 144 storage cell locations on each of the eight chips. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe (\overline{RAS}). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobes. All addresses must be stable on or before the falling edges of \overline{RAS} and \overline{CAS} . \overline{RAS} is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. \overline{CAS} is used as a chip select activating the column decoder and the input and output buffers for M1-M8.



PIN NOMENCLATURE TM425_GU8					
A0-A8	Address Inputs				
CAS	Column-Address Strobe				
DQ1-DQ8	Data In/Data Out				
NC	No Connection				
PRD	Presence Detect (VSS)				
RAS	Row-Address Strobe				
VDD	5-V Supply				
Vss	Ground				
W	Write Enable				



write enable (W)

The read or write mode is selected through the write-enable (\overline{W}) input. A logic high on the \overline{W} input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM4?^F ___8 dictates the use of early write cycles to prevent contention on DQ. When \overline{W} goes low prior to $\ddot{\Box}$, the data outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ8)

Data is written during a write cycle. The falling edge of \overline{CAS} strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, \overline{W} is brought low prior to \overline{CAS} and the data is strobed in by \overline{CAS} with setup and hold times referenced to this signal.

data out (DQ1-DQ8)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state until \overrightarrow{CAS} is brought low. In a read \cdots ie the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of \overrightarrow{t} as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while \overrightarrow{CAS} is low: \overrightarrow{CAS} going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state, a necessity due to the common I/O feature of the TM425___8.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless \overline{CAS} is applied, the \overline{RAS} -only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with \overline{RAS} causes all bits in each row to be refreshed. \overline{CAS} can remain high (inactive) for this refresh sequence to conserve power.

CAS-before-RAS refresh

The \overline{CAS} -before- \overline{RAS} refresh is utilized by bringing \overline{CAS} low earlier than \overline{RAS} (see parameter t_{CLRL}) and holding it low after \overline{RAS} falls (see parameter t_{RLCHR}). For successive \overline{CAS} -before- \overline{RAS} refresh cycles, \overline{CAS} can remain low while cycling \overline{RAS} . The external address is ignored and the refresh address is generated internally.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding CAS at VIL after a read operation and cycling RAS after a specified precharge period, similar to a ''RAS-only'' refresh cycle. The external address is also ignored during the hidden refresh cycles.

page-mode (TM4256__8)

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated.



nibble mode (TM4257__8)

Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. The next sequential nibble bits can be read or written by cycling \overrightarrow{CAS} while \overrightarrow{RAS} remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Column A8 and row A8 (CA8, RA8) provide the two binary bits for initial selection of the nibble addresses. Thereafter, the falling edge of \overrightarrow{CAS} will access the next bit of the circular 4-bit nibble in the following sequence:



In nibble-mode, all normal memory operations (read, write, or ready-modify-write) may be performed in any desired combination.

power up

To achieve proper operation, an initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles.

single-in-line package and components

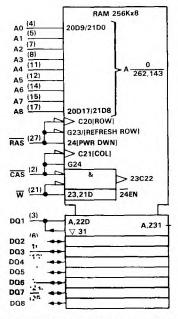
PC substrate: 0,79 mm (0.031 inch) minimum thickness

Bypass capacitors: Multilayer ceramic

Leads: Tin/lead solder coated over phosphor-bronze

Contact area for socketable devices: Nickel plate and solder plate on top of copper

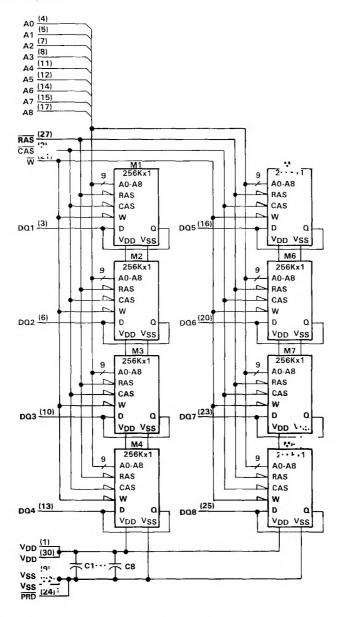
logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



functional block diagram



[†]TM425_GU8 only.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Voltage range for any pin except VDD and data out (see Note 1) 1.5 V to 10 V
Voltage range on VDD supply and data out with respect to VSS $\dots \dots $
Short circuit output current for any output
Power dissipation
Operating free-air temperature range 0°C to 70°C
Storage temperature range

[†] Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to VSS.

recommended operating conditions

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	4.5	5	5.5	V
Vss	Supply voltage		0		V
VIH	High-level input voltage	2.4		6.5	V
VIL	Low-level input voltage (see Note 2)	-1		0.8	V
TA	Operating free-air tamperature	0	_	70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

	PARAMETER	TEST	TM	425	8-12	TM	425	8-15	
	FARAMEICR	CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VOH	High-level output voltage	IOH = -5 mA	2.4	_	VDD	2.4		VDD	v
VOL	Low-level output voltage	ioL = 4.2 mA	0		0.4	0		0.4	V
łj	Input current (leakage)	$V_1 \approx 0 V$ to 6.5 V, $V_{DD} = 5 V$, All other pins = 0 V			±10			± 10	μ A
ю	Output current (leakage)	V _O = 0.4 V to 5.5 V, V _{DD} = 5 V, CAS high			±10			±10	μA
^I DD1 [‡]	Average operating current during read or write cycle	t _C = minimum cycle, All outputs open		520	624		440	544	mA
¹ 0D2 [‡]	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open		20	36		20	36	mA
IDD3‡	Average refresh current	t _c = minimum cycle, CAS high and RAS cycling, All outputs open		360	480		320	424	mA
	Average page-mode current	t _{c(P)} = minimum cycle, RAS low and CAS cycling, All outputs open		280	384		240	344	mA
¹ DD5 [‡]	Average nibble-mode current	$t_{C(N)}$ = minimum cycle, RAS low and CAS cycling, All outputs open		256	352		216	312	mA

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

[†]All typical values are at $T_A = 25 \,^{\circ}C$ and nominal supply voltages.

¹IDD1-IDD5 are measured with M1-M8 in the same mode (i.e., operating, standby, refresh, page mode, nibble mode).



PARAMETER		TEST		8-20	
		CONDITIONS	MIN TYP [†] MA		
VOH	High-level output voltage	IOH = -5 mA	2.4	VDD	V
VOL	Low-level output voltage	IOL = 4.2 mA	0	0.4	۷
կ	Input current (leakage)	$V_{I} = 0 V$ to 6.5 V, $V_{DD} = 5 V$, All other pins = 0 V		± 10	μА
10	Output current (leakage)	$V_0 = 0.4 V$ to 5.5 V, $V_{DD} = 5 V$, CAS high		±10	μA
IDD1 [‡]	Average operating current during read or write cycle	t _c = minimum cycle, All outputs open	360	464	mA
	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open	20	36	mA
IDD3 [‡]	Average refresh current	t _c = minimum cγcle, CAS high and RAS cycling, All outputs open	280	384	mA
	Average page-mode current	t _{c(P)} = minimum cycle, RAS low and CAS cycling, All outputs open	200	280	mA
DD5 [‡]	Average nibble-mode current	t _{c(N)} = minimum cycle, RAS low and CAS cycling, All outputs open	176	256	mA

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

[†]All typical values are at $T_A = 25$ °C and nominal supply voltages.

*IDD1-IDD5 are measured with M1-M8 in the same mode (i.e., operating, standby, refresh, page mode, nibble mode).

capacitance over recommended supply voltage range and operating free-air temperature range, $f\,=\,1\,\,\text{MHz}$

	PARAMETER	MIN MAX	UNIT
Ci(A)	Input capacitance, address inputs	56	pF
Ci(DQ)	Input capacitance, data inputs	lbs	pF
Ci(RAS)	Input capacitance, RAS input	04	pF
Ci(W)	Input capacitance, W input	64	pF
Ci(CAS)	Input capacitance, CAS input	64	pF
Co(VDD)	Decoupling capacitance	0.8	μF

5

Additional information on these products can be obtained from the factory as it becomes available.



switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		Traz conditions	ALT.	TM425_	8-12	TM425_	8-15	UNIT
		TEST CONDITIONS	SYMBOL	MIN	MAX	MIN	MAX	UNIT
t _a (C)	Access time from CAS	$C_L = 100 \text{ pF},$ Load = 2 Series 74 TTL gates	tCAC		60		75	ns
t _{a(R)}	Access time from RAS	$t_{RLCL} = MAX,$ Load = 2 Series 74 TTL gates	^t RAC		120		150	ns
^t dis(CH)	Output disable time after CAS high	$C_L = 100 \text{ pF},$ Load = 2 Series 74 TTL gates	tOFF	0	35	0	35	ns

PARAMETER		TEST CONDITIONS	ALT.	TM4258-20		UNIT
		SYMBO		MIN	MAX	
ta(C)	Access time from CAS	$C_L = 100 \text{ pF},$ Load = 2 Series 74 TTL gates	^t CAC		100	ns
^t a(R)	Access time from RAS	t _{RLCL} = MAX, Load = 2 Series 74 TTL gates	^t RAC		200	ns
^t dis(CH)	Output disable time after CAS high	CL = 100 pF, Load = 2 Series 74 TTL gates	tOFF	0	35	ns



		ALT. SYMBOL	TM4258-12 MIN MAX	UNIT
tc(P)	Page-mode cycle time (read or write cycle)	tPC	120	ns
tc(rd)	Read cycle time [†]	tRC	230	ns
tc(W)	Write cycle time	tWC	230	ns
tw(CH)P	Pulse duration, CAS high (page mode)	tCP	50	ns
tw(CH)	Pulse duration, CAS high (non-page mode)	tCPN	25	ns
tw(CL)	Pulse duration, CAS low	tCAS	60 10,000	ns
tw(RH)	Pulse duration, RAS high (precharge time)	tRP	100	ns
tw(RL)	Pulse duration, RAS low	tRAS	120 10,000	ns
tw(W)	Write pulse duration	twp	40	ns
t _t	Transition times (rise and fall) for RAS and CAS	tŢ	3 50	ns
t _{su} (CA)	Column-address setup time	tASC	0	ns
t _{su(RA)}	Row-address setup time	tASR	0	ns
t _{su(D)}	Data setup time	tDS	0	ns
tsu(rd)	Read-command setup time	tRCS	0	ns
tsu(WCL)	Early write-command setup time before CAS low	twcs	0	ns
t _{su} (WCH)	Write-command setup time before CAS high	tCWL	40	ns
t _{su} (WRH)	Write-command setup time before RAS high	tRWL	40	ns
th(CLCA)	Column-address hold time after CAS low	tCAH	20	ns
th(RA)	Row-address hold time	tRAH	15	ns
th(RLCA)	Column-address hold time after RAS low	tAR	80	ns
th(CLD)	Data hold time after CAS low	tDH	35	ns
th(RLD)	Data hold time after RAS low	^t DHR	95	ns
th(CHrd)	Read-command hold time after CAS high	tRCH	0	ns
th(RHrd)	Read-command hold time after RAS high	tRRH	10	ns
th(CLW)	Write-command hold time after CAS low	tWCH	35	ns
th(RLW)	Write-command hold time after RAS low	twcr	95	ns
RLCH	Delay time, RAS low to CAS high	tCSH	120	ns
tCHRL	Delay time, CAS high to RAS low	tCRP	0	ns
tCLRH	Delay time, CAS low to hAS nigh	tRSH	60	ns
TRLCHR	Delay time, RAS low to CAS high [‡]	tCHR	25	ns
tCLRL	Delay time, CAS low to RAS low #	tCSR	25	ns
TRHCL	Delay time, RAS high to low t	tRPC	20	ns
TRLCL	Delay time, ow to ow (maximum value specified only to guarantee access time)	tRCD	30 60	ns
t _{rf}	Refresh time interval	tREF	4	ms

Dynamic RAM Modules

5

NOTE 3: Timing measurements are referenced to VIL max and VIH min.

[†]All cycle times assume $t_t = 5$ ns. [‡]CAS-before-RAS refresh only.



		ALT.	TM425_		TM425		UNIT
		SYMBOL	MIN	MAA	MIN	MAX	
tc(P)	Page-mode cycle time (read or write cycle)	tPC	145		190		ns
tc(rd)	Read cycle time [†]	tRC	260	_	330		ns
t _{c(W)}	Write cycle time	tWC	260		330		ns
tw(CH)P	Pulse duration, CAS high (page mode)	tCP	60		80		ns
tw(CH)	Pulse duration, CAS high (non-page mode)	^t CPN	25		30		ns
tw(CL)	Pulse duration, CAS low	tCAS	75	10,000	100	10,000	ns
tw(RH)	Pulse duration, RAS high (precharge time)	tRP	100		120		ns
tw(RL)	Pulse duration, RAS low	tRAS	150	10,000	200	10,000	ns
tw(W)	Write pulse duration	tWP	45		55		ns
tt	Transition times (rise and fall) for RAS and CAS	tŢ	3	50	3	50	ns
t _{su(CA)}	Column-address setup time	tASC	0		0		ns
t _{su(RA)}	Row-address setup time	tASR	. 0		0		ns
t _{su(D)}	Data setup time	tDS	0		0		ns
tsu(rd)	Read-command setup time	tRCS	0	_	0		ns
t _{su} (WCL)	Early write-command setup time before CAS low	twcs	0		0		ns
t _{su} (WCH)	Write-command setup time before CAS high	tCWL	45		60		ns
t _{su} (WRH)	Write-command setup time before RAS high	tRWL	45		60		ns
th(CLCA)	Column-address hold time after CAS low	tCAH	25		30		ns
th(RA)	Row-address hold time	^t RAH	15		20		ns
th(RLCA)	Column-address hold time after RAS low	tAR	100		130		ns
th(CLD)	Data hold time after CAS low	tDH	45		55		ns
th(RLD)	Data hold time after RAS low	tDHR	120		155		ns
th(CHrd)	Read-command hold time after CAS high	tRCH	0		0	2	ns
th(RHrd)	Read-command hold time after RAS high	tRBH	10	1000	15		ns
th(CLW)	Write-command hold time after CAS low	tWCH	45	5.00	55		ns
th(RLW)	Write-command hold time after RAS low	tWCR	120		155		ns
TRLCH	Delay time, RAS low to CAS high	tCSH	150		200		ns
tCHRL	Delay time, CAS high to RAS low	tCRP	0		0		ns
tCLRH	Delay time, CAS low to RAS high	tRSH	75		100		ns
TRLCHR	Delay time, RAS low to CAS high ‡	tCHR	30		35		ns
	Delay time, CAS low to RAS low [‡]		30	 	35		ns
tCLRL	Delay time, RAS high to CAS low [‡]	tCSR	20		25		ns
TRHCL		^t RPC			25		ns
^t RLCL	Delay time, RAS low to CAS low (maximum value specified only to guarantee access time)	^t RCD	30	75	30	100	ns
trf	Refresh time interval	TREF		4		4	ms

NOTE 3: Timing measurements are referenced to VIL max and VIH min.

[†]All cycle times assume $t_t = 5$ ns. [‡]CAS-before-RAS refresh only.



NIBBLE-MODE CYCLE

switching characteristics over recommended supply voltage range and operating free-air temperature range

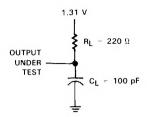
PARAMETER		ALT.	TM425	78-12	TM425	78-15	TM425	78-20	UNIT
	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	
ta(CN)	Nibble-mode access time from CAS	^t NCAC		30		40		50	ПS

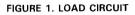
timing requirements over recommended supply voltage range and operating free-air temperature range

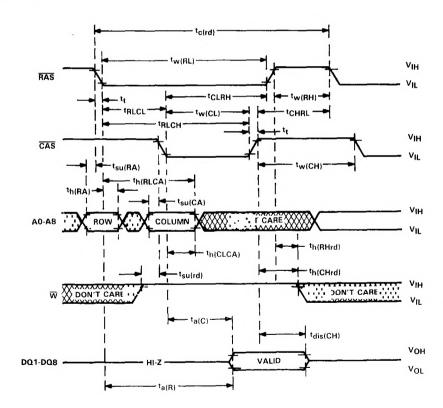
		ALT. SYMBOL	TM4257		TM4257	8-15	TM4257	8-20	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	•
tc(N)	Nibble-mode cycle time	^t NC	60		75		90		-
^t CLRHN	Nibble-mode delay time, CAS low to RAS high	^t NRSH	30		40		50		
tCLWLN	Nibble-mode delay time, \overline{CAS} to \overline{W} delay	^t NCWD	25		30		40		
tw(CLN)	Nibble-mode pulse duration, CAS low	^t NCAS	30		40		50		ns
tw(CHN)	Nibble-mode pulse duration, CAS high	^t NCP	20		25		30		
t _{su} (WCHN)	Nibble-mode write command setup time before CAS high	^t NCWL	25		35		45		



PARAMETER MEASUREMENT INFORMATION



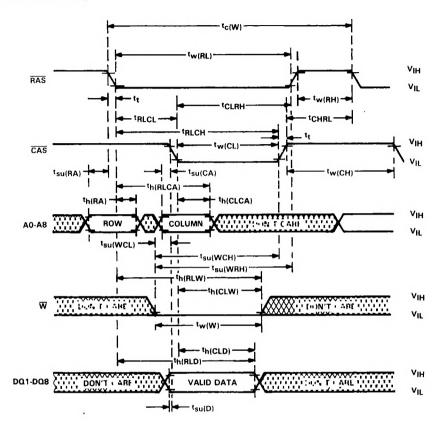




read cycle timing



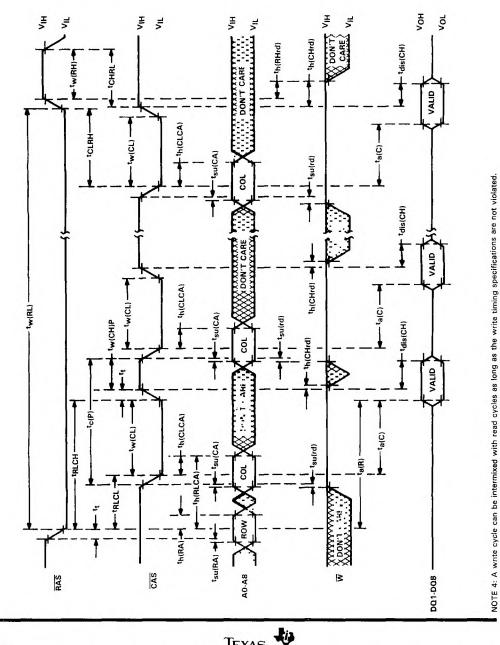
early write cycle timing





TM4256FL8, TM4256GU8 262,144 BY 8-BIT DYNAMIC RAM MODULES

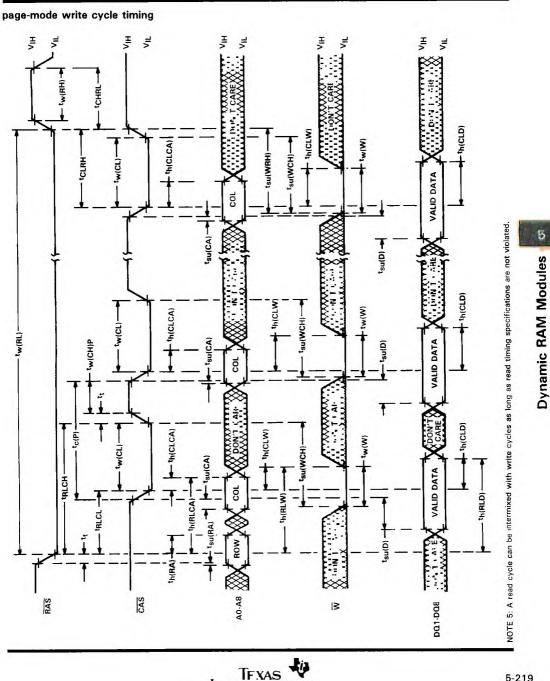
page-mode read cycle timing



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TM4256FL8, TM4256GU8 262,144 BY 8-BIT DYNAMIC RAM MODULES

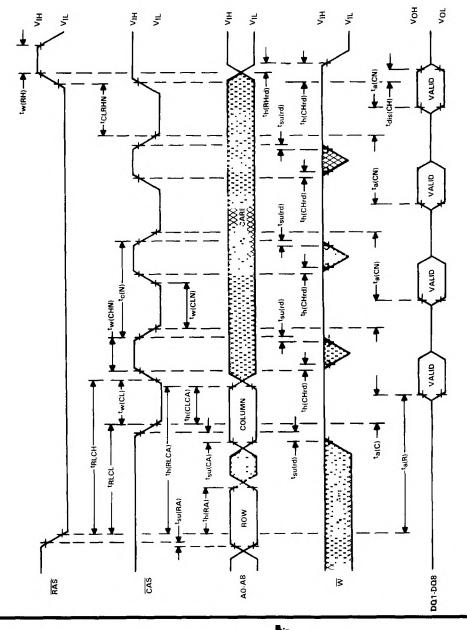


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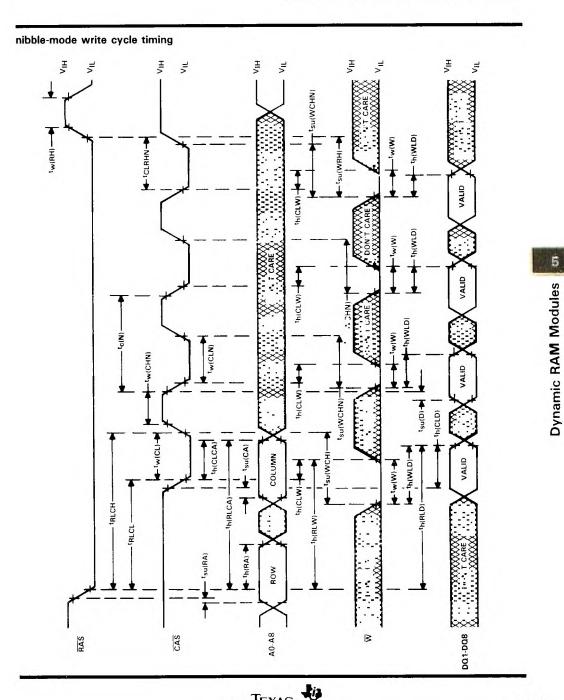
TM4257FL8, TM4257GU8 262,144 BY 8-BIT DYNAMIC RAM MODULES

nibble-mode read cycle timing





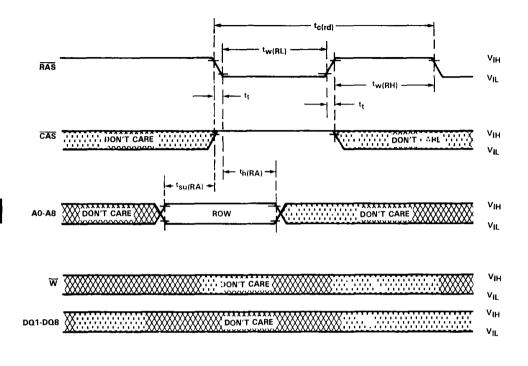
Dynamic RAM Modules



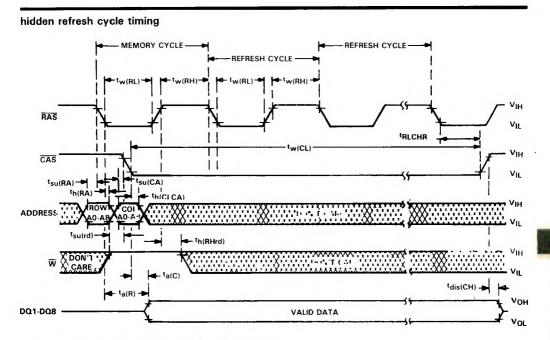
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TEXAS

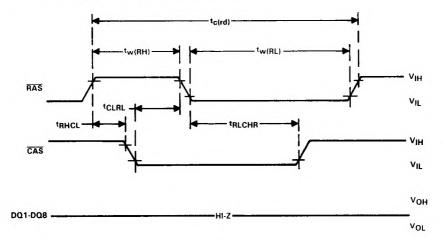
RAS-only refresh timing







automatic (CAS-before-RAS) refresh cycle timing





TI single-in-line package nomenclature[†] 4256 - 15 TM Ŧ 8 Ŧ тι MEMORY PINOUT BOARD WORD WIDTH TEMPERATURE SPEED MODULE DEVICE CONFIGURATION DIMENSIONS OUTPUT RANGE **F** Version L Package L 0°C to 70°C Max Access Pin 24-No Connect (76,2 x 16,5 mm) -12 120 ns G Version (3.0 x 0.65 inches) - 15 150 ns Pin 24-PRD U Package - 20 200 ns (88,9 x 16,5 mm) (3.5 x 0.65 inches)

[†]The F pinout configuration designator is used when specifying the L package; the G pinout configuration version designator is used when specifying the U package.



ADVANCE INFORMATION

TM4256GP8, TM4256GV8 262,144 BY 8-BIT DYNAMIC RAM MODULES

OCTOBER 1985 - REVISED NOVEMBER 1985

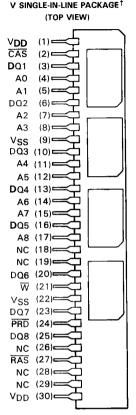
- 262,144 X 8 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
 —Pinned Module for Through-Hole Insertion (TM4256GV8)
 —Leadless Module for Use with
- Sockets (TM4256GP8)
- Low Profile, Double-Side Mount . . . 0.45'' Height
- Utilizes Eight 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

	ACCESS TIME ROW ADDRESS	ACCESS TIME COLUMN ADDRESS		READ- MODIFY- WRITE- CYCLE
	(MAX)	(MAX)	(MIN)	(MIN)
TM\$4256-12	120 ns	60 ns	230 ns	270 ns
TMS4256-15	150 ns	75 ns	260 ns	305 ns
TMS4256-20	200 ns	1 00 ns	330 ns	370 ns

- Common CAS Control with Common Data-In and Data-Out Lines
- Low Power Dissipation
- Operating Free-Air Temperature . . . 0 °C to 70 °C
- Upward Compatible with Planned 1 Meg DRAM Family (Height and Length May Increase)

description

The TM4256G_8 series are 2048K, dynamic random-access memory modules organized as 262,144 \times 8 bits in a 30-pin single-in-line package comprising eight TMS4256FML, 262,144 \times 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with eight 0.2 μ F decoupling capacitors. Each TMS4256FML is described in the data sheet and is fully electrically tested



Dynamic RAM Modules

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[†]TM4256GV8 package is shown.

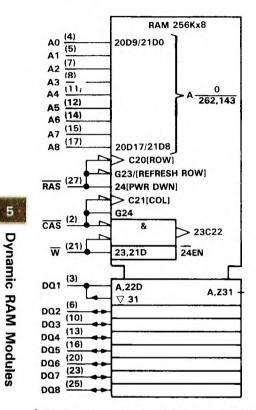
Р	PIN NOMENCLATURE			
A0-A8	Address Inputs			
CAS	Column-Address Strobe			
DQ1-DQ8 Data In/Data Out				
NC No Connection				
PRD Presence Detect				
RAS Row-Address Strobe				
VDD 5-V Supply				
V _{SS}	Ground			
₩	Write Enable			

and processed according to TI's MIL-STD-883B (as amended for commercial applications) flows prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed. The module is rated for operation from 0 °C to 70 °C.



TM4256GP8, TM4256GV8 262.144 BY 8-BIT DYNAMIC RAM MODULES

logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

A0 (4) A1 (5) A2 (7) A3 (8) A4 A5 A6 -A7 (15) A8 (17) P.57: (27) (21) v 256Kx1 256Kx1 9 A0-A8 A0-A8 RAC RAC CAS CAS w w DQ5 (16) DQ1 (3) D D Q 0 VDD VSS VDD VSS 256Kx1 A0-A8 Au-Aa RAS RAS CAS CAS w w DQ6⁽²⁰⁾ DQ2 (6) D D c VDD VSS VDD VSS 256Kx 80-0A AD.AH RAS RAS CAS CAS w w DQ3 (10) DQ7⁽²³⁾ D n n a VDD VSS VDD VSS 256Kx 256Kx 9 q A0-A8 A0-A8 RAS RAS CAS CAS w DQ8⁽²⁵⁾ w DQ4 (13) D D ۵ 0 VDD VSS VDD VSS VDD (1) VDD (30) Vss (9) Vss (22) **C8** C1 古 PRD (24)

functional block diagram



Dynamic RAM Modules

5-226

operation

The TM4256G_8 operates as eight TMS4256s connected as shown in the functional block diagram. Refer to the TMS4256 data sheet for details of its operation. The common I/O feature of the TM4256G_8 requires the use of early-write cycles to prevent contention on D and Q.

presence detect

This feature allows for hardware presence detection of the memory module. The PRD pin for each module in the system should be pulled high through a pull-up resistor, resulting in a logic one when no module is present. When a module is present, PRD is a logic zero as this pin is connected to V_{SS} on the module. PRD can only be used to detect a modules' presence, not its functionality. In a system not requiring presence detect, it is recommended that this pin be left as a no connect; this allows the use of either type of module without adverse effects.

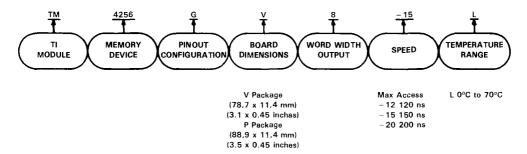
specifications

For TMS4256 electrical specifications, refer to the TMS4256 data sheet. The common I/O feature of the TM4256G_8 dictates the use of early-write cycles to prevent contention on D and Q.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness Bypass capacitors: Multilayer ceramic Leads: Tin/lead solder coated over phosphor-bronze Contact area for socketable devices: Nickel plate and solder plate on top of copper

TI single-in-line package nomenclature





G Dynamic RAM Modules

ADVANCE INFORMATION

TM4256GP9, TM4256GV9 262,144 BY 9-BIT DYNAMIC RAM MODULES

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1985 - REVISED NOVEMBER 1985

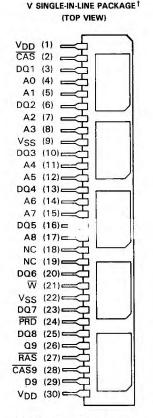
- 262,144 X 9 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP) — Pinned Module for Through-Hole Insertion (TM4256GV9)
 - -Leadless Module for Use with Sockets (TM4256GP9)
- Low Profile, Double-Side Mount . . . 0.45" Height
- Utilizes Nine 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

	ACCESS TIME ROW	ACCESS TIME COLUMN	READ OR WRITE	READ- MODIFY- WRITE
	ADDRESS (MAX)	ADDRESS (MAX)	(MIN)	CYCLE (MIN)
TMS4256-12	120 ns	60 ns	230 ns	270 ns
TMS4256-15	150 ns	75 ns	260 ns	305 ns
TMS4256-20	200 ns	100 ns	330 ns	370 ns

- Common CAS Control for Eight Common Data-In and Data-Out Lines
- Separate CAS Control for One Separate Pair of Data-In and Data-Out Lines
- Low Power Dissipation
- Operating Free-Air Temperature . . . 0 °C to 70 °C
- Upward Compatible with Planned
 1 Meg DRAM Family (Height and Length May Increase)

description

The TM4256G_9 series is a 2304K, dynamic random-access memory module organized as 262,144 \times 9 bits [bit nine (D9, Q9) is generally used for parity and is controlled by CAS9] in a 30-pin single-in-line package comprising nine TMS4256FML, 262,144 \times 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with nine 0.2 μ F



[†]TM4256GV9 package is shown.

PI	N NOMENCLATURE
A0-A8	Address Inputs
CAS, CAS9	Column-Address Strobes
DQ1-DQ8	Data In/Data Out
D9	Data in
NC	No Connection
PRD	Presence Detect
09	Data Out
RAS	Row-Address Strobe
VDD	5-V Supply
Vss	Ground
W	Write Enable

decoupling capacitors mounted beneath the chip carriers. Each TMS4256FML is described in the data sheet and is fully electrically tested and processed according to TI's MIL-STD-883B (as amended for commercial

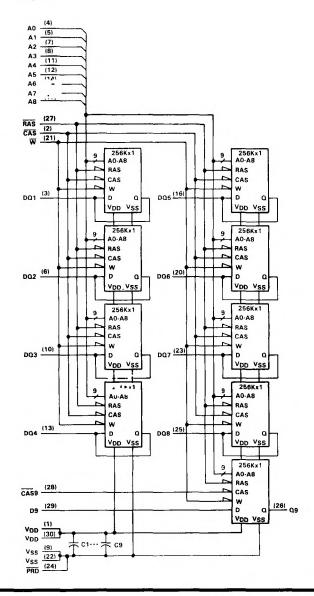
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TM4256GP9, TM4256GV9 262,144 BY 9-BIT DYNAMIC RAM MODULES

applications) flows prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed. The module is rated for operation from 0°C to 70°C.

functional block diagram





operation

The TM4256G_9 operates as nine TMS4256s connected as shown in the functional block diagram. Refer to the TMS4256 data sheet for details of its operation. The common I/O feature of the TM4256G_9 dictates the use of early-write cycles to prevent contention on D and Q.

specifications

For TMS4256 electrical specifications, refer to the TMS4256 data sheet. The common I/O feature of the TM4256G_9 dictates the use of early-write cycles to prevent contention on D and Q.

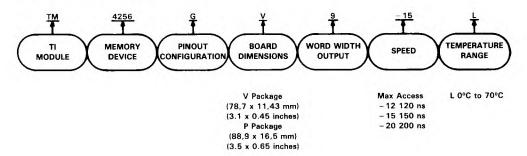
presence detect

This feature allows for hardware presence detection of the memory module. The PRD pin for each module in the system should be pulled high through a pull-up resistor, resulting in a logic one when no module is present. When a module is present, PRD is a logic zero as this pin is connected to VSS on the module. PRD can only be used to detect a modules' presence, not its functionality. In a system not requiring presence detect, it is recommended that this pin be left as a no connect; this allows the use of either type of module without adverse effects.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness Bypass capacitors: Multilayer ceramic Leads: Tin/lead solder coated over phosphor-bronze Contact area for socketable devices: Nickel plate and solder plate on top of copper

TI single-in-line package nomenclature





Dynamic RAM Modules



ADVANCE INFORMATION

TM4256HE4 524,288 BY 4-BIT DYNAMIC RAM MODULE

E SINGLE-IN-LINE PACKAGE

SEPTEMBER 1985 - REVISED NC

12

- 524,288 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- 24-Pin Single-in-Line Package (SIP)
- Utilizes Eight 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

	ACCESS TIME BOW	ACCESS TIME COLUMN	READ OR WRITE	READ- MODIFY- WRITE
	ADDRESS (MAX)	ADDRESS (MAX)	CYCLE (MIN)	CYCLE (MIN)
TMS4256-12	120 ns	60 ns	230 ns	270 ns
TMS4256-15	150 ns	75 ns	260 ns	305 ns
TMS4256-20	200 ns	100 ns	330 ns	370 ns

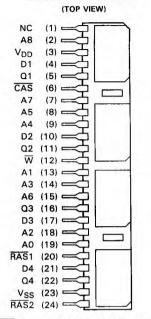
- Common CAS Control with Separate Data-In and Data-Out Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4256HE4-12	2600 mW	100 mW
TM4256HE4-15	2400 mW	100 mW
TM4256HE4-20	1800 mW	100 mW

 Operating Free-Air Temperature . . . 0 °C to 70 °C

description

The TM4256HE4 is a 2048K, dynamic randomaccess memory module organized as 524,288 X 4 bits in a 24-pin single-in-line package (SIP) comprising eight TMS4256FML, 262,144 X 1 bit dynamic RAM's in 18-lead plastic-chip carriers mounted on both sides of a substrate together with four 0.2 μ F decoupling capacitors. The on-board capacitors eliminate the need for



TRAS1 is the row-address strobe for side 1, and RAS2 is the row-address strobe for side 2. Side 1 is shown in top view.

PIN N	OMENCLATURE
A0-A8	Address Inputs
CAS	Column-Address Strobe
D1-D4	Data Inputs
NC	No Connection
Q1-Q4	Data Outputs
RAS1, RAS2	Row-Address Strobes
VDD	5-V Supply
VSS	Ground
$\overline{\mathbf{w}}$	Write Enable

bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.475 inch board spacing, the TM4256HE4 has a density of seven devices per square inch (approximately 2.8X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

The TM4256HE4 is organized as two banks of 256K X 4 selected by $\overline{RAS1}$, $\overline{RAS2}$; \overline{CAS} and \overline{W} which are common to all devices. The D and Q signals are common to pairs of devices on opposing sides of the substrate. This configuration requires that only one \overline{RAS} signal be active during a read or write cycle to prevent data bus contention or writing erroneous data. On refresh cycles (\overline{CAS} high), $\overline{RAS1}$ and $\overline{RAS2}$ can be low at the same time.

TEYAS.

INSTRUMENTS

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Each TMS4256FML is described in the TMS4256 data sheet and is fully electrically tested and processed according to TI's MIL-STD-883B (as amended for commercial applications) flows prior to assembly. After assembly onto the substrate, a further set of electrical tests is performed.

operation

The TM4256HE4 operates as eight TMS4256s connected as shown in the functional block diagram. Refer to the TMS4256 data sheet for details of its operation.

specifications

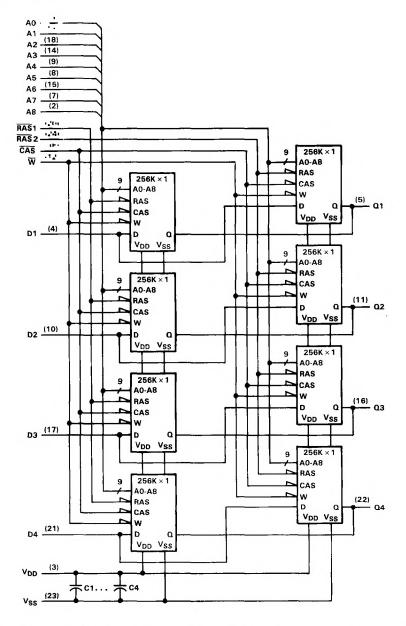
For TMS4256 electrical specifications, refer to the TMS4256 data sheet.

single-in-line package and components

PC substrate: 1,14 mm (0.045 inch) minimum thickness Bypass capacitors: Multilayer ceramic Leads: Tin/lead solder coated over phosphor-bronze

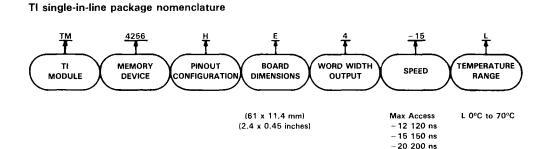


functional block diagram





TM4256HE4 524,288 BY 4-BIT DYNAMIC RAM MODULE





ADVANCE INFORMATION

TM4416KU8 16,384 BY 8-BIT DYNAMIC RAM MODULE

SEPTEMBER 1985 - REVISED NOVEMBER 1985

- 16,384 X 8 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
- Utilizes Two 16K X 4 Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

	ACCESS	ACCESS	READ
	TIME	TIME	OR
	ROW	COLUMN	WRITE
	ADDRESS	ADDRESS	CYCLE
	(MAX)	(MAX)	(MIN)
TM4416KU8-12	120 ns	70 ns	230 ns
TM4416KU8-15	150 ns	80 ns	260 ns

Low Power Dissipation:

	OPERATING	STANDBY
	(TYP)	(TYP)
TM4416KU8-12	400 mW	30 mW
TM4416KU8-15	350 mW	30 mW

 Operating Free-Air Temperature . . . 0 °C to 70 °C

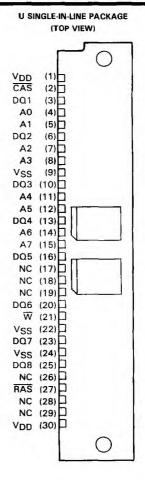
description

The TM4416KU8 is a 128K, dynamic randomaccess memory module organized as 16,384 × 8 bits in a 30-pin single-in-line package comprising two TMS4416FPL, 16,384 × 4 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with two 0.2 μ F decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance.

operation

address (A0 through A7)

Fourteen address bits are required to decode 1 of 16,384 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe (\overline{RAS}). Then the six column-address bits are set up on pins A1 through A6 and latched onto the



5

P	IN NOMENCLATURE
A0-A7	Address Inputs
CAS	Column-Address Strobe
DQ1-DQ8	Data in/Data Out
NC	No Connection
RAS	Row-Address Strobe
VDD	5-V Supply
Vss	Ground
W	Write Enable

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chip by the column-address strobe (\overline{CAS}). All addresses must be stable on or before the falling edges of \overline{RAS} and \overline{CAS} . \overline{RAS} is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. \overline{CAS} is used as a chip select activating the column decoder and the input and output buffers.

write enable (W)

The read or write mode is selected through the write-enable (\overline{W}) input. A logic high on the \overline{W} input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The grounded output-enable (\overline{G}) dictates the use of early write cycles to prevent contention on DQ. When \overline{W} goes low prior to \overline{CAS} , the data outputs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ8)

Data is written during a write cycle. The falling edge of \overline{CAS} strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, \overline{W} is brought low prior to \overline{CAS} and the data is strobed in by \overline{CAS} with setup and hold times referenced to this signal.

data out (DQ1-DQ8)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of \overline{CAS} as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remain valid while \overline{CAS} is low; \overline{CAS} going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state. In the early write cycle, the outputs are always in the high-impedance state, a necessity due to the grounded output enable.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless \overrightarrow{CAS} is applied, the \overrightarrow{RAS} -only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with \overrightarrow{RAS} causes all bits in each row to be refreshed. \overrightarrow{CAS} can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 64 column locations on a single module, the row address and RAS are applied to multiple modules. CAS is then decoded to select the proper module.

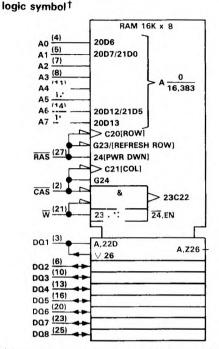
power up

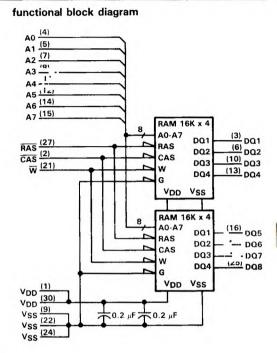
After power up, the power supply must remain at its steady-state value for 1 ms. In addition, the \overline{RAS} input \cdots remain high for 100 μ s immediately prior to initialization. Initialization consists of performing eight \overline{RAS} cycles before proper device operation is achieved.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness 8ypass capacitor: Multilayer ceramic Contact area for socketable devices: Nickel plate and solder plate on top of copper







[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

/oltage range for any pin except VDD and data out (see Note 1)	-1.5 V to 10 V
/oltage range for VDD supply and data out with respect to VSS	1 V to 6 V
Short circuit output current	50 mA
Power dissipation	2 W
Dperating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

¹Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to VSS.

 Additional information concerning the handling of ESD sensitive devices is available in a document entitled "Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies" in Section 12.

recommended operating conditions

			MIN	NOM	MAX	UNIT
VDD	Supply voltage		4.5	5	5.5	V
Vss	Supply voltage		3	0		V
	VIH High-level input voltage	V _{DD} = 4.5 V	2.4		4.8	V
ЧH		V _{DD} = 5.5 V	2.4	1.1	5.8	v
VIL	Low-level input voltage (see N	otes 3 and 4)	-0.6	0	0.8	V
TA	Operating free-air temperature		0		70	°C

NOTES: 3. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

4. Due to input protection circuitry, the applied voltage may begin to clamp at -0.6 V. Test conditions must comprehend this occurrence. See Application Report entitled "TMS4164A and TMS4416 Input Diode Protection" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4416KU8-12	TM4416KU8-15	LINUT
		TEST CONDITIONS	MIN TYPT MAX	MIN TYPT MAX	UNIT
VOH	High-level output voltage	$I_{OH} = -2 \text{ mA}$	2.4	2.4	V
VOL	Low-level output voltage	IOL = 4.2 mA	0.4	0.4	V
4	Input current (leakage)	$V_I = 0 V$ to 5.8 V, $V_{DD} = 5 V$, All other pins = 0 V	± 10	± 10	μA
ю	Output current (leakage)	$V_0 = 0.4 \text{ V to 5.5 V},$ $V_{DD} = 5 \text{ V}, \text{ CAS high}$	± 10	± 10	μA
IDD1	Average operating current during read or write cycle	t _c = minimum cycle, All outputs open	108	96	mA
IDD2	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open	10	10	mA
IDD3	Average refresh current	t _C = minimum cycle, RAS cycling, CAS high, All outputs open	92	80	mA
IDD4	Average page-mode current	t _{C(P)} = minimum cycle, RAS low, CAS cycling, All outputs open	92	80	mA

[†]All typical values are at $T_A = 25$ °C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

	PARAMETER	MAX	UNIT
Ci(A)	Input capacitance, address inputs	14	pF
Ci(RC)	Input capacitance, strobe inputs	20	pF
Ci(W)	Input capacitance, write-enable input	20	pF
Ci/o	Input/output capacitance, data ports	10	pF



switching characteristics over recommended supply voltage range and operating free-air temperature range

PADAMETER	TEAT CONDITIONS	ALT.	TM4416KU8-12		TM4416KU8-15		UNIT	
PARAMETER		TEST CONDITIONS	SYMBOL	MIN	MAX	MIN	MAX	UNI
ta(C)	Access time from CAS	$C_L = 100 \text{ pF},$ Load = 2 Series 74 TTL gates	^t CAC		70		80	ns
t _{a(R)}	Access time from RAS	$t_{RLCL} = MAX,$ $C_L = 100 \text{ pF},$ Load = 2 Series 74 TTL gates	^t RAC		120		150	ns

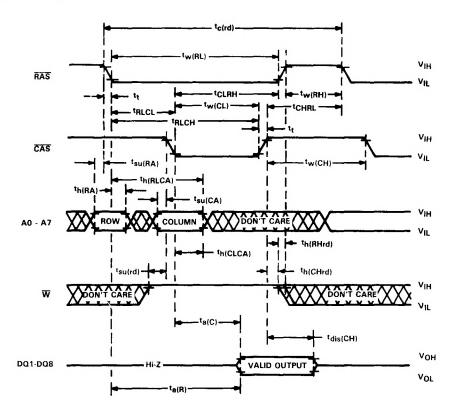
timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT.	TM441	BKU8-12	TM441	6KU8-15	
•		SYMBOL	MIN	MAX	MIN	MAX	UNIT
tc(P)	Page-mode cycle time	tPC			:4.		ns
tc(rd)	Read cycle time [†]	^t RC	230		260		ns
tc(W)	Write cycle time	tWC	230		260		ns
tc(rdW)	Read-write/read-modify-write cycle time	TRWC	315		365	-	ns
tw(CH)	Pulse duration, CAS high (precharge time) [‡]	tCP	40		50		ns
tw(CL)	Pulse duration, CAS low	tCAS	70	10,000	80	10,000	ns
tw(RH)	Pulse duration, RAS high (precharge time)	tRP	80		100		ns
tw(RL)	Pulse duration, RAS low	tRAS	120	10,000	150	10,000	ns
tw(W)	Write pulse duration	twp	30		40		ns
tt	Transition times (rise and fall) for RAS and CAS	tŢ	3	50	3	50	ns
tsu(CA)	Column-address setup time	tASC	0		0		ns
tsu(RA)	Row-address setup time	tASR	0		0		ns
t _{su(D)}	Data setup time	tDS	5		5		ns
tsu(rd)	Read-command setup time	tRCS	0		0		ns
t _{su} (WCH)	Write-command setup time before CAS high	tCWL	50		60		ns
t _{su} (WRH)	Write-command setup time before RAS high	tRWL	50		60		ns
th(CLCA)	Column-address hold time after CAS low	tCAH	35	A	40	1.5. A.	ns
th(RA)	Row-address hold time	tRAH	20		30		ns
th(RLCA)	Column-address hold time after RAS low	tAR	85		110		ns
th(CLD)	Data hold time after CAS low	tDH	40	1000	60	1000	ns
th(RLD)	Data hold time after RAS low	tDHR	90		130		ns
th(RHrd)	Read-command hold time after RAS high	tRRH	10		10		n
th(CHrd)	Read-command hold time after CAS high	tRCH	0		0		ns
th(CLW)	Write-command hold time after CAS low	tWCH	40		60	-	ns
th(RLW)	Write-command hold time after RAS low	tWCR	90	()	130		n
TRLCH	Delay time, RAS low to CAS high	tCSH	120		150		n
tCHRL	Delay time, CAS high to RAS low	tCRP	0		0		0
tCLRH	Delay time, CAS low to RAS high	tRSH	70		80		n
TRLCL	Delay time, RAS low to CAS low (maximum value specified only to guarantee access time)	tRCD	25	50	25	70	n
tWLCL	Delay time, W low to CAS low (early write cycle)	twcs	- 5		- 5		n
trf	Refresh time interval	TREF		4	1	4	m

[‡]Page mode only.

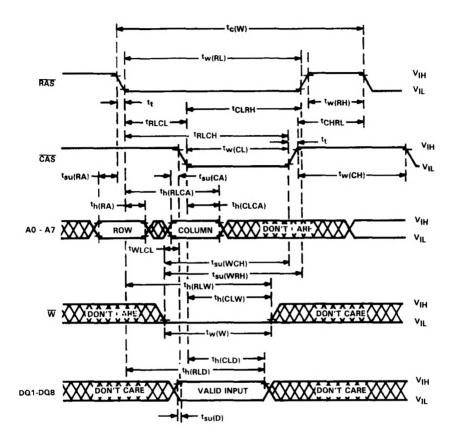


read cycle timing



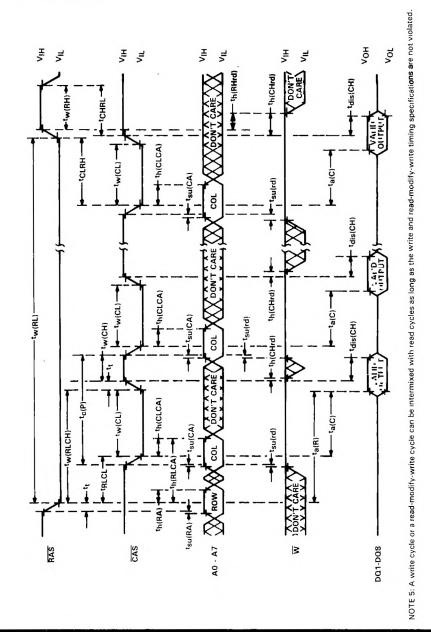


early write cycle timing



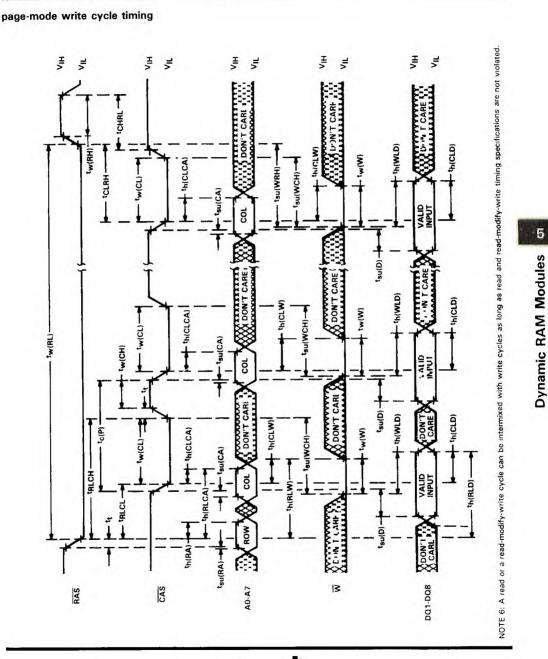


page-mode read cycle timing



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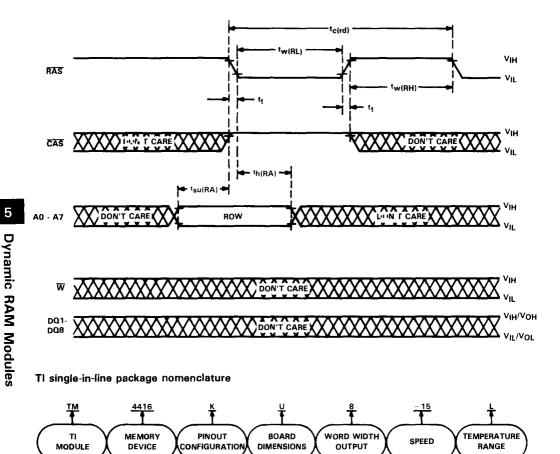
Dynamic RAM Modules



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ADVANCE INFORMATION

TM4464LU8 65,536 BY 8-BIT DYNAMIC RAM MODULE

OC' ···)185 - REVISED NOVEMBER 1985

65,536 X 8 Organization Single 5-V Supply (10% Tolerance) . 30-Pin Single-in-Line Package (SIP) Utilizes Two 64K X 4 Dynamic RAMs in **Plastic Chip Carrier** Long Refresh Period . . . 4 ms (256 Cycles) All Inputs, Outputs, Clocks Fully TTL Compatible **3-State Outputs Performance Ranges:** ACCESS ACCESS READ TIME TIME OR ROW COLUMN WRITE ADDRESS ADDRESS CYCLE (MAX) (MAX) (MIN)

60 ns

75 ns

230 ns

260 ns

Low Power Dissipation:

TM4464LU8-12

TM4464LU8-15

	OPERATING	STANDBY
	(TYP)	(TYP)
TM4464LU8-12	650 mW	25 mW
TM4464LU8-15	550 mW	25 mW

120 ns

150 ns

 Operating Free-Air Temperature . . . 0 °C to 70 °C

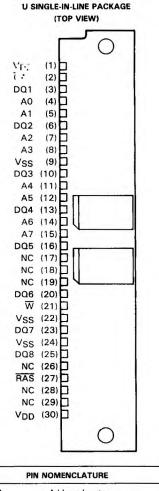
description

The TM4464LU8 is a 512K, dynamic randomaccess memory module organized as 65,536 × 8 bits in a 30-pin single-in-line package comprising two TMS4464FML, 65,536 × 4 bit dynamic RAM's in 22-lead plastic chip carriers mounted on top of a substrate together with two 0.2 μ F decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance.

operation

address (A0 through A7)

Fourteen address bits are required to decode 1 of 65,536 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe



P	IN NOMENCLATURE
A0-A7	Address Inputs
CAS	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
RAS	Row-Address Strobe
VDD	5-V Supply
VSS	Ground
∇	Write Enable

 (\overline{RAS}) . Then the six column-address bits are set up on pins A1 through A6 and latched onto the chip by the column-address strobe (\overline{CAS}) . All addresses must be stable on or before the falling edges of \overline{RAS} and \overline{CAS} . \overline{RAS} is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. \overline{CAS} is used as a chip select activating the column decoder and the input and output buffers.

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TM4464LU8 65,536 by 8-bit dynamic ram module

write enable (W)

The read or write mode is selected through the write-enable (\overline{W}) input. A logic high on the \overline{W} input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM4464LU8 dictates the use of early write cycles to prevent contention on DQ. When \overline{W} goes low prior to \overline{CAS} , the data outputs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ8)

Data is written during a write cycle. The falling edge of \overline{CAS} strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, \overline{W} is brought low prior to \overline{CAS} and the data is strobed in by \overline{CAS} with setup and hold times referenced to this signal.

data out (DQ1-DQ8)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of \overline{CAS} as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while \overline{CAS} is low; \overline{CAS} going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state, a necessity due to the grounded output enable.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless CAS is applied, the RAS-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with RAS causes all bits in each row to be refreshed. CAS can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 64 column locations on a single module, the row address and RAS are applied to multiple modules. CAS is then decoded to select the proper module.

power up

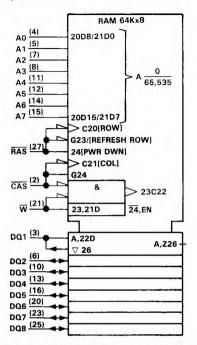
After power up, the power supply must remain at its steady-state value for 1 ms. In addition, the RAS input must remain high for 100 μ s immediately prior to initialization. Initialization consists of performing eight RAS cycles before proper device operation is achieved.

single-in-line package and components

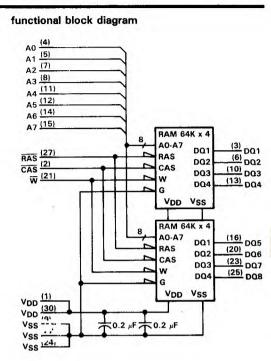
PC substrate: 0,79 mm (0.031 inch) minimum thickness Bypass capacitors: Multilayer ceramic Contact area for socketable devices: Nickel plate and solder plate on top of copper



TM4464LU8 65,536 BY 8-BIT DYNAMIC RAM MODULE



logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Voltage range for any pin except VDD and data out (see Note 1)	
Voltage range for VDD supply and data out with respect to VSS	1 V to 6 V
Short circuit output current	50 mA
Power dissipation	2 W
Operating free-air temperature range	. 0°C to 70°C
Storage temperature range (65°C to 150°C

[†]Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to VSS.

 Additional information concerning the handling of ESD sensitive devices is available in a document entitled "Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies" in Section 12.

TM4464LU8 65,536 BY 8-BIT DYNAMIC RAM MODULE

recommended operating conditions

			MIN	NOM	MAX	UNIT
VDD	Supply voltage		4.5	5	5.5	V
VSS	Supply voltage			0		V
M	High-level input voltage VDD = 4.5 V VDD = 5.5 V	$V_{DD} = 4.5 V$	2.4	1.1	4.8	
VIH		2.4		5.8	v	
VIL	Low-level input voltage (see N	ote 3)	-1	0	0.8	V
TA	Operating free-air temperature		0		70	°C

NOTE 3: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM	4464LU	8-12	TM	4464LU	8-15	
	FANAIVIETEN	TEST CONDITIONS	MIN	MIN TYPT MAX		MIN TYPT MAD		MAX	UNIT
VOH	High-level output voltage	$^{1}OH = -2 \text{ mA}$	2.4			2.4	11000		٧
VOL	Low-level output voltage	$l_{OL} = 4.2 \text{ mA}$	12.4		0.4			0.4	V
ų	Input current (leakage)	$V_1 = 0 V$ to 5.8 V, $V_{DD} = 5 V$, All other pins = 0 V			±10			± 10	μA
10	Output current (leakage)	V _O = 0.4 V to 5.5 V, V _{DD} = 5 V, CAS high			±10			±10	μΑ
IDD1	Average operating current during read or write cycle	t _C = minimum cycle, All outputs open		130	160		110	140	mA
IDD2	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open		5	10.		5	10	mA
1DD3	Average refresh current	t _C = minimum cycle, RAS cycling, CAS high, All outputs open		100	120		90	110	mA
IDD4	Average page-mode current	t _{c(P)} = minimum cycle, RAS low, CAS cycling, All outputs open		90	110		80	100	mA

[†]All typical values are at $T_A = 25 \,^{\circ}C$ and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, $f\,=\,1\,\,\text{MHz}$

	PARAMETER	MIN MAX	UNIT
Ci(A)	Input capacitance, address inputs	14	рF
Ci(RC)	Input capacitance, strobe inputs	20	pF
Ci(W)	Input capacitance, write-enable input	20	pF
Ci/o	Input/output capacitance, data ports	10	pF
Co(VDD)	Decoupling capacitance	0.4	μF



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switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER				ALT. TM4464LU8		2 TM4464LU8-15		UNIT
		TEST CONDITIONS	TEST CONDITIONS SYMBOL		MAY	MIN MAX		UNIT
ta(C)	Access time from CAS	$C_L = 100 \text{ pF},$ Load = 2 Series 74 TTL gates	tCAC		70		80	ns
t _a (R)	Access time from RAS	$t_{RLCL} = MAX,$ $C_L = 100 \text{ pF},$ Load = 2 Series 74 TTL gates	^t RAC		120		150	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT.	TM446	4LU8-12	TM446	4LU8-15	UNIT	
		SYMBOL	MIN	MAX	MIN	MAX	UNIT	
t _{c(P)}	Page-mode cycle time	tPC	120		140		ns	
tc(rd)	Read cycle time [†]	tRC	230	-	260		ns	
tc(W)	Write cycle time	tWC	230		260		ns	
tc(rdW)	Read-write/read-modify-write cycle time	^t RWC	315		365		ns	
tw(CH)	Pulse duration, CAS high (precharge time) [‡]	tCP	40		50		ns	
tw(CL)	Pulse duration, CAS low	tCAS	70	10,000	80	10,000	ns	
tw(RH)	Pulse duration, RAS high (precharge time)	tRP	80	1.191	100		ns	
tw(RL)	Pulse duration, RAS low	tRAS	120	10,000	150	10,000	ns	
tw(W)	Write pulse duration	twp	30	·	40		ns	
tt	Transition times (rise and fall) for RAS and CAS	tŢ	3	50	3	50	ns	
t _{su} (CA)	Column-address setup time	tASC	0		0		ns	
tsu(RA)	Row-address setup time	TASR	0		0		ns	
t _{su(D)}	Data setup time	tDS	5		5		ns	
tsu(rd)	Read-command setup time	^t RCS	0		0		ns	
tsu(WCH)	Write-command setup time before CAS high	tCWL	50	-	60		ns	
t _{su} (WRH)	Write-command setup time before RAS high	tRWL	50		60		ns	
th(CLCA)	Column-address hold time after CAS low	tCAH	35		40		ns	
th(RA)	Row-address hold time	tRAH	20		30		ns	
th(RLCA)	Column-address hold · · after RAS low	tAR	85		110		ns	
th(CLD)	Data hold time after 🐨 ow	tDH	40		60		ns	
th(RLD)	Data hold time after RAS low	^t DHR	90		130		ns	
th(BHrd)	Read-command hold time after RAS high	tRRH	10	1000	10		ns	
th(CHrd)	Read-command hold time after CAS high	t RCH	0		0		ns	
th(CLW)	Write-command hold time after CAS low	tWCH	40		60		ns	
th(RLW)	Write-command hold time after RAS low	tWCR	90		130	C	ns	
TRLCH	Delay time, RAS low to CAS high	tCSH	120		150		ns	
tCHRL	Delay time, CAS high to PAS low	tCRP	0	-	0		ns	
^t CLRH	Delay time, CAS low to	tRSH	70		80		ns	
TRLCL	Delay time, RAS low to CAS low (maximum value specified only to guarantee access time)	tRCD	30	50	30	70	ns	
tWLCL	Delay time, W low to CAS low (early write cycle)	twcs	- 5		- 5		ns	
trf	Refresh time interval	TREF		4		4	ms	

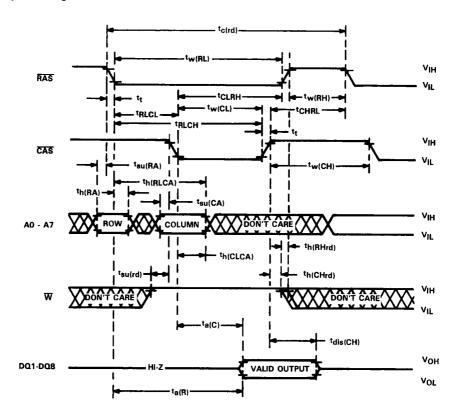
[†]All cycle times assume $t_t = 5$ ns.

[‡]Page mode only.



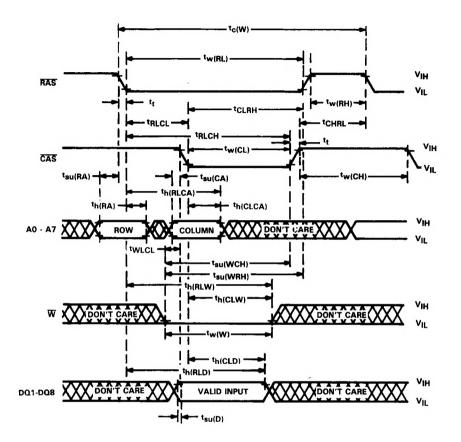
TM4464LU8 65,536 BY 8-BIT DYNAMIC RAM MODULE

read cycle timing





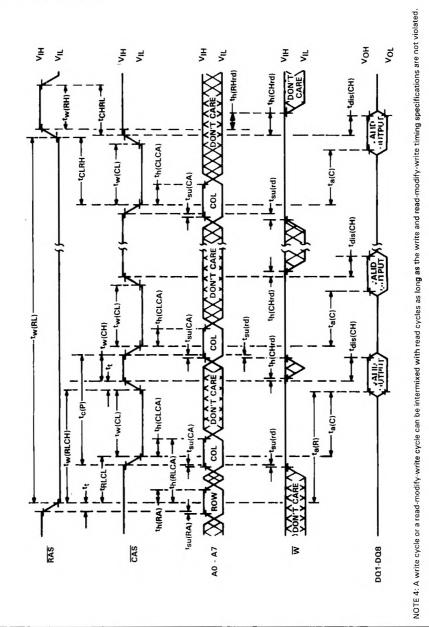
early write cycle timing





TM4464LU8 65,536 BY 8-BIT DYNAMIC RAM MODULE

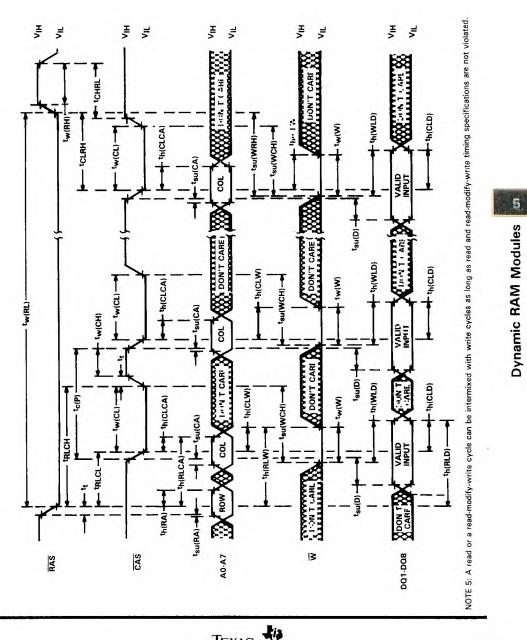
page-mode read cycle timing



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Dynamic RAM Modules

page-mode write cycle timing



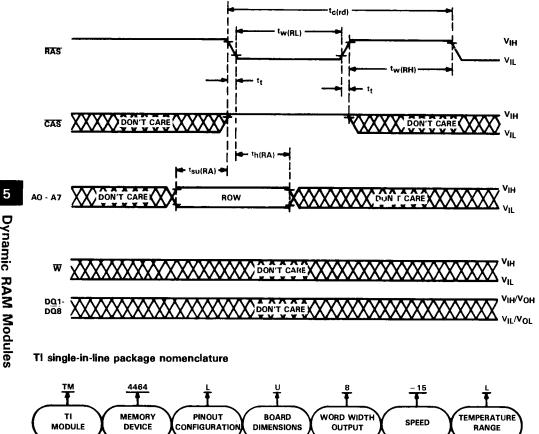
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5-255

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TM4464LU8 65,536 BY 8-BIT DYNAMIC RAM MODULE

RAS-only refresh timing



(88,9 x 16,5 mm) Max Access (3.5 x 0.65 inches) - 12 120 ns

L 0°C to 70°C – 15 150 пв

