This is the text from the Western Digital 1984 Storage Management Products Handbook pages 116 and 118. This chip is covered from pages 111 to 132.

279x-02 Floppy Disk Formatter / Controller Family

The 279X has two modes of operation according to the state of DDEN (Pin 37). When DDEN = 1, Single Density (FM) is selected. When DDEN = 0, Double Density (MFM) is selected, In either case, the CLK input (Pin 24) is set at 2 MHz for 8" drives or 1 MHz for 51/4"drives.

On the 2791/2793, the ENMF input (Pin 25) can be used for controlling both 5 1/4" and 8" drives with a single 2 MHz clock. When ENMF= 0, an internal divide by 2 of the CLK is performed. When ENMF = 1, no divide takes place. This allows the use of a 2 MHz clock for both 51/4" and 8" configurations.

The internal VCO frequency must also be set to the proper value. The 5/8 input (Pin 17) is used to select data separator operation by internally dividing the Read Clock. When 5/8 = 0, 5 1/4" data separation is selected; when 5/8 = 1, 8" drive data separation is selected.

CLOCK (24)	ENMF (25)	5/8 (17)	DRIVE
2 MHz	1	1	8"
2 MHz	0	0	51/4"
1 MHz	1	0	51/4"

FUNCTIONAL DESCRIPTION

The WD279X-02 is software compatible with the FD179X-02 series of Floppy Disk Controllers. Commands, status, and data transfers are performed in the same way. Software generated for the 179X can be transferred to a 279X system without modification.

In addition to the 179X, the 279X contains an internal Data Separator and Write precompensation circuit. The TEST (Pin 22) line is used to adjust both data separator and precompensation. When TEST = 0, the WD (Pin 31) line is internally connected to the output of the write precomp one-shot. Adjustment of the WPW (Pin 33) line can then be accomplished. A second one-shot tracks the precomp setting at approximately 3:1 to insure adequate Write Data pulse widths to meet drive specifications.

Similarly, Data separation is also adjusted with TEST = 0. The TG43 (Pin 29) line is internally connected to the output of the read data one-shot, which is adjusted via the RPW (Pin 18) line. The DIRC (Pin 16) line contains the Read Clock output (0.5 MHz for 8" drives). The VCO Trimming capacitor (Pin 26) is adjusted for center frequency.

Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in-circuit. The TEST line also contains a pull-up resistor, so adjustments can be performed simply by grounding the TEST pin, overriding the pull-up. The TEST pin cannot be used to disable stepping rates during operation as its function is quite different from 179X.

Other pins on the device also include pull-up resistors and may be left open to satisfy a Logic 1 condition. These are: ENP, 5\8, ENMF, WPRT, DDEN, HLT, TEST, and MR.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, DDEN should be placed to logical "1." For MFM formats, DDEN should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

The WD279X recognizes tracks and sectors numbered 00FFX. However, due to programming restrictions, only tracks and sectors 00 thru F4 can be formatted.

Sector Length Table*	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

"2795/97 may vary - see command summary.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the 279X before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

For write operations, the 279X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

READY

Whenever a Read or Write command (Type II or III) is received the 279X samples the Ready input. It this input is logic low the command is not executed and an interrupt is generated. Ail Type l commands are performed regardless of the state of the Ready input. Also, whenever a Type ll or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44-76.

COMMAND DESCRIPTION

The WD279X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

Write Precompensation

When operating in Double Density mode (DDEN = 0), the 279X has the capability of providing a user-defined precompensation value for Write Data. An external potentiometer (10K) tied to the WPW signal (Pin 33) allows a setting of 100 to 300 ns from nominal.

Setting the Write precomp value is accomplished by forcing the TEST line (Pin 22) to a Logic 0. A stream of pulses can then be seen on the Write Data (Pin 31) line. Adjust the WPW Potentiometer for the desired pulse width. This adjustment may be performed in-circuit since Write Gate (Pin 30) is inactive while TEST = 0.

Data Separation

The 279X can operate with either an external data separator or its own internal recovery circuits. The condition of the TEST line (Pin 22) in conjunction with MR (Pin 19) will select internal or external mode.

To program the 279X for external VCO, a MR pulse must be applied while TEST = 0. A clock equivalent to eight times the data rate (e.g. 4.0 MHz for 8" Double Density) is applied to the VCO input (Pin 26). The feedback reference voltage is available on the Pump output (Pin 23) for external integration to control the VCO. TEST is returned to a Logic 1 for normal operation. Note: To maintain this mode, TEST must be held low whenever MR is applied. For internal VCO operation, the TEST line must be high during the MR pulse, then set to a Logic 0 for the adjustment procedure.

A 50K Potentiometer tied to the RPW input (Pin 18) is used to set the internal Read Data pulse for proper phasing. With a scope on Pin 29 (TG43), adjust the RPW pulse for 1/8 of the data rate (250 ns for 8" Double Density). An external variable capacitor of 5-60 pf is tied to the VCO input (Pin 26) for adjusting center frequency. With a frequency counter on Pin 16 (DIRC) adjust the trimmer cap to yield the appropriate Data Rate (500 K Hz for 8" Double Density). The line must be low while the 5/8 line is held high or the adjustment times above will be doubled.

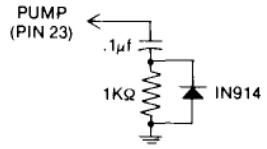
After adjustments have been made, the TEST pin is returned to a Logic 1 and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 1ines may toggle without affecting the drive.

The PUMP output (Pin 23) consists of positive and negative pulses, which their duration is equivalent to the phase difference of incoming Data vs. VCO frequency. This signal is internally connected to the VCO input, but a Filter is needed to connect these pulses to a slow moving DC voltage.

The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favor of a PUMP UP condition. Therefore, it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.

A first order lag-lead filter can be used at the PUMP output (Pin 23). This filter controls the instantaneous response of the VCO to bit-shifted data (jitter) as well as the response to normal frequency shift, i.e., the lock-up time. A balance must be accomplished between the two conditions to inhibit over-responsiveness to jitter and to prevent an extremely wide lock-up response, leading to **PUMP** runaway. The filter affects these two reactions in mutually opposite directions.

The following Filter Circuit is recommended for 8" FM/MFM:



Since 51/4" Drives operate at exactly one-half the data rate (250 Kb/sec) the above capacitor should be doubled to 0.2 uF.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-in, and Step-Out commands. Each of the Type I Commands contains a rate field (r0 r1), which determines the stepping motor rate as defined in Table 3.

A 2 us (MFM) or 4 us (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step Direction Motor through the device interface.

TABLE 3. STEPPING RATES

CLK		2 MHz	1 MHz
R1	RO	TEST = 1	TEST = 1
0	0	3 ms	6 ms
0	1	6 ms	12 ms
1	0	10 ms	20 ms
1	1	15 ms	30 ms

After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type l commands. Note that this time doubles to 30 ms for a 1 MHz clock. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1.The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID