TI STRICTLY PRIVATE

WAFER TAPE DRIVE
PROBLEM ANALYSIS AND MODIFICATIONS
TEXAS INSTRUMENTS JAPAN ENGINEERING CENTER

* J E C *

COMPACT COMPUTER GROUP JEC

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SECTION 1

SCOPE

THIS DOCUMENTS DESCRIBES ANALYSIS AND MODIFICATIONS FOR WAFER TAPE DRIVE. ANALYSIS AND MODIFICATIONS ARE BASED UPON OUR EXPERIMENTAL AND MEASURMENTS WHICH COME FROM PRIVATE LAB IN OUR SUB-CONTRACTORS IN JAPAN.

1.1 GOAL

SOLVE INTERCHANGEABILITY PROBLEM AND IMPROVE SYSTEM RELIABILITY.

ERROR RATE MUST BE REQUIRED AS ; 10$ -7 BITS FOR SELF READ/WRITE.
10$ -6 BITS FOR INTERCHANGED.

PRODUCT COST AFTER PROPER MODIFICATIONS SHALL BE LESS OR EQUAL TO ORIGINAL COST GOAL. OUR INITIAL COST GOAL IS LESS THAN $40.00 BML , AND LESS THAN $50.00 FOB JAPAN AS WELL AS TURN KEY BASE.

RELATED INFORMATION IS AVAILABLE AT JEC (JAPAN ENGINEERING CENTER):

YUICHI MURANO OR KAZU KAWAMURA

TEXAS INSTRUMENTS JAPAN , ENGINEERING CENTER.

SUNCREST BULDING 8TH FL. 13-5 KITA-AOYAMA , 2 CHOME , MINATO-KU , TOKYO JAPAN.

MSG " ECJ " M/S 4356 TEL 03-403-7511 EXT 226.

SECTION 2

PROBLEM ANALYSIS

ANALYSIS ARE CONSIDERED FROM BOTH SIDE MECHANICAL AND ELECTRICAL AND WORKED WITH TWO SUB-CONTRACTORS IN ORDER TO RETRIEVE ANY ERRORS OF MEASURMENTS AND/OR MISS UNDERSTANDING OF PROBLEMS.

ALL DATAS ARE TAKEN FROM LATEST LUBBOCK DRIVES WITH ENTREPO CARTRIDGES WHICH WE GOT FROM LUBBOCK ON SEP. 84'.

2.1 APPROACH

UNDER OUR EXPERIENCE WE REALIZED THAT PRESENT WAFER DRIVE SHOWS SATISFACTLY LEVELS OF PERFORMANCE FOR SELF READ-WRITE OPERATIONS, BUT INTERCHANGED.

WE SUSPECTED THAT THE DATAS WRITTEN ON CARTRIDGES CARRY X % OF ERRORS WHEN IT WAS WRITTEN ON A DRIVE, AND ACCUMULATION OF ERROR WHEN ITS READ ON ANOTHER DRIVES ARE ASSUMINGLY EXCEEDED THE READ MARGIN.

SO THERE'S CHANCE THAT X +/- Y > Z UNDER SOME PORTIONS.

X : WRITTEN DATA ERRORS.
Y : ERRORS OF DRIVE ITSELF.
Z : MERGIN OF READ.

"X" CONSISTS OF 1) DATA SKEW ,2) BIT SHIFT BY SPEED ,3) WRITE GAIN AND/OR 4) WRITE DATA SHIFT.

"Y" CONSISTS OF 1) AZIMUTH ,2) BIT SHIFT BY SPEED ,3) WOW-FLUTTER , 4) READ GAIN AND/OR 5) READ TIMMING.

"Z" IS 33 % OF JITTER ALLOWANCE BY SOFTWARE.

2.1.1 MECHANICAL RELATED ANALYSIS.

2.1.2 SPEED CONTROL.

TAPE SPEED :(MOTOR SHAFT DIM.) X 3.14 X (MOTOR ROTATION) /60 / 2.54
0.25 X 3.14 X 1550 / 60 / 2.54 = 7.99 INC/SEC

A) START TIME
(SPEED UPTO 98% OF FULL SPEED)

1, WITHOUT MOTOR CONTROL ---------- 400 MS.

2, WITH MOTOR CONTROL ---------- 400 MS.

B) SPEED VARIATIONS

1, WITHOUT MOTOR CONTROL ---------- 2.5 % / 100 SEC.
(CONSTANT LOAD)
---------- 8.5 %
(CHANGE LOAD)

2, WITH MOTOR CONTROL ---------- 2.25 % / 100 SEC.
(CONSTANT LOAD)
---------- 2.5 %
(CHANGE LOAD)

3, DRIVE TO DRIVE ---------- 19.5 %
(WITHOUT MTC)
---------- 1.25 %
(WITH MTC)

4, TEMPERATURE RESPONSE ---------- - 8 %
(10 C FROM 25 C)
---------- + 5 %
(40 C FROM 25 C)

2.1.3 MODIFIED SPEED CONTROL.

REFERING TO 2.1.2 , PRESENT LUBBOCK SPEED CONTROL LOGICS WORKS SATISFACTLY EXCEPT TEMPERATURE RESPONSE.

PURPOSE FOR MODIFICATION OF SPEED CONTROL LOGIC ARE 1) ADD TEMPERATURE COMPENSATE FUNCTION, 2) REDUCE PARTS AND 3) EASE OF ADJUSTMENTS.

MOTOR SPEED CONTROL IS USED LAG552-2 , 8 PINS DIP IC , WHICH MADE BY MITSUMI.

LAG552 IS A MOTOR SPEED CONTROL IC OPERATED WITH LOW VOLTAGE OF VCC=1.8V MIN.

-OPERATING TEMPARATURE	---	10 - 60 C
-SUPPLY VOLTAGES	---	10 V MAX.
-OUTPUT CURRENT	---	700 MA
-POWER DISSIPATIONS	---	700 MW
-VOLTAGE REGULATION	---	+/- .02 %/C
-VOLTAGE REGULATION	---	+/- .2 %/V

FOLLOWING ARE SHOWN IMPROVEMENTS OF MODIFIED SPEED CONTROL:

- SPEED VARIATION	----------	0.3 % / 80 SEC. (CONSTANT LOAD)
		1.5 % (CHANGE LOAD)
- TEMPERATURE RESPONSE	----------	-0.8 % (10 C FROM 25 C)
	----------	+0.2 % (40 C FROM 25 C)

2.1.4 WOW FLUTTER .

WOW-FLUTTER OF PRESENT SYSTEM IS MAINLY COUSED BY PINCH ROLLER INSIDE OF CARTRIDGES. PEAK OF WOW-FLATTER IS NEAR 6HZ.

- WOW FLATTER VS CARTRIDGES (5')

CARTRIDGE #	WOW-FLATTER(%)
1	6.4
2	2.3
3	3.0
4	2.8
5	1.9
6	3.1
7	2.3
8	9.0 *
9	2.2
10	5.6

" X" = 3.29 % (* IS EXCLUDED)

WOW-FLATTER ALSO COUSED BY ECCENTRICITY OF MOTOR SHAFTS. PRESENT NAMIKI MOTOR HAS VARIOUS ECCENTRICITY OF SHAFT WHICH IS OVER 5 U .

WOW-FLATTER CAN BE REDUCED BY CHANGING MOTOR SHAFT TO SMALL. UNDER OUR EXPERIMENTAL , WOW-FLATTER IS DOWN TO 1.52 % FROM 3.29 % AT 1.5 MM SHAFT WITH 2580 RPM. HOWEVER THIS CHANGES ALSO MAKE ANOTHER PROBLEM WHICH IS LIFE OF TAPES. WEAR OF TAPE IS ACCELARATED BY SMALLER SHAFT.

PRESENT MECHANISM IS DESIGNED TO CONTROL PINCH PRESSURE BY USING LOW DEGREE OF MATERIAL INSTEAD OF USING PINCH PRESSURE MECHANISM IN IT.

2.1.5 PINCH PRESSURE .

WITHOUT PINCH PRESSURE CONTROL MECHANISM, PINCH PRESSURE MAY VARY EVERYTIME INSERTING CARTRIDGES.

- CARTRIDGE POSITION VS MOTOR CURRENT

DRIVE #	RIGHT ADJUSTED	LEFT ADJUSTED	ERROR
1	73 MA	62 MA	15.0 %
2	53	46	13.2
3	73	64	12.3
4	74	62	16.7
5	120	109	9.0
6	74	59	20.0
8	104	91	12.5
9	88	81	7.9
10	66	61	7.6

"X" = 12.7 %

THIS DATA SHOW NOT ONLY RELATION OF CARTRIDGE POSITIONING, BUT ALSO MECHANICAL DISTRIBUTION BETWEEN CARTRIDGES AND DRIVES.

FOR INSTANCE, IN CASE OF "RIGHT ADJUSTED " CURRENT CHANGES FROM 66 MA TO 120 MA, AND CONSEQUENTRY MOTOR SPEED IS CHANGED FROM 1440 RPM TO 1600 RPM WITHOUT SPEED CONTROL LOGICS.

2.1.6 MODIFIED MECHANISM .

MODIFIED MECHANISM IS DESIGNED TO SOLVE PROBLEMS WHICH COUSED BY RELATION BETWEEN PINCH ROLLER AND CAPSTAIN. MODIFIED ONE HAS MECHANISM TO KEEP CONSTANT PRESSURE TO PINCH ROLLER, AND TO RECOVER ARBITRARY INSERTION OF CARTRIDGES.

MAJORE MODIFICATION OF MECHANISM IS SPRING RETAINED PINCH PRESSURE CONTROL FOR MOTOR MOUNTINGS. PRESENT MECHANISM WAS DESIGNED THAT PINCH PRESSURE IS MANAGED BY USING LOW DEGREE PINCH ROLLER, AND THIS ALSO COUSE WOW-FLATTER PROBLEM.

MODIFIED MECHANISM IS ALLOW TO USE HARDER PINCH ROLLERS, 55 - 60 DEGREE.

* POINTS FOR MECHANICAL MODIFICATIONS *

1, DRIVE MECHANISM

- SPRING RETAINED MOTOR MOUNTING.
- ADD STRIKER ON LEFT SIDE OF CARTRIGE INLET.
- ADD RETAINER SPRING ON AZIMUTH ADJUSTING SCREW.
- OFFSETTED BOT SENSOR SLIGHTLY TO SECURE DETECTIONS.

2, CARTRIDGES

- INCREASE HARDNESS OF PINCH ROLLER. (55 - 60)
- ADD RETAINER RIBS INSIDE OF CARTRIDGES TO KEEP TAPE WINDINGS DOWN ON REEL.

ACCURACY OF PRESENT CARTRIDGES AND DRIVE MECHANISM IS NOT GOOD ENOUGH TO INCREASE RELIABLITY OF SYSTEMS. CARTRIDGES SEEMS TO HAVE NO DATUM ZERO POINT , AND POSITION BETWEEN TOP CASE AND BOTTOM CASE IS OFFSETTED. ALSO BOTH CARTRIDGES AND DRIVE MECHANISM ARE REALIZED MANY SINKS OF PLASTIC MOLDINGS.

2.2 ELECTRICAL RELATED ANALYSIS

2.2.1 WRITE DATA .

DIGITAL WRITE DATA FROM 70C20 CPU SHOULD BE DESIGNED TO KEEP CERTAIN BIT CELL TIMES OF 125 US. SINCE DATA WAS WRITTEN AS PHASE ENCORDING METHOD, DATA FREQUENCIES ARE 125 US AND 62.5 US AS WELL AS F AND 2F.

- WRITE DATA TIMMING -

* DATA PATTERN " 0011 " AND WRITE 6 CYCLES.
* TEST POINT - OUTPUT FROM C240.

TIMMING	ERROR
F (MAX) = 125 US	0.0 %
F (MIN) = 124 US	-0.8 %
2F (MAX) = 67 US	+6.7 %
2F (MIN) = 58 US	-7.2 %

THIS ERROR SURELY BECOME ONE OF ACCUMULATED FACTORS, AND DATA WRITTEN ON CARTRIDGES ARE POSSIBLY CARRY THIS ERRORS BEFORE PLAYBACK BY ANOTHER DRIVES.

THIS ERROR MAY BE COUSED BY THAT 70C20 PROCESS OTHER TASKS ,SUCH AS INTERRUPT HANDRING, DURING SENDING WHITE DATA OPERATION.

2.2.2 WRITE CIRCUIT .

PRESENT WRITE CIRCUIT HAS PARALLEL CAPACITOR C15 ,AND DESIGNED RESONANCE WITH HEAD INDUCTANCE. THIS CIRCUIT WORKS BANDWITH OF RESONANCE ,AND EVENTUALLY DISTORT PHASE.

- PHASE DISTORTION VS CAPACITOR VALUE -

* WRITE 80 US AND 40 US.

CAPACITOR	MAX.	MIN.	ERROR
0.0000 UF	81/41US	79/39 US	1.25 %
0.00411	TOO DISTORTED (CAN'T MEASURE)		-
0.00457	82/40	78/39	2.5
0.005	82/42	77/41	3.7
0.00553	82/47	69/42	13.7
0.00589	85/46	65/43	18.7
0.0647	79/47	65/45	18.7

AS A RESULT OF THIS EXPERIMENTS , CAPACITOR VALUE SHOULD BE 0.005 +/- OTHERWISE PHASE DISTORTION EXTREMELY INCREASED.
HOWEVER ,EVEN IF CHOOSE PRICISE VALUE OF CAPACITORS, TOLERANCE OF HEAD INDUCTANCE IS USUALLY +/- 20 OR 30 %.
NAMIKI'S HEADS ALSO SHOW 10 - 20 % OF DISTRIBUTION.

CAPACITOR C15 MUST BE REMOVED FROM CIRCUITS.

2.2.3 READ CIRCUIT .

IN READ OPERATION CAPACITOR C15 ALSO DISTORT READ WAVEFORM FROM HEAD. SPEED VARIATION BETWEEN A DRIVE AND B DRIVE COUSED FREQUENCY CHANGE OF READ DATA,AND THIS COUSE CHANGE OF RESONANCE POINT OF HEAD CIRCUIT.

CAPACITOR C20 OF DIFFERENTIATION CIRCUIT MAKE OUTPUT WAVEFORM DULL,AND THIS CHANGES THRESHOLD TIMING.

BUFFER U6 74C240 USE ON BOTH READ AND WRITE CRICUIT, AND THIS COUSE INTERFERENCE BETWEEN EACH CIRCUITS.

REDUCED HEAD INDUCTANCE IS PURPOSED TO ENSURE OVER WRITTEN ON PRIVIOUS DATAS RATHER THAN IMPROVE READ WAVEFORM. REMENDER OF PRIVIOUS DATA COUSE JITTER WHEN READ.

2.2.4 MODIFIED ELECTRONICS .

* POINTS FOR ELECTRICAL MODIFICATIONS *

1, REMOVE CAPACITOR C15 ON WRITE CRICUIT.
2, REMOVE CAPACITOR C20 ON READ CRICUIT.
3, CHANGE HEAD INDUCTANCE TO 10 MH 30 OHM.
4, USE SEPARATE IC FOR U6.
5, RE-DESIGN MOTOR SPEED CONTROL LOGIC USING LAG552.

FOR ALL ABOVE MODIFICATIONS, AMP. BOARD IS NEWLY DESIGNED.

SECTION 3

EVALUATION TEST

3.1 METHOD OF TEST

TEST FOR INTERCHANGEABILITY IS TESTED BY 5 DRIVES X 5 TAPES,CALLED 5 X 5 MATRIX TEST. EVALUATION IS BASED AS COMPARISON BETWEEN MODIFIED DRIVES AND LATEST LUBBOCK DRIVES UNDER SAME CIRCUMSTANCE.

3.2 TEST RESULT

3.2.1 LUBBOCK DRIVES .

5 OUT OF 30 DRIVES FROM LUBBOCK ON AUGAST 84 ARE CHOSEN AT RANDUM.

TEST IS DONE AT 10^7 READ ON SELF R/W AND 10^6 ON INTERCHANGED.

: (DRIVE , TAPE)

TEST #1 : USE 5" TAPES.

- SELF READ/WRITE -- NO ERRORS.
- INTERCHANGED -- ERROR ON
  (3, 4) - ERROR 6=55
  (3, 5) - ERROR 26=53
  (4, 2) - ERROR 16=9
  (4, 3) - ERROR 4=1, ERROR 16=9
  (5, 1) - ERROR 6=3, ERROR 4=1
  (5, 2) - ERROR 26=1, ERROR 6=7
  (5, 3) - ERROR 16=11,ERROR 6=3
  (5, 4) - ERROR 6=10

TEST #2 : USE 5′ TAPES.

- SELF READ/WRITE -- NO ERRORS.

- INTERCHANGED -- ERROR ON
  (1, 4) - ERROR 6=1
  (3, 1) - ERROR 6=3
  (3, 2) - ERROR 6=4
  (3, 4) - ERROR 6=43, ERROR 12=1
  (3, 5) - ERROR 26=56
  (4, 5) - ERROR 12=1
  (5, 2) - ERROR 6=1

3.2.2 MODIFIED DRIVE .

TEST #1,2,3 ARE 10^7(EXP) READ ON SELF R/W AND 10^6 READ ON INTERCHANGED. TEST #4,5 ARE 10^8 READ ON SELF R/W AND 10^7 READ ON INTERCHANGED.

TEST #1 : USE 5" ORIGINAL(ENTREPO) TAPES. (GROUP 1 DRIVES)

- SELF READ/WRITE -- NO ERRORS.
- INTERCHANGED -- NO ERRORS.

TEST #2 : USE 5" ORIGINAL (ENTREPO) TAPES. (GROUP 2 DRIVES)

- SELF READ/WRITE -- NO ERRORS.
- INTERCHANGED -- NO ERRORS.

TEST #3 : 10 X 5 TEST. (5 X 5 TEST USING CARTRIGES AFTER GROUP 1 TEST)

- INTERCHANGED -- NO ERRORS.

TEST #4 : 10 7 BITS READ TEST WITH 20" ORIGINAL (ENTREPO) TAPES.

- SELF READ/WRITE -- NO ERRORS.
- INTERCHANGED -- ERROR ON
  (1, 2) - ERROR 26=94
  (1, 5) - ERROR 26=2, ERROR 6=2
  (3, 2) - ERROR 12=1
  (3, 5) - ERROR 26=8, ERROR 6=7
  (4, 1) - ERROR 26=1, ERROR 6/12=1
  (5, 1) - ERROR 12=5, ERROR 6=53
  (5, 2) - ERROR 26=10, ERROR 6=58
  ERROR 12=1 ,ERROR 4=8

TEST #5 : 10 7 BITS READ TEST WITH MODIFIED 20" TAPES.

- SELF READ/WRITE -- NO ERRORS.
- INTERCHANGED -- ERROR ON
  (5, 4) - NON I/O ERROR =1, ERROR 6=1

3.2.3 TEST CONCLUSION .

ACCORDING TO TEST RESULT, LUBBOCK DRIVES SEEMS TO HAVE LITTLE IMPROVEMENTS FOR INTERCHANGEABILITY PROBLEMS. TEST DATA LOOKS DRIVE #5 OR DRIVE #3 HAS INTERCHANGE PROBLEMS, BUT NOT ON BOTH TEST #1 AND #2. IN CASE OF ERRORS ON ALL OTHER DRIVES, RE-READ OPERATION WAS PERFORMED ON WRITTEN DRIVES, BUT NO ERROR WAS FOUND .

MODIFIED DRIVES OBVIOUSLY PERFORMED BETTER THAN LUBBOCK DRIVES, EVEN TO USE ENTERPO CARTRIDGES. 5 X 5 TEST ON BOTH GROUPS AND 10 X 5 TEST WERE COMPLETED WITHOUT ANY SINGLE BIT ERROR UNDER 10^7 BITS READ.

ALTHOUGH 10^7 BITS READ TEST IS NOT REQUIREMENTS OF INTERCHANGED TEST, MODIFIED DRIVES WITH MODIFIED CARTRIDGES CLEAR 5 X 5 TEST ONLY WITH SINGLE ERRORS.

OF COURSE MODIFIED DRIVES ARE DESIGNED TO USE MODIFIED CARTRIDGES. COMBINATION OF BOTH DRIVE AND CARTRIDGES ARE REQUIRED TO SOLVE INTERCHANGEABILITY PROBLEMS.

MODIFIED CARTRIDGES ARE NOT ALLOWED TO USE LUBBOCK DRIVES DUE TO PRODUCE TAPE DAMAGES BY HARDER PINCH ROLLERS.

3.2.4 ERROR DISTRIBUTION .

ERROR DISTRIBUTION AFTER MODIFICATION

SECTION 4

SUBCONTRACTOR

4.1 RECOMMENDED SOURCE OF SUPPLY

PIONEER ANSAFONE MANUFACTURING CORPORATIONS

70 - 1 HAYASHI 2 - CHOME, TOKOROZAWA CITY,
SAITAMA. JAPAN 359

TEL) 0429 - 49 - 5111.
DEX) 2953 - 774.

: ONE OF PIONEER GROUPS AND 100 % OWNED BY PIONEER CO,LTD.
MAINLY PRODUCE TELEPHON ANSWERING SYSTEM AND DICTATING MACHINES
FOR OEM BASIS.

4.2 QUOTATION

QUOTATION FROM PIONEER ARE BASED UPON TI SCHIMATICS 1048963 REV 15.

UNIT PRICE : 11,020. YEN ($ 47.91)/ 120K / YEAR.
NOTE : $$ 1 = 230 YEN

WARRANTY : 12 MONTHS AFTER SHIPMENT FROM FACTRY.

TOOLING : 18,000,000 YEN. ($ 78 K) : ESTIMATED

INCLUDE: AC ADAPTER / MANUAL / OVER PACK.
70C20 WAS ESTIMATED 575 YEN.
EXCLUDE: IBC CHIP / HEXBUS CABLE / CARTRIDGES.

PRICE SHOWN ABOVE DID NOT COUNT ANY COST REDUCTION PLAN, HOWEVER PCB INTERCONNECT AND MOTOR IS USED AS ANOTHER ALTERNATIVE. MOTOR IS USED 1MM THICKER ONE OR PIONEERS ONE.

ESTIMATED THEIR MATERIAL COST WOULD BE 11020 X .75 = 8295 YEN($ 35.90).

PIONEER ALSO PROPOSED THEIR COST REDUCTION MODEL WHICH TO AIM $ 30.00 , MODEL ARE USE THICKER CASE TO ALLOW MORE FLEXIBILITY TO CHOICE OF MOTORS AND/OR TO DESIGN OF INSIDE STRACTURE SUCH AS ONE PRINTED CIRCUIT.

4.2.1 JEC COST ESTIMATION .

- REGISTOR TOTAL	-------	¥ 85.	
- CAPACITOR TOTAL	-------	¥ 180.	
- TR/DIODE TOTAL	-------	¥ 275.	
- IC TOTAL	-------	¥ 2640.	
- PLASTIC TOTAL	-------	¥ 800.	ESTIMATE.
- ELECTRIC PARTS	-------	¥ 5750.	
- PACKING/MIS	-------	¥ 1200.	ESTIMATE.
MATERIAL TOTAL	:	¥ 10930.	$ 47.50.

COST ESTIMATE ARE BASED UPON MODIFIED DRIVES.