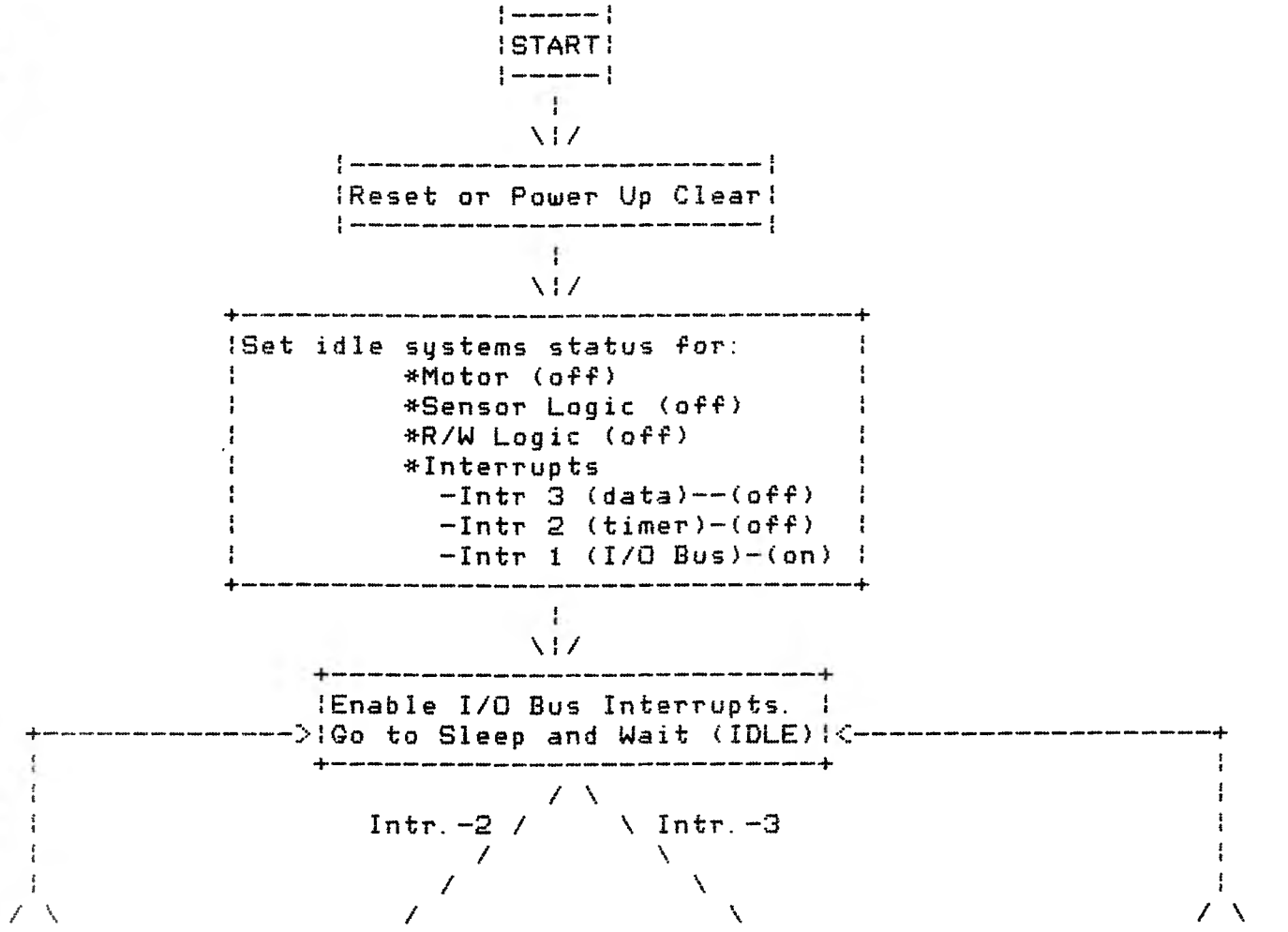
Microtape Functional Flowchart

Functional Flowchart



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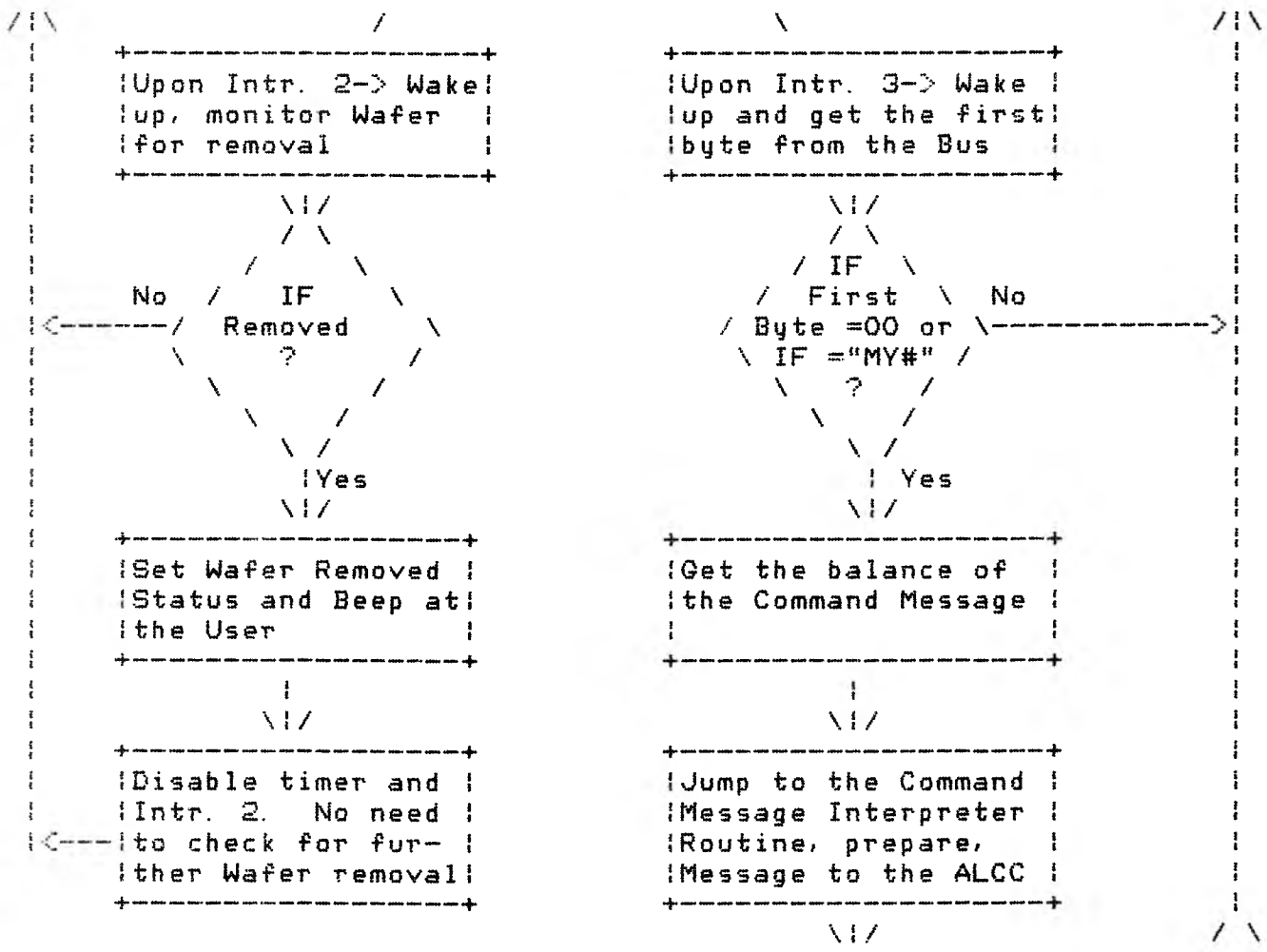
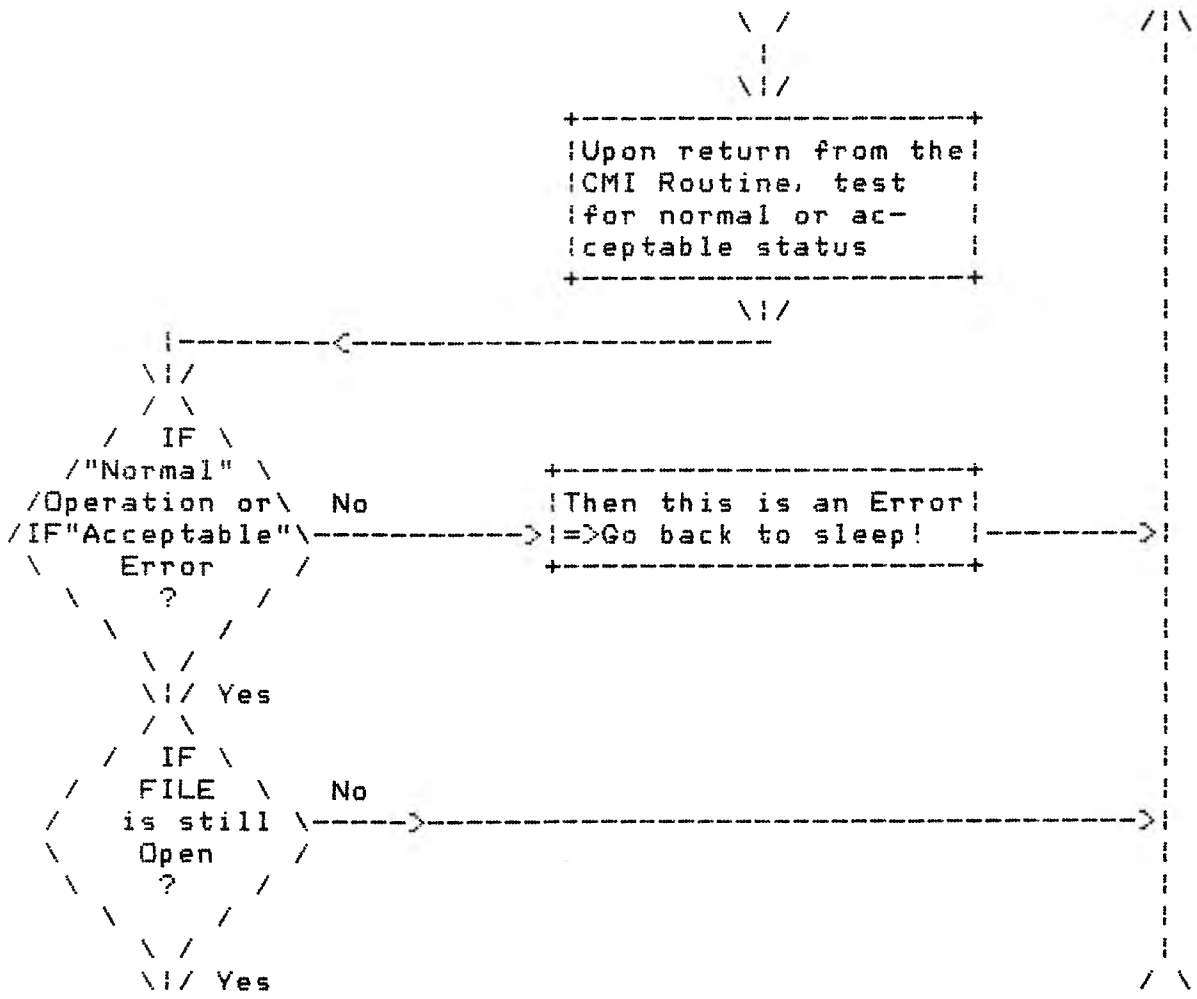

Upon Intr. 2-> Wake up, monitor Wafer for removal
IF Removed ?
No
Yes
Set Wafer Removed Status and Beep at the User
Disable timer and Intr. 2. No need to check for fur- ther Wafer removal
Upon Intr. 3-> Wake up and get the first byte from the Bus
IF First Byte =00 or IF ="MY#" ?
No
Yes
Get the balance of the Command Message
Jump to the Command Message Interpreter Routine, prepare, Message to the ALCC


Upon return from the CMI Routine, test for normal or acceptable status
IF "Normal" Operation or IF "Acceptable" Error ?
No
Then this is an Error
=>Go back to sleep!
Yes
IF FILE is still Open ?
No
Yes

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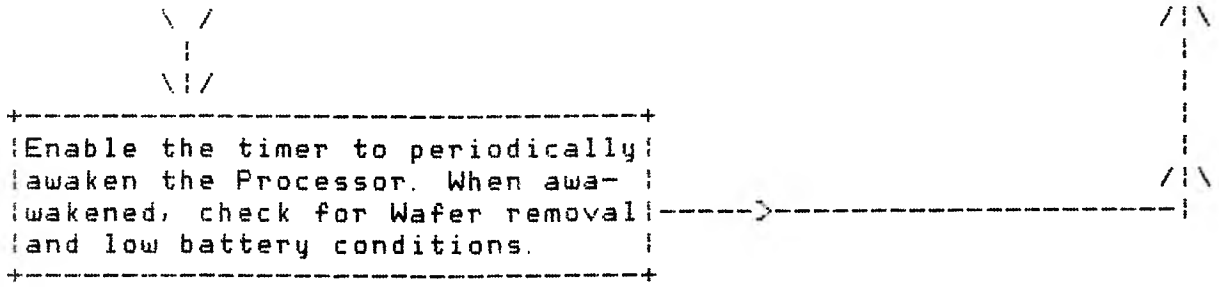
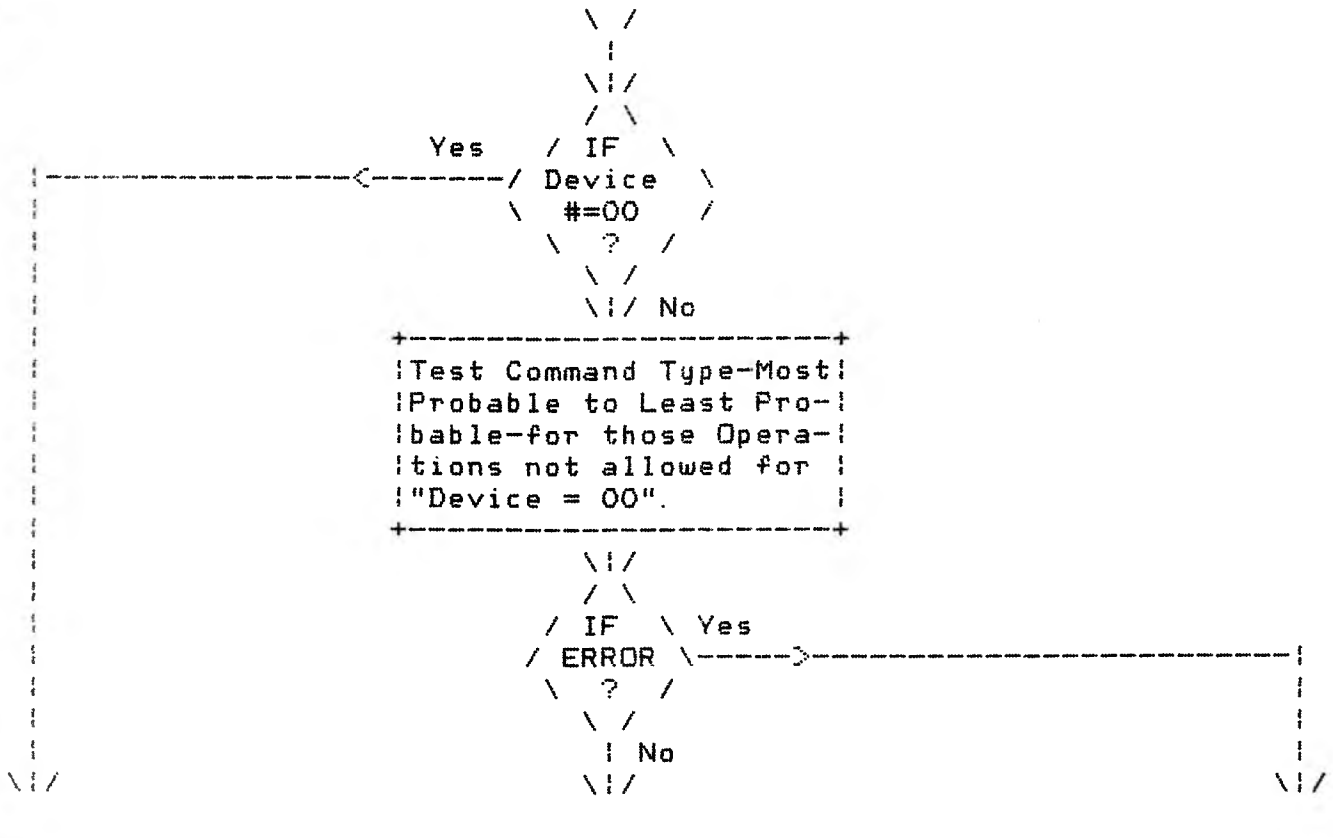

Enable the timer to periodically awaken the Processor. When awakened, check for Wafer removal and low battery conditions.

COMMAND MESSAGE INTERPRETER ROUTINE



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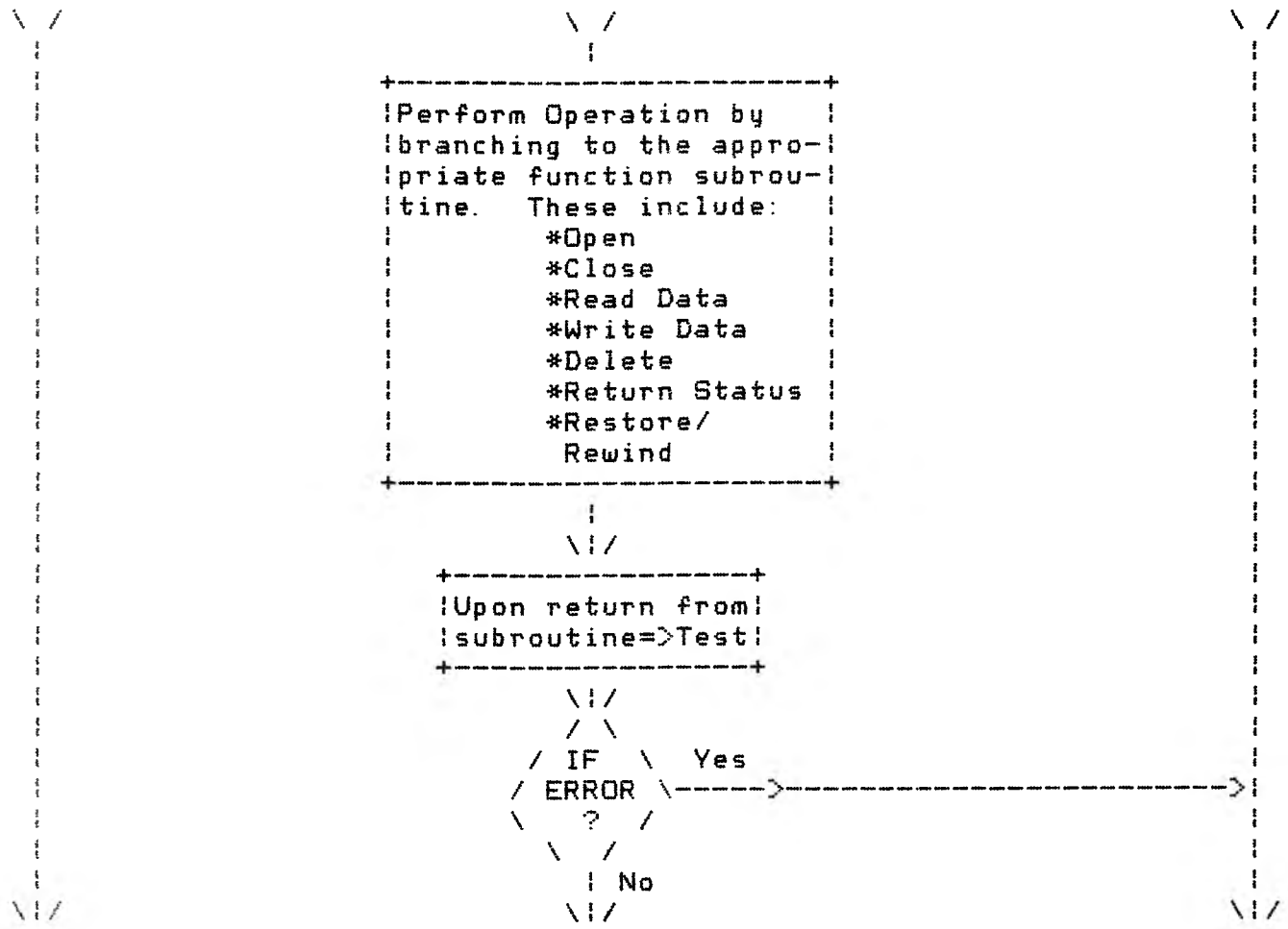
Perform Operation by branching to the appropriate function subroutine. These include:
*Open
*Close
*Read Data
*Write Data
*Delete
*Return Status
*Restore/ Rewind
Upon return from subroutine=>Test
IF ERROR ?
Yes
No

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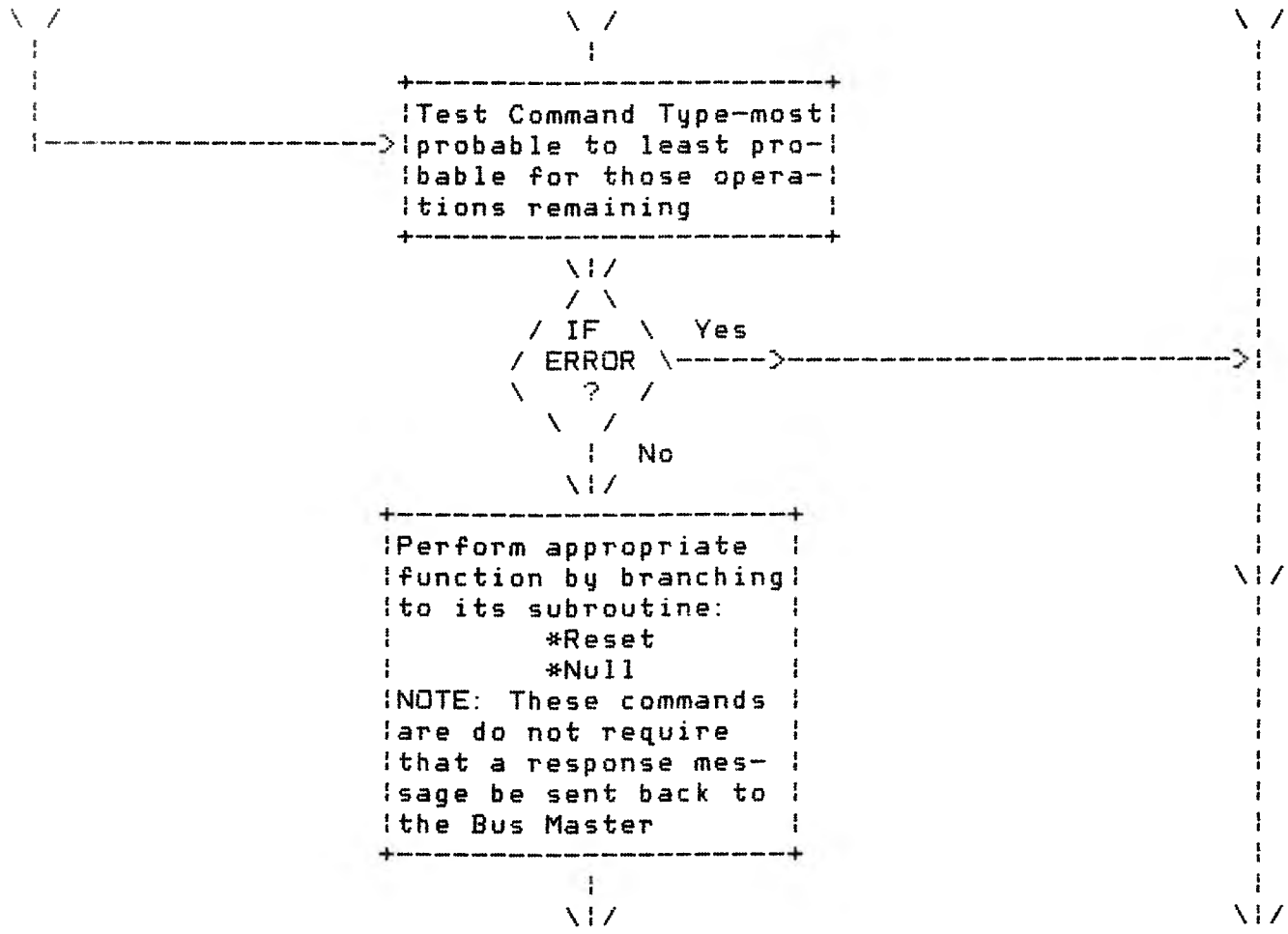
Test Command Type-most probable to least probable for those operations remaining
IF ERROR ?
Yes
No
Perform appropriate function by branching to its subroutine:
*Reset
*Null
NOTE: These commands are do not require that a response message be sent back to the Bus Master

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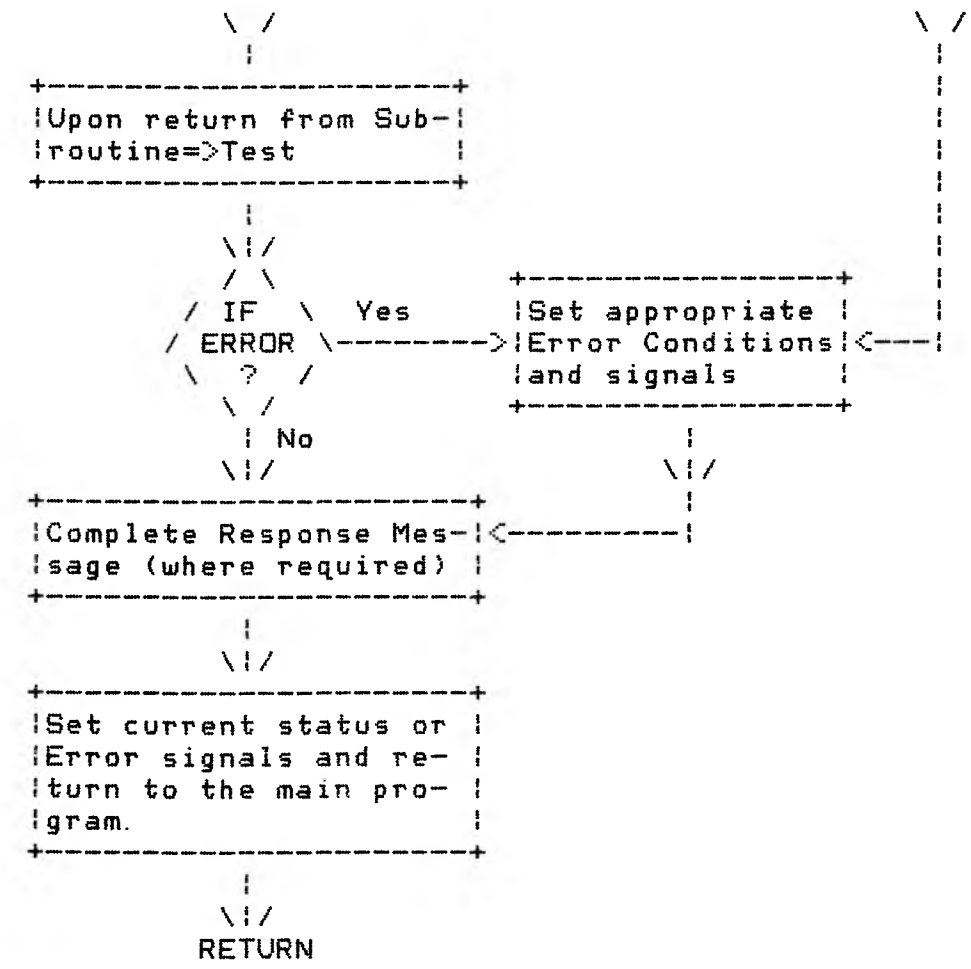
Upon return from Sub-routine=>Test
IF ERROR ? Yes
No
Set appropriate Error Conditions and signals
Complete Response Message (where required)
Set current status or Error signals and return to the main program.
RETURN

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READ/WRITE CIRCUIT EXPLANATION

The READ/WRITE circuit consist of three separate sections: a Digital Head Read and Write Circuit section, a Sensor Circuit section, and a Low Battery Detect Circuit section. Each section is discussed separately.

1.0 The Low Battery Detect Circuit compares the battery voltage (divided by R7 and R8) to the Analog Circuit Voltage (divided by R50 and R34). If the Battery Voltage is low, the comparator (1/4 of a LM339N comparator IC) pulls resistor R42 low informing the processor of a low battery condition. Resistor R40 provides hysterisis for the slowly changing Battery Voltage level.

2.0 The Sensor Circuit provides indication of a Write Protected Wafer and Beginning of Tape/End Of Tape information. Both Sensors and the Amber Front Panel LED (D13) are turned on by Q1, which is in turn activated by the "SENSOR EN L" line (where R30 sets the current gain). Resistor R31 is a low value resistor which limits the current going through the three diodes. Diode D9 serves as ZOT protection for the Front Panel LED.

The Write Protect Sensor detects the presence of a small, white dot on the wafer. If this dot is present, the light from the emitter portion of the sensor will reflect and cause the detector portion of the Sensor to pass a small amount of current. This current shows up as a voltage at the inverting input of the comparator. This voltage is compared to the divided analog voltage form R50 and R34. Whether the reflective, small white dot is present or not is indicated by the output of the comparator (whether R21 is pulled low or not).

The Beginning Of Tape/End Of Tape Sensor detects the presence of a reflective, metallic strip on the moving tape as it passes underneath the BOT/EOT Sensor. Light from the Sensor emitter passes through the wafer plastic to strike the tape. If the reflecitve strip is present, then the light bounces back through the wafer plastic to the Sensor dector. If the strip is not present, then the light is "absorbed" by the graphite backcoating on the tape. The presence of light at the Sensor detector will cause a proportionate amount of current to be passed by the transistor. This will show up as a voltage level at the top of R32. Because the wafer is not perfectly transparent, but is in fact translucent, a small amount of "background" light will show up at the Sensor from the wafer plastics. Additionally, as the tape is run more, the amount of light reflected from the tape will probably increase. For these reasons, we place a combination filter and Sample/Hold between the Sensor and the comparator input. Capacitor C14 and Resistor R33 eliminate the background light level and reduce spurious noise from the moving tape. The values were selected to provide approximately 34 mS of indication from the Sensor as the tape passes underneath it. Should the reflective strip be present, the comparator will indicate to the CPU by pulling the BOT/EOT line (normally pulled high by R39) low. Since the signal from the Sensor is relatively fast, no hysteresis resistor in the feedback loop is needed.

3.0 The Digital Head Read and Write Circuitry is fairly complex and will be discussed by stages here. When the user desires to put data on or retrieve data from the tape, they first turn the analog circuit power on. This is done by the CPU pulling one of several control lines low. Any of the "active" control lines will pull R9 low thus enabling the Analog Supply Voltage transistor Q3. C13 and C15 provide bulk and high frequency decoupling for the analog voltage.

The "Write Data" line from the CPU is normally tri-stated during any operation except a "Write" (pulled high by R14). This is done because any changing waveform on this line could affect the data during "Read" operation. (Even though the data is tri-stated by the Write Drivers, some small amount of voltage is leaked through. This Milli-Volt signal is easily ignored by Digital Logic but the very sensitive Read Circuitry may interpret this as false data.) During a Write Operation, data is fed through two exclusive or gates. One gate inverts the data and the other gate just buffers it. This ensures that we have two very closely matched complementary waveforms. Each waveform is fed to two inverters whose outputs are tied together. (The CMOS inverters provide a fairly substantial drive capability.) Each inverter pair's output is fed to the Digital Head through a resistor (R44 and R45) and each resistor may be bypassed by a capacitor (C18 and C19, optional). This technique allows one side of the head to be driven high and the other side to be pulled low. As the CPU changes the state of the Write Data line, the driver on each side of the head also changes state. This creates a flux reversal on the tape. When the state change occurs, the drivers must supply far more than their steady state current to the head. There is a RL time-constant that is involved and for best operation, we wish to make this time constant very short. Thus the optional bypass capacitors. Capacitor C20 is used during the read operation to prevent oscillations which might lead to self erasing and bad data.

For "Read Operations", the CPU disables the "Write Data" line and tri-states the Head Drivers. The small signal coming from the Head (generated by the inductance of the Head and the moving tape) is differentially amplified by the first stage of the dual Op Amp. Resistors R46 and R47 are equal and precisely matched (1%). The gain is set by R48/R46. Resistor R49 is equal in value to R48 for minimum offset. Diodes D13 and D14 serve to protect the Op Amp inputs since they should not see more than the V(+) or V(-) Supply Rails. These voltages could be seen by the Op Amp since the Head is an inductive device and, in the write mode, there is some overshoot of the supply rails at the input of the Op Amp. The diodes do not affect data in the read mode since there must be approximately 0.6V for them to conduct and the signal from the head is only 12mV to 25mV in size.

The second Op Amp stage performs a number of functions during "Read Operations". Capacitor C16 and Resistor R17 perform a "low pass" filter function on incoming signals and serve to block the first stage's gained offset from being amplified any more. Capacitor C17 and Resistor R18 perform a "high pass" filter function. A Bandpass function is formed by the two RC networks and, since the effective impedances are different, a second stage voltage gain is created. The bandpass filter also serves to limit the Noise Bandwidth. Diodes D1 and D7 are in the feedback loop to ensure that the Amplifier stays within a proper operating signal range. This is effectively a limiter function. It should be noted that C16 can cause a problem since the input waveform to the second stage is not symetrical. This means that the Op Amp side of the Capacitor can charge up or down if there is a greater "high" or "low" time for the signal. We avoid this distortion by making sure that the first stage output waveform has relatively fast rise and fall times (which directly relates back to writing a high quality signal with fast rise and fall times). It should also be noted that the amplified waveform from the Head is biased at the mid-point level of the Analog Voltage (about 2.5V). Resistors R35 and R36 set the bias voltage level and capacitors C6 and C21 serve to decouple the voltage level. Diode D6 prevents the Op Amps from ever seeing more than the supply rail when the Analog voltage is turned off.

In the third stage, a comparator (1/4 LM339N) compares the conditioned Head signal to the 2.5V reference level. Resistors R10 and R11 form a hysterisis network to protect against false transitions during periods of "no data" (so that noise will not yield false information). Resistor R43 is pulled down or released by the open collector comparator to indicated data transitions. The Raw Read Data is fed to both the processor and the next stage.

The fourth and final stage performs the function of an edge detector. Raw Read Data is received from the third stage and inverted. The inverter is capable of supplying a significant amount of current and can be thought of as a voltage source. Resistor R41 and Capacitor C12 form a RC network and yield a time constant. By selecting the appropriate value of R41 and C12, a timed high going pulse is formed by exclusively OR-ing the output of the RC network and the Raw Data signal for every flux transition. The value of the RC network currently yields a 4 micro-second pulse out of the XOR gate for every flux transition. The edge trigerred pulses are fed to the interrupt pin on the CPU and internal code decodes the raw data and the edge triggered pulses to produce a bit stream.