INTELLIGEHT BUS CONTROLLER

DEVELOPMENT TRACE

Texas Instruments
Consumer Products Group

2/3/82

SECTION 1

Design Goals

Initial design requirements were:

a) Compatibility with electrical specs for ALC bus

b) Latch capability for HSK line

c) Capability for controlling the bus in MASTER or SLAVE modes

d) Simple hardware structure for easy implementation

During the design process following requirements were added:

a) Simple hardware interface to several popular microprocessors

b) Capability to interface with 4-bit MPU like TMS-1000

c) Simple software control and efficient coding

d) Self power-up procedure

SECTION 2

First arproach

The main requirements for first arproach was to design the circuit with minimum number of components in order to be able to use discrete ICs. The minimum implementation shown in Figure 1. Table 1 shows necessary components for TTL and CMOS implementation.

Table 1: TTL and CMOS implementation

	TTL	CMOS
1	74LS74	CD4013
2	CD4049	CD4049
3	7406	CD40107 (3)
TOTAL	3	5

Initial design goals were met, but circuit proved to be very unefficient from software point of view, requiring very large amount of time to be spent on monitoring the status lines. Also circuit required allocation of 14 dedicated signals from MPU.

SECTION 3

First Improvements

Minimum configuration proved cost effectivness of using custom or semicustom integrated circuit to achieve better results, like:

a) less number of dedicated signals

b) simpler control from MPU

c) monitoring the bus control signals to issue an interrupt when data available

d) inhibit till next message

The circuit shown in Figure 2 satisfies requirements stated above. It can be connected to the bus of TMS-7000 without extra components. Circuit will act like a "smart" peripheral and has it's own set of commands.

SECTION 4

Final Configuration

Close study of circuit in Figure 2 and in-depth analysis of applications exhibit additional function most-likely needed for wide range use.

a) compatibility with 4 and 8 bit MPU

b) capability to work with popular MPU, like TMS-7000, 8085, 1802 and 6502

c) additional commands like "Disable Interrupt"

d) capability to interface with bidirectional buses as well as with unidirectional

e) programmable level for interrupt line, including open-drain output

f) power-up clear

g) data latch clear with release of HSK

All of this features are incorporated into the circuit shown in Figure 3.

Minimum configuration

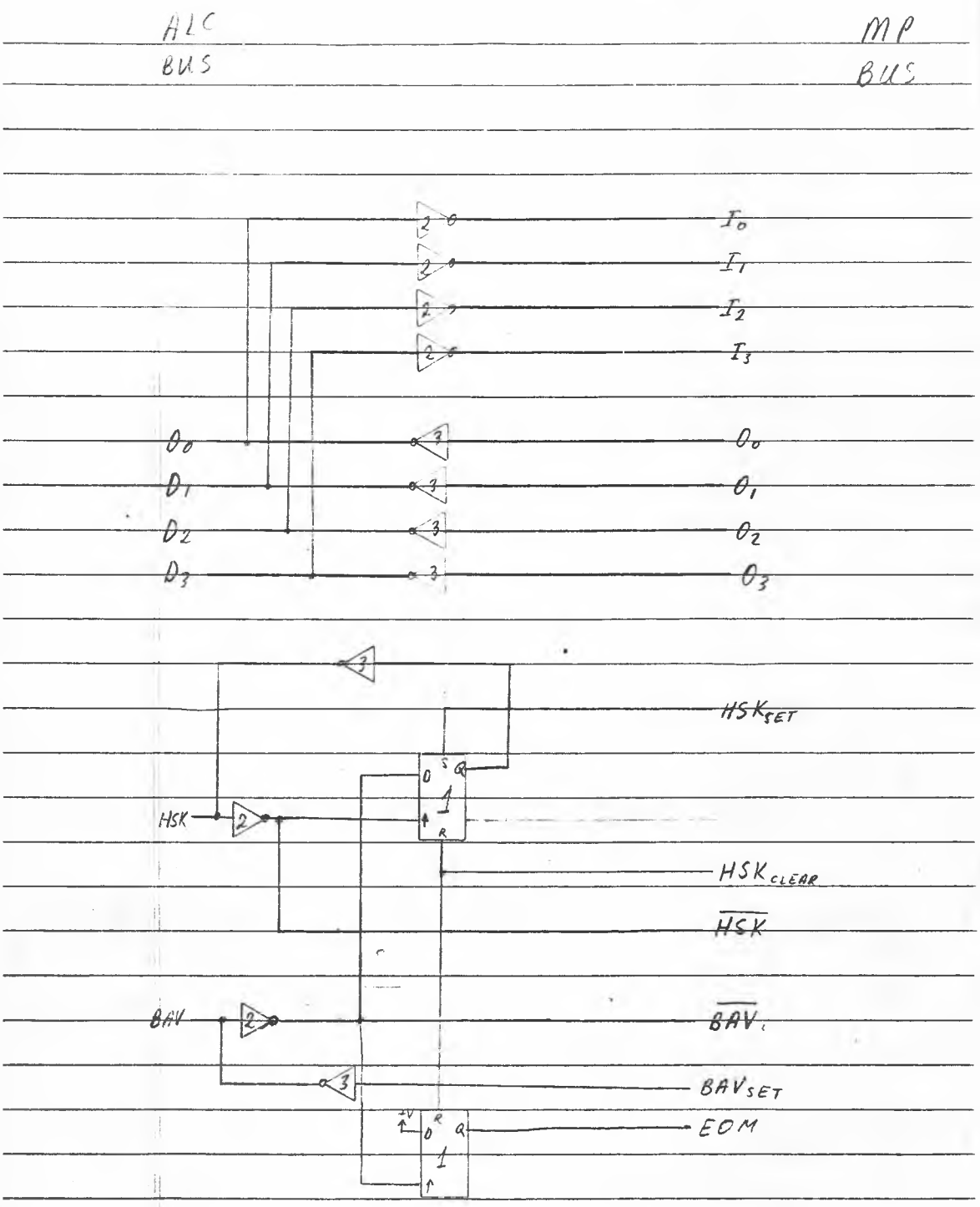

Figure 1