IBC - I

PRELIMINARY SPECIFICATIONS

FOR VENDOR QUOTES

Texas Instruments
Consumer Products Group

12/31/81

SECTION 1

General Information

1.1 Quote Breakdown

Quotes are requested for Gate Array / Semi-Custom and/or Full-Custom CMOS implementation of the logic provided. Expected volume requirements are indicated below. Please provide information on available packages for this part. The logic provided should be referred as IBC-I.

1.2 Volume

*Packaged prototype units required by May 1, 1982

*First production 2H82: 10,000 - 20,000

*Production: 1Q83 - 20,000 units
2Q83 - 30,000 units
3Q83 - 50,000 units
4Q83 - 20,000 units

1.3 For Additional Information

For clarification or additional information contact

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SECTION 2

Electrical Characteristics

1. Technology - CMOS

2. Operating Temperature Range - 0 C - +70 C

3. Operating Vdd - 4.5 TO 9.5 Vdc

4. Input/Output Characteristics - see Table 1 and 2

5. Timing Requirements - see Section 3

6. Power Requirements - less than 1 mW (dynamic)

Table 1

Input-Output Characteristics for

$\overline{D\ 0 - D\ 5, IRQ}$ (Open Drain Outputs)

	Vdd (Vdc)	MIN	MAX	UNIT
Vih (note 1)	5	3.5	12	V
	9	3.5	12	V
Vil (note 1)	5	0	1.5	V
	9	0	1.5	V
Vol	5	0	.4	V
	9	0	.4	V
Iol (sink current)	Vol= .4 V	4		mA

Note 1 - not applicable for $\overline{IRQ}$ line (output only)

Table 2

Input-Output Characteristics for

I/O 0 - I/O 3, $\overline{CS}$, RS, MS,

$\overline{E}$, R/$\overline{W}$, $\overline{RES}$, O 0 - O 2

	Vdd (Vdc)	MIN	MAX	UNIT
Vih	5	2	5	V
	9	4	10	V
Vil	5	0	.8	V
	9	0	3	V
Voh (note 2)	5	4.5	5	V
	10	9	10	V
Vol (note 2)	5	0	.05	V
	10	0	.1	V

Note 2 - not applicable for $\overline{CS}$, RS, MS, $\overline{E}$ and $\overline{RES}$ lines (input only)

Remarks:

At Vdd=5Vdc input lines I/O 0 - I/O 3, $\overline{CS}$, RS, MS, $\overline{E}$, R/$\overline{W}$, $\overline{RES}$ and O 0 - O 2 should be TTL compatible and output lines O 0 - O 2 and R/W should be CMOS compatible.

SECTION 3

Timing Requirements

Internal Gate Delay - 10 nsec (max @ Vdd=5 Vdc)

I/O Pair Delay - 30 nsec (max @ Vdd=5 Vdc)

Data Hold Time (note 3) - 10 nsec (max @ Vdd=5 Vdc)

Turn Off Time (3-state buffer) - 10 nsec (max @ Vdd=5 Vdc)

Note 3 - for latches indicated by letters A, B and C on logic diagram after active transition on clock line (from LOW-to-HIGH)

SECTION 4

Logic Elements Description

Latches 'A' - data latched on LOW-to-HIGH TRANSITION on clock line (see Figure 1 for truth table)

Latches 'B' - data latched on LOW-to-HIGH TRANSITION on clock line (see Figure 2 for truth table)

Latches 'C' - data latched on LOW-to-HIGH TRANSITION on clock line (see Figure 3 for truth table)

Logic Block 'D' - 2 to 1 multiplexer (see Figure 4 for truth table)

Logic Block 'E' - 4 to 1 multiplexer (see Figure 5 for truth table)

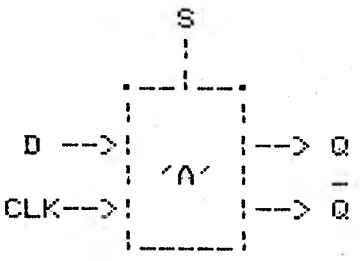
Gates 'F' - have 3-state outputs(see Figure 6 for truth table)

Gates 'H' - have input characteristics as CD4050, but Vih(max)=12 Vdc

Gates 'I' - have open drain outputs (Isink=4mA)

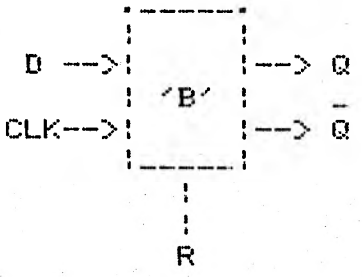
Logic Block 'K' - active pullup (see Figure 7 for truth table)

Figure 1 - Latches '^'



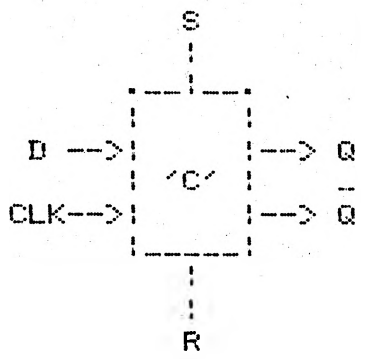
D	CLK	S	Q	$\overline{Q}$	
0	$\_/\overline{\ }$	0	0	1	
1	$\_/\overline{\ }$	0	1	0	
X	$\overline{\ }\backslash\_$	0	Q	$\overline{Q}$	NO CHANGE
X	X	1	1	0	

Figure 2 - Latches 'B'



D	CLK	R	Q	$\overline{Q}$	
0	⎍	0	0	1	
1	⎍	0	1	0	
X	⎽	0	Q	$\overline{Q}$	NO CHANGE
X	X	1	0	1	

Figure 3 - Latches 'C'

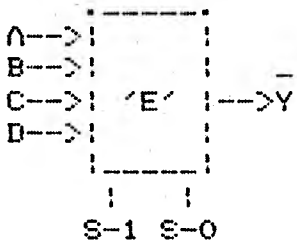


D	CLK	R	S	Q	$\overline{Q}$	
0	_/‾	0	0	0	1	
1	_/‾	0	0	1	0	
X	‾_	0	0	Q	$\overline{Q}$	NO CHANGE
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

FIGURE 4 - 2 to 1 multiplexer 'D'

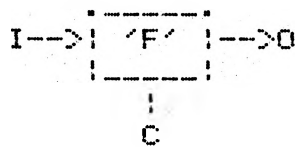
S	A	B	Y
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

FIGURE 5 – 4 to 1 multiplexer 'E'



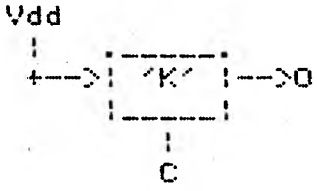
S-1	S-0	A	B	C	D	$\overline{Y}$
0	0	0	X	X	X	1
0	0	1	X	X	X	0
0	1	X	0	X	X	1
0	1	X	1	X	X	0
1	0	X	X	0	X	1
1	0	X	X	1	X	0
1	1	X	X	X	0	1
1	1	X	X	X	1	0

Figure 6 - Gates 'F'



C	I	O
1	X	Hi-Z
0	0	0
0	1	1

Figure 7 - Gates 'K'



C	O
0	ACTIVE PULLUP OFF
1	ACTIVE PULLUP ON