```
       IDT    'MICROJWO'
       OPTION XREF
*      JEF WINSOR
*
* MICROTAPE PERIPHERAL CONTROL SOFTWARE
*-----------------------------------------------------------------
* SYSTEM HARDWARE IMPLEMENTATION  ,-------,
*                         ,-------|ADDRESS|
*,--------,               | ,-----|SELECT |
*|   70C20|               | | ,---|       |
*|        |               | | | ,-|_______|   ,-------,
*|04  6 A0|<--ADDR 0------' | | | ,-----------|VOLTAGE|
*|    7 A1|<--ADDR 1--------' | | | ,---------|CONTROL|
*|    8 A2|<--ADDR 2----------' | | | ,------>|_______|
*|    9 A3|<--ADDR 3------------' | | |
*|   10 A4|<--NC                  | | |
*|   16 A5|<--LOW BATTERY---------' | |   ,-------,
*|   15 A6|<--MOTOR PROHIBITED------' |   |WP AND |
*|   11 A7|<--NC                      |   |EOT/BOT|
*|        |                    ,------+-->|SENSORS|
*|06  3 B0|-->LED              |      |   |_______|
*|    4 B1|-->WRITE ENABLE-----+------+--,   | |
*|    5 B2|-->SENSORS ON-------'      |  |   | |
*|   37 B3|-->MOTOR ON----------------*--+-, | |
*|   38 B4|-->A-LATCH--------------,     | | | |
*|    1 B5|-->R/W----------------, |     | | | |
*|   39 B6|-->ENABLE-----------, | |     | | | |
*|    2 B7|-->NC               V V V     | | | |
*|        |                  ,---------, | | | |
*|08 28 C0|<->DATA 0/RS---<->|         | | | | |
*|   29 C1|<->DATA 1-----<->| I/O BUS | | | | |
*|   30 C2|<->DATA 2-----<->|         | | | | |
*|   31 C3|<->DATA 3-----<->| SUPPORT | | | | |
*|   32 C4|<->CS---------<->|_________| | | | |
*|   33 C5|---NC                 |  ,----+-+-' |
*|   34 C6|---NC           ,-----+--' ,--+-+---'
*|   35 C7|---NC           |  ,--+----'  V V
*|        |                |  |  |     ,-----,
*|0A 27 D0|<--WRITE DATA--+--+--+---->|TAPE |
*|   26 D1|<--EOT/BOT------'  |  |  ,--|DRIVE|
*|   24 D2|<--WP--------------'  |  |  |_____|
*|   23 D3|<--INPUT RAW DATA-----+--'     |     *input raw data
*|   22 D4|<--  ---*--- +V ROM    |        |      may go back to
*|   21 D5|<--  ---*      OPTIONS |        |      port a to help
*|   20 D6|<--  ---*              |        |      micro-code
*|   19 D7|<--  ---'              |        |
*|        |                       |        |
*| 13 INT1|<---IRQ----------------'        |
*| 12 INT3|<---TAPE TRANSITION PULSE-------'
*|________|
       PAGE
*-----------------------------------------------------------------
* register file equates
STACKL EQU    >10                        reserved stack area length
BITCON EQU    R2                         nibble bit counter
STACK  EQU    R3                         soft stack location
REGS   EQU    STACK+STACKL               start of registers
NIBCON EQU    REGS+1                     data length nibble counter
COUNT  EQU    NIBCON                     16 bit counter
CHKSUM EQU    REGS+3                     checksum value (16 bits)
INT1V  EQU    REGS+5                     int1 ram-vector
INT2V  EQU    REGS+7                     int2 ram-vector
```

```
INT3V   EQU     REGS+9                  int3 ram-vector
DATAP   EQU     REGS+11                 data pointer
DLPCNT  EQU     DATAP                   data length pointer/counter
DATA    EQU     REGS+12                 nibble pack/unpack
SAB     EQU     DATA+10                 ms address byte of sab
STATUS  EQU     SAB-9                   status to be returned
DLEN    EQU     SAB-7                   data length
BLEN    EQU     SAB-5                   buufer length
RNUM    EQU     SAB-3                   record number
DQUAL   EQU     SAB-2                   device qualifier
CCODE   EQU     SAB-1                   command code
DCODE   EQU     SAB                     device code
        PAGE
*---------------------------------------------------------------------
* peripheral file equates
IOCNTL  EQU     P0                      i/o control
TIME    EQU     P2                      timer start value
CAPTUR  EQU     P3                      timer value @ int3
PSCALE  EQU     P3                      prescale control
TIMER   EQU     P2                      timer control
TEST    EQU     P4                      data & system test port
DRIVE   EQU     P6                      drive & system control
BCNTL   EQU     P8                      bus control
BDATA   EQU     P8                      bus data
BSTAT   EQU     P8                      bus status
WAFER   EQU     P10                     wafer i/o
DDRD    EQU     P11                     ddr for port d
        PAGE
*---------------------------------------------------------------------
* constant equates
BITIME  EQU     >00                     data half-bit time
CINPUT  EQU     >03                     input command code
CPRINT  EQU     >04                     print command code
DLTIME  EQU     >00                     dl half-bit time
ENABLE  EQU     >00                     enable ibc
EOT     EQU     >02                     bit test for EOT
DROP    EQU     >01                     drop hsk bit
HSK     EQU     >01                     bus ready bit test
HSKSET  EQU     >00                     let hsk float
INHIB   EQU     >04                     inhibit bus communication
INITDR  EQU     >00                     initialize drive
INITWF  EQU     >01                     initialize wafer ddr
INPUT   EQU     >08                     wafer data bit
*                       change to >10 for micro-code
*                       change rbitdt to read from TEST
INVBIT  EQU     >01                     wafer write invert
I123C   EQU     >AA                     clear int1, 2 & 3 flags
I2C     EQU     >88                     clear int2 flag
I2CS    EQU     >8C                     clear and select int2
I23C    EQU     >AB                     clear int2 & 3 flags
I23CS   EQU     >BC                     clear and select int2 & 3
I3C     EQU     >A0                     clear int3 flag
I3CS    EQU     >B0                     clear and select int3
I3FLAG  EQU     >A0                     test int3 flag bit
IRQ     EQU     >01                     bus data ready bit test
LSN     EQU     >0F                     mask to clear msn
MT      EQU     >08                     turn on motor
MTSN    EQU     >0C                     turn on motor & sensor
MTWE    EQU     >0A                     turn on motor & WE
OK      EQU     >00                     ok status code
RELEAS  EQU     >01                     release hsk bit
SETBIT  EQU     >01                     store 1 bit
```

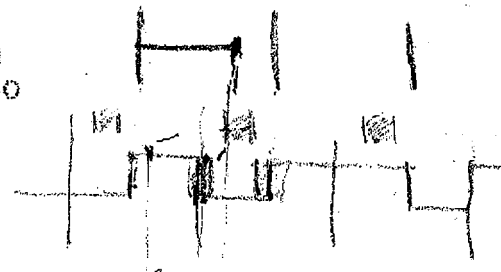
```
START   EQU     >80                     timer start bit
SYNCTM  EQU     >00                     sync half-bit time
TIMOUT  EQU     >FF                     time-out error code
ZERO    EQU     >00                     constant
        PAGE
*-------------------------------------------------------------------------------
* initialization
INIT    PUSH    A                       r2 is for bitcon
        MOVP    %INITDR,DRIVE           initialize drive
        MOVP    %INITWF,DDRD            initialize wafer ddr
        MOVP    %I123C,IOCNTL           initialize int1,2&3
        MOVP    %ZERO,TIMER             reset timer
        MOVP    %ENABLE,BCNTL           enable ibc
        EINT                            enable interrupts
SOM     NOP                             wait start of message
        MOVD    %9,COUNT                pab length
        MOVD    %SAB,DATAP              data pointer
        CALL    @RCVPAB                 receive pab
        CMP     %CINPUT,CCODE           test for input command
        JNE     GTPAB2
        BR      @XINPUT                 execute input
GTPAB2  CMP     %CPRINT,CCODE           test for print command
        JEQ     XPRINT
        JMP     SOM                     handle reset command
*-------------------------------------------------------------------------------
RETDL   MOVD    %2,COUNT                response length
        MOVD    %DLEN,DATAP             data pointer
        CALL    @XMTPAB                 return zero dl
        MOVP    %HSKSET,BCNTL           release hsk
RTSTAT  MOVD    %1,COUNT                status length
        MOVD    %STATUS,DATAP           data pointer
        CALL    @XMTPAB                 return status
        MOVP    %HSKSET                 release hsk
        JMP     SOM                     wait for som
        PAGE
*-------------------------------------------------------------------------------
* receive bus & write wafer
XPRINT  MOVD    %WBITDT,INT2V           set up int2 vector
        MOVP    %>1F,TIMER              set up max prescaler
        MOVP    %>FF,TIME               set up max time
        MOV     %5,BITCON               set up macro loop
        MOVP    %I25C,IOCNTL            select & clear int2
        MOVP    %MTSN,DRIVE             turn on motor & sensor
EOTW    BTJOP   %EOT,WAFER,EOTW         wait for EOT
        MOVP    %MTWE,DRIVE             turn on motor & WE
        MOVP    %>9F,TIMER              start BOT timer
BOTW    BTJO    %>FF,BITCON,BOTW        wait for safe area
        MOVP    %SYNCTM,TIME            set up sync bit time
        MOVD    %99,NIBCON              set up for 99 nibbles of sync
        MOV     %8,BITCON               set up nibble bit-counter
        MOV     %>F,B                   set up sync data
        CLR     CHKSUM                  zero checksum
        CLR     CHKSUM-1
        MOVP    %>80,PSCALE             start data timer
        MOVP    %HSKSET,BCNTL           let hsk float
WSYNC   BTJO    %>0F,BITCON,WSYNC       test for end of nibble
        MOV     %>8,BITCON              restart nibble bit-counter
        DJNZ    COUNT,WSYNC             test for end of sync
        MOVD    DLEN,NIBCON             move dl to nibcon
        RL      NIBCON                  multiply nibcon by 2
        RLC     NIBCON-1                (byte count -> nibble count)
        CLR     B                       clear b (start nibble)
```

```
          MOV     %8,DLPCNT                       non-linear dl counter
WTSNDL    BTJO    %>0F,BITCON,WTSNDL              wait for end of nibble
          MOV     %>8,BITCON                      restart nibble bit-counter
          BTJO    %>C,DLPCNT,WLSB                 test for next dl byte
          MOV     DLEN-1,B                        get ms byte
          JMP     WRTDL
WLSB      MOV     DLEN,B                          get ls byte
          SUB     %2,DLPCNT                       non-linear adjust
WRTDL     BTJZ    %1,DLPCNT,WRTDL2                test for ls/ms nibble
          SWAP    B                               ms nibble
WRTDL2    DJNZ    DLPCNT,WTSNDL                   test for end of dl
WRTDL3    BTJO    %>0E,BITCON,WRTDL3              test for 3 & 1/2 bits done
          MOVP    %BITIME,TIME                    set up real bit time
          JMP     WNIBD2
* receive bus & write wafer
* critical path for writing to microtape
WNIBDT    BTJO    %>0F,BITCON,WNIBDT              wait for end of nibble
          MOV     %>0B,BITCON                     restart bit counter
          MOV     A,B                             move data through queue
          BTJOP   %IRQ,BSTAT,BUSERR               test for bus data ready
          MOVP    %RELEAS,BCNTL                   reset irq
          MOVP    BDATA,A                         read data from bus
          MOVP    %HSKSET,BCNTL                   let hsk float
          AND     %LSN,A                          clear msn for checksum
          ADD     A,CHKSUM                        add data to checksum
          ADC     %0,CHKSUM-1
* eot test must be added
WNIBD2    DECD    NIBCON                          decrement nibble counter
          JC      WNIBDT                          test for end of data

          MOV     %8,DLPCNT                       non-linear counter
WCHKSM    BTJO    %>0F,BITCON,WCHKSM              wait for end of nibble
          MOV     %>8,BITCON                      restart nibble counter
          BTJO    %>C,DLPCNT,WCLSB                test for ms/ls byte
          MOV     CHKSUM-1,B                      get ms byte
          JMP     WRTCSM
WCLSB     MOV     CHKSUM,B                        get ls byte
          SUB     %2,DLPCNT                       non-linear adjust
WRTCSM    BTJZ    %1,DLPCNT,WRTCS2                test for ms/ls nibble
          SWAP    B                               ms nibble
WRTCS2    DJNZ    DLPCNT,WTSNDL                   test for end of chksum
WLAST     BTJO    %>0F,BITCON,WLAST               wait for end of nibble
          MOVP    %ZERO,DRIVE                     turn drive off
          MOV     %OK,STATUS                      set up ok status
          MOVD    %0,DLEN                         return zero data length
          BR      @RETDL
*--------------------------------------------------------------------------
* interrupt 2 routine for wafer write
WBITDT    DEC     BITCON                          decrement bit counter
          BTJZ    %1,BITCON,WINVRS                test for 2nd bit-half
          MOVP    B,WAFER                         output true bit-half
          RR      B                               rotate data right
          RETI
WINVRS    XORP    %INVBIT,WAFER                   inverted output
          RETI
          PAGE
*--------------------------------------------------------------------------
USERR     BR      @HSKERR                         bus time-out error
          PAGE
*--------------------------------------------------------------------------
* read wafer & transmit bus
XINPUT    MOVD    %WBITDT,INT2V                   set up int2 vector
```

```
        MOVP    %>1F,PSCALE                     set up max prescale
        MOVP    %>FF,TIME                       set up max time
        MOV     %6,BITCON                       set up macro loop
        MOVP    %I2SC,IOCNTL                    select & clear int2
        MOVP    %MTSN,DRIVE                     turn on motor & sensor
EOTR    BTJOP   %EOT,WAFER,EOTR                 wait for EOT
        MOVP    %MT,DRIVE                       turn on motor only
        MOVP    %>8E,TIMER                      start timer
        MOVD    %ISYNC2,INT2V                   set up int2 vector
        MOVD    %ISYNC3,INT3V                   set up int3 vector
BOTR    BTJO    %>FF,BITCON,BOTR                wait for safe area
        MOVP    %>82,PSCALE                     set up prescale of 3
*
********** times will be for half-bits, prescale = 6 ? ******
*
        MOVP    %I23SC,IOCNTL                   clear & select int2&3
        IDLE                                    wait for tape transition
        MOV     %>20,BITCON                     set up valid-bit counter
        CLR     CHKSUM                          clear chksum
        CLR     CHKSUM-1
RSYNC   IDLE                                    wait for next trahsition
        MOVP    CAPTUR,B                        read bit time
        INV     B                               get true count
        ADD     B,CHKSUM                        add to cumulative
        ADC     %0,CHKSUM-1
        DJNZ    BITCON,RSYNC                    test for end of sync sample
*
********** add check for bit time in above loop **************
*
SHFTIM  MOV     %5,BITCON                       divide cumulative by >20
        RR      CHKSUM-1                        shift msb right
        RRC     CHKSUM
        DJNZ    BITCON,SHFTIM                   test for end of divide
        MOV     CHKSUM,B
        MOVP    B,TIME                          set up 2/3 bit timer
        MOVD    %RBITDT,INT2V                   set up int2 vector
*
********** arrange for start of bit testing ******************
*           start timer at mid bit
PREPDL  CLR     NIBCON                          set nibble count to 0
        CLR     NIBCON-1
        CLR     CHKSUM                          set chksum to 0
        CLR     CHKSUM-1
        MOVP    %RCVBUS,DDRC      SET UP FOR STATUS
        MOVP    %RCVIO,RCVNIB     SET UP FOR FIRST I/O
        MOV     %8,BYTCON         NON LINEAR COUNTER FOR DL
        MOV     %4,BITCON         SET UP NIBBLE BIT COUNTER
STARTW  BTJO    %>F,B,STARTW      WAIT FOR START NIBBLE
        BTJO    %7,BITCON,RNIBD2  WAIT TO COLLECT NIBBLE
        MOV     %4,BITCON         RESTART NIBBLE BIT-COUNT
        JMP     RDLCS
RNIBDL  BTJO    %7,BITCON,RNIBDL  WAIT FOR END OF NIBBLE
        MOV     %4,BITCON           RESTART NIBBLE BIT-COUNT
        BTJZP   %HSKTST,RCVNIB,WERR2 NICE TO CUT OUT
        AND     %LSN,B              MASK OFF MSN
        OR      %CSR8RW,B         PREPARE FOR XMIT
        MOVP    %XMTBUS,DDRC      SET UP FOR OUTPUT
        MOVP    B,XMTNIB          SET UP DATA
        XORP    %XMTRW,XMTNIB     SEND NIBBLE
        XORP    %XMTRW,XMTNIB
        MOVP    %XMTIO,XMTNIB     TOGGLE HSK
        XORP    %XMTRW,XMTNIB
```

```
         XORP   %HSKRST,XMTNIB
         XORP   %XMTRW,XMTNIB
         MOVP   %RCVBUS,DDRC       SET UP FOR STATUS CHECK
RDLCS    AND    %LSN,B             MASK OFF MSN
         ADD    B,CHKSUM           ADD NIBBLE TO CHKSUM
         ADC    %0,CHKSUM-1
         BTJZ   %1,BYTCON,RNIBL2   TEST FOR MS/LS NIBBLE
         SWAP   B                  MS NIBBLE
RNIBL2   BTJO   %>C,BYTCON,RLSB    TEST FOR NEXT BYTE OF DL
         OR     B,COUNT-1          STORE MS BYTE
         JMP    RNIBL3
*--------  ---------  ----------  ----------
WERR2    BR     @HSKERR            BUS TIME ERROR
*--------  ---------  ----------  ----------
RLSB     OR     B,COUNT            STORE LS BYTE
         SUB    %2,BYTCON          NON-LINEAR ADJUST
RNIBL3   DJNZ   BYTCON,RNIBDL      TEST FOR END OF DL
* read wafer & transmit bus
* critical path for reading from microtape
RNIBDT   BTJO   %>07,BITCON,RNIBDT      wait for end of nibble
         MOV    %>04,BITCON             restart bit counter
         MOV    B,A                     move data through queue
         CLR    B                       set all input bits to 0
         BTJOP  %HSK,BSTAT,BUSERR       test for inactive bus
         MOVP   A,BDATA                 send data over bus
         MOVP   %DROP,BCNTL             drop hsk
         MOVP   %HSKSET,BCNTL           let hsk float
         AND    %LSN,A                  clear msn for checksum
         ADD    A,CHKSUM                add data to checksum
         ADC    %0,CHKSUM-1
         DECD   NIBCON                  decrement nibble counter
         JC     RNIBDT                  test for end of data

RNIBDT   MOV    %2,BYTCON          SET UP BYTE NIBBLE-COUNT
RNIBD2   BTJO   %7,BITCON,RNIBD2   WAIT FOR END OF NIBBLE
         MOV    %4,BITCON             RESTART NIBBLE BIT-COUNT
         BTJZP  %HSKTST,RCVNIB,WERR2 NICE TO CUT OUT
         AND    %LSN,B                MASK OFF MSN
         OR     %CSRSRW,B           PREPARE FOR XMIT
         MOVP   %XMTBUS,DDRC        SET UP FOR OUTPUT
         MOVP   B,XMTNIB            SET UP DATA
         XORP   %XMTRW,XMTNIB       SEND NIBBLE
         XORP   %XMTRW,XMTNIB
         MOVP   %XMTIO,XMTNIB       TOGGLE HSK
         XORP   %XMTRW,XMTNIB
         XORP   %HSKRST,XMTNIB
         XORP   %XMTRW,XMTNIB
         MOVP   %RCVBUS,DDRC        SET UP FOR STATUS CHECK
         AND    %LSN,B              MASK OFF MSN
         ADD    B,CHKSUM            ADD NIBBLE TO CHKSUM
         ADC    %0,CHKSUM-1
         DJNZ   BYTCON,RNIBD2       TEST FOR END OF BYTE
         DECD   COUNT
         JC     RNIBDT              TEST FOR END OF DATA
         MOV    %6,BYTCON           SET UP NON-LINEAR COUNTER
RCHKSM   BTJO   %7,BITCON,RCHKSM   WAIT FOR END CHKSUM NIBBLE
         MOV    %4,BITCON             RESTART NIBBLE BIT-COUNT
         AND    %LSN,B              MASK OFF MSN
         BTJZ   %1,BYTCON,RCHKS2    TEST FOR MS/LS NIBBLE
         SWAP   B                   MS NIBBLE
RCHKS2   BTJO   %>C,BYTCON,RCHKL    TEST FOR NEXT BYTE OF
         OR     B,COUNT-1           STORE MS BYTE
```

```
          JMP     RCHK53
RCHKL     OR      B,COUNT             STORE LS BYTE
          SUB     %2,BYTCON           NON-LINEAR ADJUST
RCHKS3    DJNZ    BYTCON,RCHKSM       TEST FOR END OF CHKSUM
          MOVP    %0,SYSCON           SENSOR=0, MOTOR=0, WE=0
          SUB     COUNT,CHKSUM        VERIFY CHKSUM
          SBB     COUNT-1,CHKSUM-1
          JC      CHKSOK              TEST CHKSUM
          MOV     %6,STATUS           STORE DEVICE ERROR
          JMP     RLAST
CHKSOK    MOV     %0,STATUS           STORE OK STATUS
RLAST     BR      @RTSTAT
*---------------------------------------------------------------
* interrupt 2 routine for wafer read
RBITDT    ORP     %I3C,IOCNTL                 clear interrupt 3 flag
          DEC     BITCON                      decrement bit counter
          RR      B                           rotate data right
RBITD2    BTJZP   %I3FLAG,IOCNTL,RBITD2       wait for int3 flag
          MOVP    %START,TIMER                restart timer
          BTJZP   %INPUT,WAFER,RBITD3         test for 0 input bit
          OR      %SETBIT,B                   if not zero, set bit
RBITD3    RETI
*---------------------------------------------------------------
ISYNC2    MOVP    %>20,BITCON                 restart sync bit-counter
          RETI
*---------------------------------------------------------------
ISYNC3    MOVP    %>82,TIMER                  restart timer
          DEC     BITCON                      decrement bit counter
          RETI
          PAGE
*---------------------------------------------------------------
HSKERR    MOVD    %0,DLEN                     return no data
          MOV     %TIMOUT,STATUS              return time-out error
          BR      @RETDL
*---------------------------------------------------------------
* receive and store data from bus
RCVPAB    DECD    COUNT                       decrement byte counter
          JC      RNXPAB                      test for non-zero dl
          RETS
RNXHSK    MOVP    %HSKSET,BCNTL               release hsk
RNXPAB    CALL    @RCVNRM                     receive lsd, raise hsk
          MOV     B,A                         save lsd
          CALL    @RCVABN                     receive msd, hold hsk
          SWAP    B                           justify byte
          OR      B,A                         combine nibbles
          STA     *DATAP                      store byte
          DECD    DATAP                       decrement pointer
          DECD    COUNT                       decrement counter
          JC      RNXHSK                      test for end of data
          RETS
*---------------------------------------------------------------
* load and transmit data to bus
XMTPAB    DECD    COUNT                       decrement counter
          JC      WNXPAB                      test for non-zero dl
          RETS
WNXHSK    MOVP    %HSKSET,BCNTL               release hsk
WNXPAB    LDA     *DATAP                      load data into a
          MOV     A,B                         move nibble into b
          CALL    @XMTNRM                     transmit lsd, raise hsk
          SWAP    A                           position data
          MOV     A,B                         move nibble into b
          CALL    @XMTABN                     transmit msd, hold hsk
```



Co Routine

Read bit

looking

```
        DECD    DATAP                   decrement pointer
        DECD    COUNT                   decrement counter
        JC      WNXHSK                  test for end of data
        RETS
        PAGE
*-------------------------------------------------------------------------------
* receive nibble from bus
RCVNRM  BTJZP   %IRQ,BSTAT,RXERR        test for bus data ready
        MOVP    %RELEAS,BCNTL           reset irq
        MOVP    BDATA,B                 read data from bus
        MOVP    %HSKSET,BCNTL           let hsk float
        AND     %LSN,B                  clear msn
        RETS
RCVABN  BTJZP   %IRQ,BSTAT,RXERR        test for bus data ready
        MOVP    %RELEAS,BCNTL           reset irq
        MOVP    BDATA,B                 read data from bus
        AND     %LSN,B                  clear msn
        RETS
        PAGE
*-------------------------------------------------------------------------------
RXERR   BR      @HSKERR                 bus timeout
*-------------------------------------------------------------------------------
* transmit nibble to bus
XMTNRM  BTJZP   %HSK,BSTAT,RXERR        test for bus ready
        MOVP    B,BDATA                 send data over bus
        MOVP    %DROP,BCNTL             drop hsk
        MOVP    %HSKSET,BCNTL           let hsk float
        RETS
XMTABN  BTJZP   %HSK,BSTAT,RXERR        test for bus ready
        MOVP    B,BDATA                 send data over bus
        MOVP    %DROP,BCNTL             drop hsk
        RETS
        PAGE
*-------------------------------------------------------------------------------
INT1    BR      *INT1V                  indirect branch
INT2    BR      *INT2V                  indirect branch
INT3    BR      *INT3V                  indirect branch
*-------------------------------------------------------------------------------
        AORG    >FFD0
        DATA    ZERO                    trap 23
        DATA    ZERO                    trap 22
        DATA    ZERO                    trap 21
        DATA    ZERO                    trap 20
        DATA    ZERO                    trap 19
        DATA    ZERO                    trap 18
        DATA    ZERO                    trap 17
        DATA    ZERO                    trap 16
        DATA    ZERO                    trap 15
        DATA    ZERO                    trap 14
        DATA    ZERO                    trap 13
        DATA    ZERO                    trap 12
        DATA    ZERO                    trap 11
        DATA    ZERO                    trap 10
        DATA    ZERO                    trap 09
        DATA    ZERO                    trap 08
        DATA    ZERO                    trap 07
        DATA    ZERO                    trap 06
        DATA    ZERO                    trap 05
        DATA    ZERO                    trap 04
        DATA    INT3                    interrupt 3
        DATA    INT2                    interrupt 2
        DATA    INT1                    interrupt 1
```

DATA INIT reset

```
10 CLEAR ,49140!
20 XMIT=&HC041
30 RCV=&HC070
40 BUF=&HC0A6
50 A$="F1G?E?E8$"
60 LENGTH=16
70 GOSUB 820
80 DIM A(100)
85 VMIN=1000
86 VMAX=0
90 FOR J=1 TO N
100 GOSUB 1020
110 Q$=INKEY$
120 IF LEN(Q$)=0 THEN 140
130 IF ASC(Q$)=17 THEN 230
140 X=X*1E+06-CORR
150 PRINT J,X
152 IF X<VMIN THEN VMIN=X
154 IF X>VMAX THEN VMAX=X
160 IF X<RMIN OR X>RMAX THEN 100
170 IF X<MIN THEN ERRMIN=ERRMIN+1:GOTO 100
180 IF X>MAX THEN ERRMAX=ERRMAX+1:GOTO 100
190 SLOT=(X-MIN)/((MAX-MIN)/100)
200 A(SLOT)=A(SLOT)+1
210 NEXT J
220 GOTO 240
230 N=J-1
240 REM PRINT DATA
250 LPRINT "TEST DATE AND TIME: ";M$
260 LPRINT "TEST NAME: ";N$
270 LPRINT CORR;" MICROSECONDS SUBTRACTED FROM COUNTER READING PRIOR TO QUALIF
ATION"
280 LPRINT "REJECTED BELOW ";RMIN;" MICROSEC AND ABOVE ";RMAX;" MICROSEC"
290 LPRINT "LOW LIMIT IS ";MIN;" MICROSEC AND HIGH LIMIT IS ";MAX;" MICROSEC"
300 LPRINT ERRMIN;" LESS THAN LOW LIMIT ( ";ERRMIN/N*100;"%)"
310 LPRINT ERRMAX;" GREATER THAN HIGH LIMIT ( ";ERRMAX/N*100;"%)"
320 LPRINT "SIGMA X ";SUM1
322 LPRINT "MIN TIME WAS ";VMIN
324 LPRINT "MAX TIME WAS ";VMAX
326 LPRINT "SIGMA X^2 ";SUM2
330 LPRINT "FOR ";N;" DATA POINTS MEASURED"
340 LPRINT
350 LPRINT "TIMING DISTRIBUTION IN 100 BINS"
360 LPRINT
370 LPRINT "      ";
380 FOR L=1 TO 10
390 LPRINT USING "#####";L;
400 NEXT L
410 LPRINT
420 LPRINT
430 FOR J=0 TO 9
440 LPRINT USING "#####";10*J;
450 LPRINT "  ";
460 FOR K=1 TO 10
470 LPRINT USING "#####";A(10*J+K);
480 NEXT K
490 LPRINT
500 NEXT J
510 LPRINT
520 LPRINT
530 LPRINT "CUMULATIVE PROBABILITIES"
540 LPRINT "MINIMUM LIMIT"
```

SUM1=0
SUM2=0

SUM1 = SUM1 + X
SUM2 = SUM2 + X^2

```
560 LPRINT " BIN              TIME       CUM PERCENT"
570 PLIMIT=0:SUM=0
580 FOR J=1 TO 100
590 GOSUB 730
600 NEXT J
610 LPRINT
620 LPRINT
630 LPRINT "MAXIMUM LIMIT"
640 LPRINT
650 LPRINT " BIN              TIME       CUM PERCENT"
660 PLIMIT=0:SUM=0
670 FOR J=100 TO 1 STEP -1
680 GOSUB 730
690 NEXT J
700 LPRINT CHR$(12)
710 LPRINT CHR$(12)
720 END
730 REM CUMULATIVE PROBABILITY SUBROUTINE
740 SUM=SUM+A(J)
750 IF SUM=0 THEN 810
760 PROB=SUM/N%100
770 IF PROB<PLIMIT THEN 810
780 X=J%((MAX-MIN)/100)+MIN
790 LPRINT J,X,,PROB
800 PLIMIT=PROB%2
810 RETURN
820 REM GET STAT DATA
830 PRINT "ALL TIMES ARE IN MICROSECONDS..."
840 INPUT "TEST NAME? ";N$
850 INPUT "TEST DATE, TIME? ";M$
860 INPUT "NUMBER OF DATA POINTS? ";N
870 INPUT "TIMING CORRECTION CONSTANT? ",CORR
880 INPUT "REJECT MINIMUM? ";RMIN
890 INPUT "REJECT MAXIMUM? ";RMAX
900 INPUT "MINIMUM TIME FOR DATA ANALYSIS? ";MIN
910 INPUT "MAXIMUM TIME FOR DATA ANALYSIS? ";MAX
920 RETURN
930 FOR I=1 TO LEN(A$)
940 C$=MID$(A$,I,1)
950 X=ASC(C$)
960 POKE BUF+I-1,X
970 PRINT CHR$(X);
980 NEXT I
990 RETURN
1000 CALL XMIT
1010 RETURN
1020 CALL RCV
1030 A$=""
1040 FOR I=1 TO LENGTH
1050 A$=A$+CHR$(PEEK(BUF+I-1))
1060 NEXT I
1070 X=VAL(A$)
1080 RETURN
```

```
190 B(I)=INT((X-MIN)/(MAX-MIN)*100)
200 A(B(I))=A(B(I))+1
210 NEXT I
220 [illegible]
230 N=N-1
240 REM PRINT DATA
250 LPRINT "TEST DATE AND TIME: ";D$
260 LPRINT "TEST NAME: ";N$
270 LPRINT LOW$," MICROSECONDS SUBTRACTED FROM COUNTER READING PRIOR TO [illegible]
    TION"
280 LPRINT "THE [illegible] BELOW ";MIN;" MICROSEC AND ABOVE ";MAX;" MICROSEC."
290 LPRINT "LOW LIMIT IS ";MIN;" MICROSEC AND HIGH LIMIT IS ";MAX;" MICROSEC"
300 LPRINT ERROR$;" LESS THAN LOW LIMIT (";[illegible];"%)"
310 LPRINT ERROR$;" GREATER THAN HIGH LIMIT (";[illegible];"%)"
320 LPRINT
330 LPRINT "MIN TIME WAS ";MIN
340 LPRINT "MAX TIME WAS ";MAX
350 LPRINT
360 LPRINT "THE ";N;" DATA POINTS MEASURED"
370 LPRINT
380 LPRINT "TIMING DISTRIBUTION IN 100 BINS"
390 LPRINT
400 LPRINT "    ";
410 FOR I=1 TO 10
420 LPRINT USING "####";I;
430 NEXT I
440 LPRINT
450 LPRINT
460 FOR J=0 TO 9
470 LPRINT USING "####";J*10;
480 FOR I=1 TO 10
490 LPRINT USING "#####";A(I+10*J);
500 NEXT I
510 LPRINT
520 NEXT J
530 LPRINT
540 LPRINT
550 LPRINT "CUMULATIVE PERCENTAGE [illegible]"
```

SAVE "B:[illegible].BAS"
PTIME

READ

—	BTJO	11 +2 2	30
	MOV	9	19
	MOV	5	
	CLR	5	
	BTJOP	12	(+2 on error only)
	MOVP	10	33
	MOVP	11	
	MOVP	11	28
	AND	7	
	ADD	10	
	ADC	9	27
	DECD	11	
	JC	7	(-2 last time)

I/O

$\frac{120}{4} = 30$

118

94.4

← 9 for interrupt

	ORP	11
	DEC	7
	RR	5
—	BTJZP	12 +2 2
	MOVP	11
	BTJZP	12 +2
	OR	7
	RETI	9

BIT READ

? [illegible]

9 for [illegible] 3

Ø data

74+ or 69+ (+ initial time to take interrupt + 2 + n(12) BTJOP's)

59.2 55.2

nominal bit cell = 125 μs @ 10 ips

tape speed ± 5% 9.5 – 10.5

$$\frac{9.5\ in}{sec} \times \frac{125 \times 10^{-6}\ sec}{bit} = \frac{1187.5\ \mu in}{bit}$$

$$\frac{10.5\ in}{sec} \times \frac{1\ bit}{1187.5\ \mu in}$$

$$\frac{1187.5\ \mu in}{bit} \times \frac{1\ sec}{10.5\ in} = \frac{1187.5}{10.5}\ \mu s/bit = 113.09$$

Write wafer

→ BTJO	11 +2 ↩
MOV	9
MOV	6
BTJOP	12 ✓
MOVP	11
MOVP	9
MOVP	11
AND	7
ADD	10
ADC	9
(EOT) BTJOP	~~12~~ to error (EOT)
DECD	11
JC	7 (-2 last time)
	125

write bit (on cnt 2)

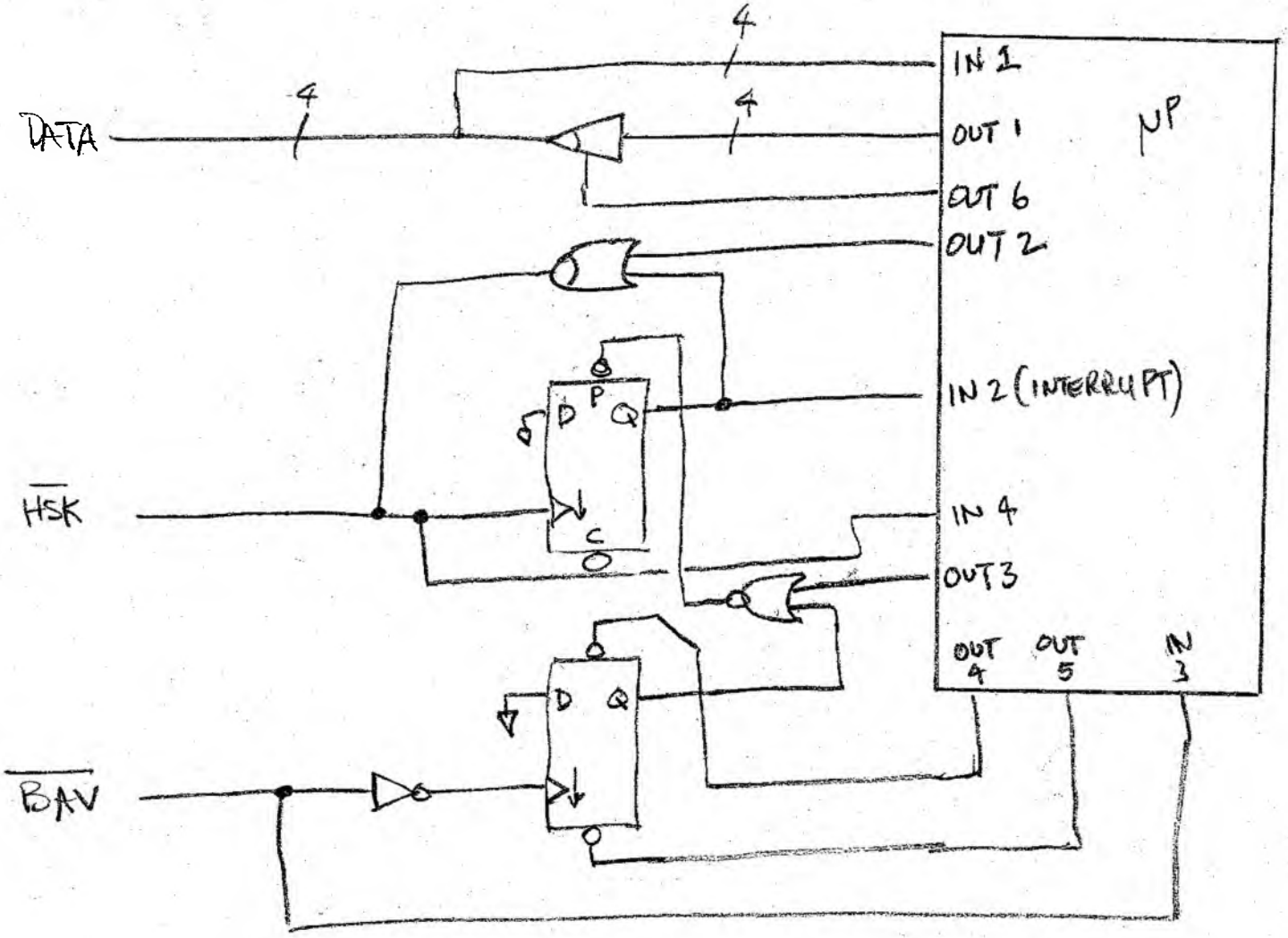
DEC	7
BTJZ	11 +2
MOVP	9
RR	5
RETI	9
XORP	11 ←
RETI	9
	41 or 40

RECEIVE

1. HSK goes low
2. latch ① responds unless inhibited by preset input
3. Latch ① output interrupts μP
4. μP look at data (take it)
5. μP clear latch (unless being overrun) by strobing OUT 3 (must clear strobe < 8μs)
6. μP handle data (could be done before 5)
7. μP inhibit latch if not addressed by strobing OUT 4 and preseting latch ②
8. Rising edge of BAV clears latch ② so latch ① will respond to next HSK.

TRANSMIT

1. μP looks at BAV to verify its low?
2. μP look at HSK to see its high
3. μP inhibit HSK latch by strobing OUT 4
4. clear bus enable?
5. μP put data on bus through OUT 1 (4) and output enable OUT 6
6. μP pull HSK low through OUT 2
7. μP let HSK go high through OUT 2
8. μP quit if through - clear inhibit through OUT 5
9. μP look at HSK to see it high through IN 4
10. When HSK is high go to step 4


4
4
4
4
DATA
IN 1
OUT 1
µP
OUT 6
OUT 2
P
D
Q
IN 2 (INTERRUPT)
HSK
C
IN 4
OUT 3
OUT 4
OUT 5
IN 3
D
Q
BAV

RCV BUS [illegible] WAFER [illegible]

[illegible] IRQ Active with first data nibble
IL in COUNT (could be same Reg)
DL tested for non zero (in [illegible] other Reg)

TRAP set up for RCVDAT

MOVD	% [illegible] INT2V	[illegible] INT2	
MOVP	% [illegible]	R - MOV HALF BIT TIME, A MOV A, TIME	variable HALF BIT TIME
MOV	% 2 COUNT2		
MOV	COUNT, NTBOUT	ISR → NTBOUT	
MOV	COUNT, NTBIN		
SWAP	NTBIN	3 MSN → NTBIN	
MOVP	% 125C, TOCNTL	INT2 SELECT & CLEAR	
EINT			
MOVP	% BIT TIMER, TIMER	START TIMER	
[illegible]			
MOVD	% WDAT INT2V	DATA INT2 — when 2nd half [illegible] bit ends, after [illegible] position to write [illegible]	
BDLY MOV	%3, NTBCON		
BD2 IDLE			
(9) DJNZ	NTBCON, WAITBD2		
(10) MOV	NTBIN, NTBOUT		
(16) MOV	COUNT-1, NTBIN		
(9) DJNZ	COUNT2, WAITBDL		
(10) SWAP	NTBIN		
WTBDT (11) MOV	%2, COUNT2	11	
BD3 (12) MOV	%1, NTBCON	4	critical loop
BD4 (6) IDLE		6	
(9) DJNZ	NTBCON, WAITBD4	9	
(10) MOV	NTBIN, NTBOUT	10	
(11) TRAP	RCVDI → Calls RCVDAT next page	11	
(9) DJNZ	COUNT2, WAITBD3	9	
(11) DECD	COUNT	11	
(5) JC	WAITBDT	5	
		84	11
(11) MOV	%8, NTBCON	60	X
BD5 IDLE			
(8) DJNZ	NTBCON, WAITBD5	44	8
(2) DINT			2
			10

timeout sampling IRQ

1	84
X	46
3	130
1	
1	
1	
46	

TI MICROTAPE READ/WRITE CIRCUIT

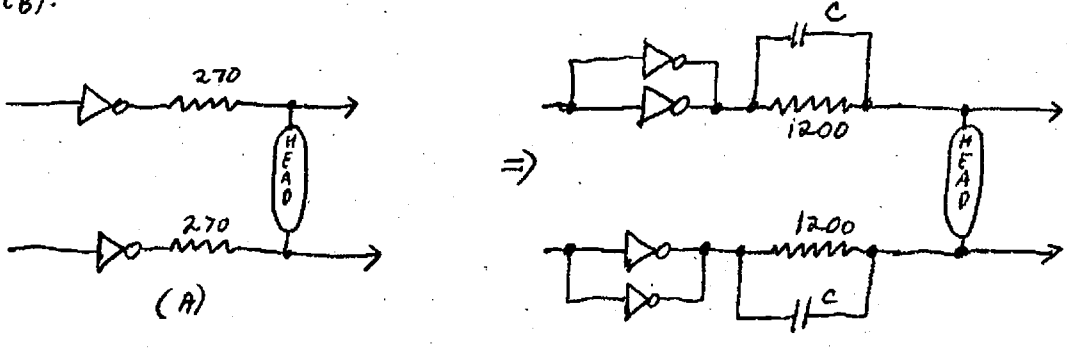
THE FOLLOWING PICTURES ILLUSTRATE COMPARATIVE PERFORMANCE BETWEEN THE TI MICROTAPE AND THE EXATRON STRINGY. WE USED THE EXATRON STRINGY PHOTOS AS A "BASELINE" VALUE, BECAUSE OF OUR FAMILIARITY WITH THE CIRCUIT. COMPARISONS WERE MADE AT 4 KHZ, 8 KHZ, & 12 KHZ. BOTH CURRENTS & VOLTAGES WERE PHOTOGRAPHED.

INITIAL PERFORMANCE:

EXATRON		MICROTAPE	
7-9%	JITTER	12-13%	<CURRENT>
16 MS	ZERO CROSSING TIME	12 MS	<CURRENT>
ACCEPTABLE	SATURATION (VOLTAGE)*	POOR	

*-OBSERVED BY THE "RETURN TO ZERO" OF THE DIFFERENTIAL VOLTAGE ACROSS THE HEAD

AFTER ANALYSIS, THE WRITE CIRCUITRY WAS MODIFIED FROM (A) TO (B):



(A) (B)

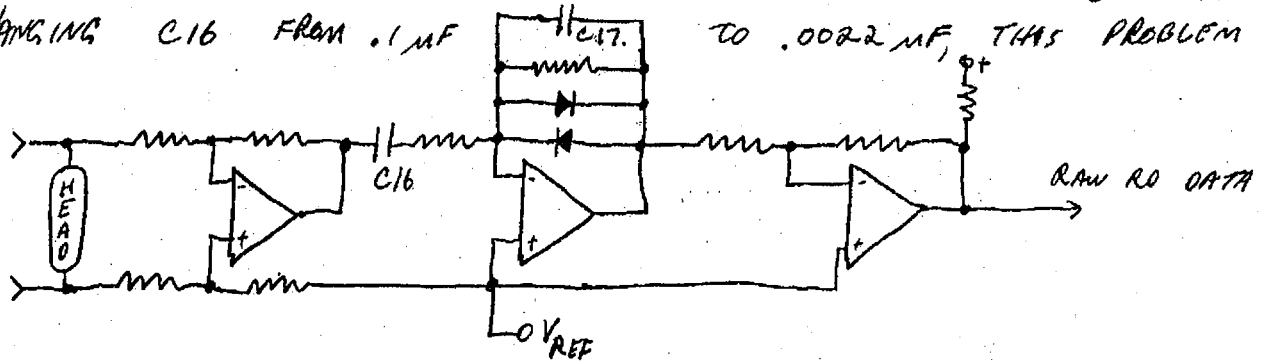
THIS WAS DONE TO IMPROVE CURRENT RISE AND FALL TIMES AND TO PROVIDE INCREASED PERFORMANCE

	NEW CIRCUIT	OLD CIRCUIT	EXATRON	UNITS
CURRENT SUPPLY (MAX)	8.7	4.35	18	MA
ZERO CROSSING TIME	<3	12	16	MS
JITTER	6%	12-13%	7-9%	
MAX/MIN/ HEAD CURRENT	4.5	8	15	MA
SATURATION VOLTAGE*	GOOD	POOR	ACCEPTABLE	

THE CAPACITOR VALUE C WAS CHOSEN AFTER OPTIMIZING THE RESISTANCE (1200Ω) AND WAS CHOSEN BECAUSE OF THE RESONANT FREQUENCY OF THE RLC NETWORK (AT 8 KHZ). NOTE THE SHARP RISE + FALL TIMES OF THE CURRENT WAVEFORM (PLATE #36) AND THE ~~FAIRLY~~ QUICK WRITE VOLTAGE "RETURN TO ZERO" TIME.

COMPARISONS BETWEEN THE THREE CIRCUIT PERFORMANCES ARE ON THE NEXT PAGE.

ONE ADDITIONAL PROBLEM WAS FOUND WITH THE READ CIRCUIT. IT COULD REPRODUCE A SQUARE WAVE VERY ACCURATELY (≈6% JITTER) BUT COULD NOT REPRODUCE SKEWED WAVEFORMS. (THIS PROBLEM WAS EXPERIENCED BY JEFF IN THAT HE COULD ACQUIRE SYNC FIND (A SQUARE WAVE) BUT COULD NOT ACQUIRE THE START NIBBLE (A SKEWED WAVEFORM). ~~FEED~~ FEEDING THE READ CIRCUIT A 33% DUTY CYCLE SQUARE WAVE SHOWED THIS CLEARLY. BY CHANGING C16 FROM .1 μF TO .0022 μF, THIS PROBLEM CLEARED

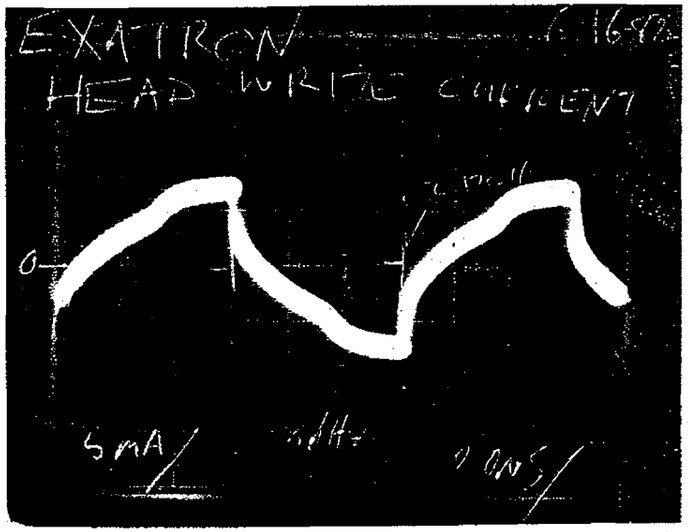


UP. IT ALSO REDUCED THE JITTER BY A LITTLE, AS WELL.

NOTE THAT IN SEVERAL "READ DATA" PHOTOS, ON BOTH THE HEAD AND THE 1ST STAGE OUPUT, 2 GLITCHES / CYCLE SHOW. THIS IS A REAL PART OF THE CIRCUIT AND IS ELIMINATED BY C17

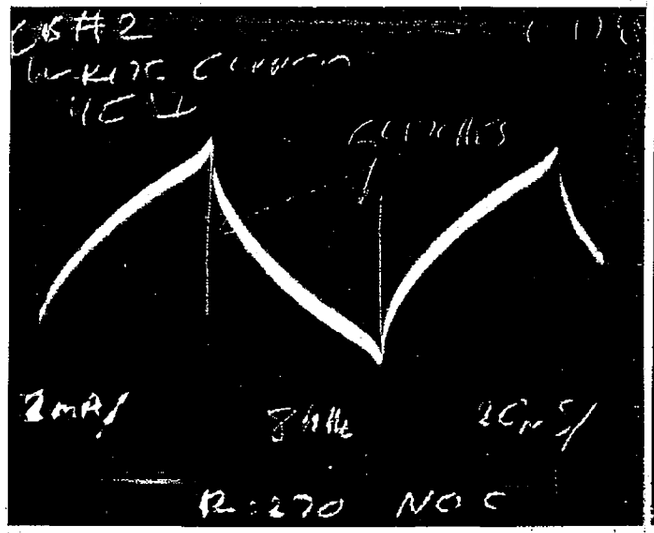
COMPARITIVE PERFORMANCE

EXATRON HEAD WRITE CURRENT



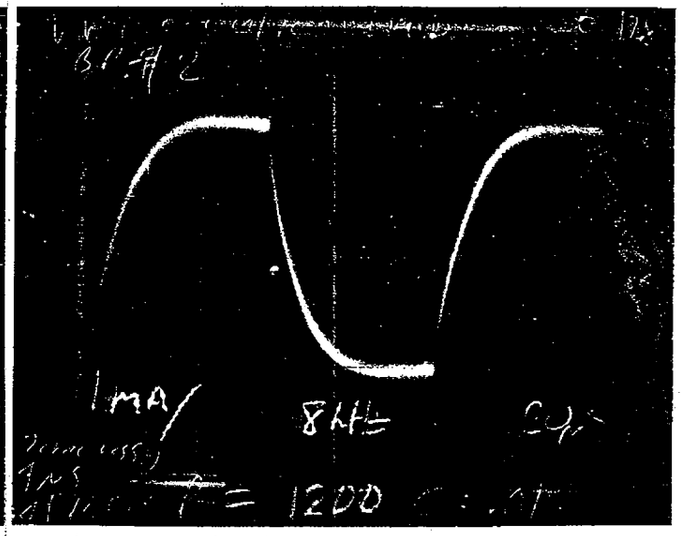
5 mA/DIVISION - 20μS/DIVISION @8KHZ

MICROTAPE - OLD CIRCUIT - WRITE CURRENT



2 mA/DIVISION - 20μS/DIVISION @ 8KHZ

MICROTAPE - NEW CIRCUIT - WRITE CURRENT



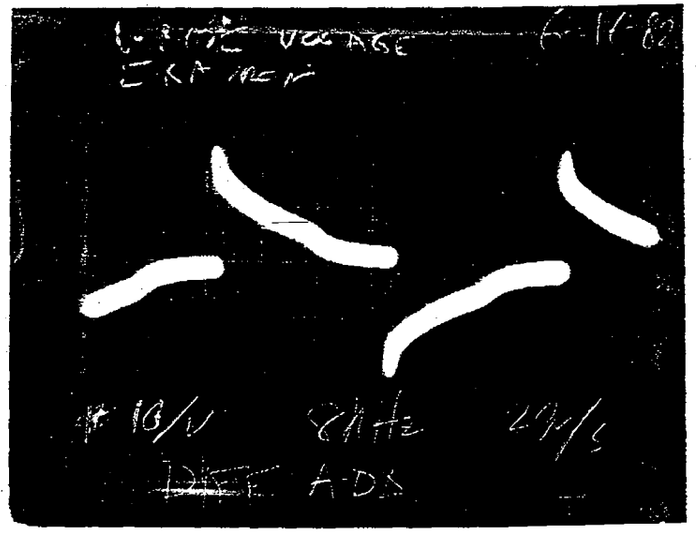
1 mA/DIVISION - 2μs/DIVISION @8KHZ

ZERO CROSSING -	16μS	12μS	<3μS
JITTER -	7-9%	12-13%	6%
RISE TIME* -	22μS	34μS	12μS

*TO 2/3 FINAL VALUE

COMPARATIVE PERFORMANCE

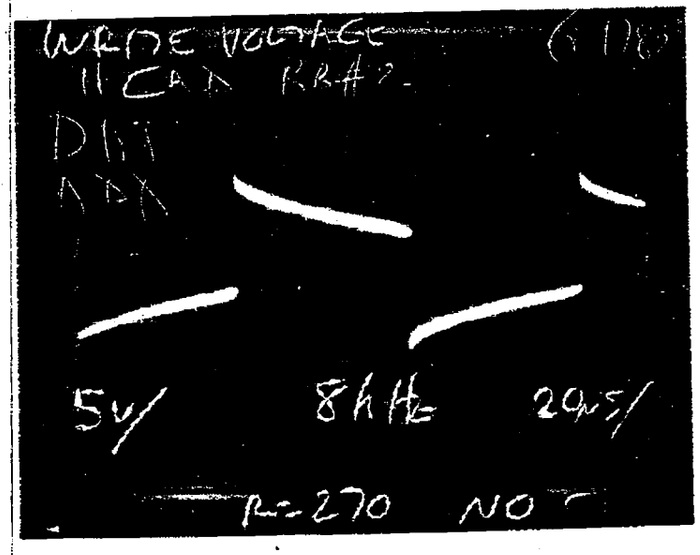
EXATRON HEAD WRITE VOLTAGE



10 V/DIVISION - 20 μS/DIVISION @ 8KHZ

TIME CONSTANT* 24 μS
RELATIVE MERIT ACCEPTABLE

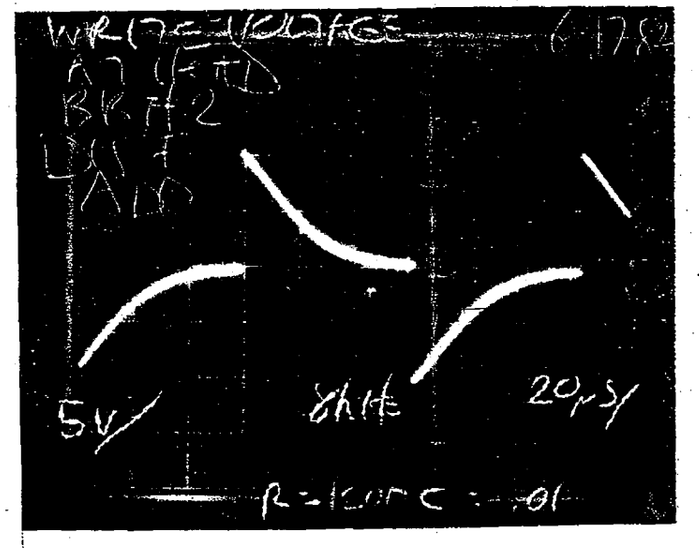
MICROTAPE - OLD CIRCUIT - WRITE VOLTAGE



5V/DIVISION - 20 μS/DIVISION @ 8KHZ

62 μS
VERY POOR

MICROTAPE - NEW CIRCUIT WRITE VOLTAGE

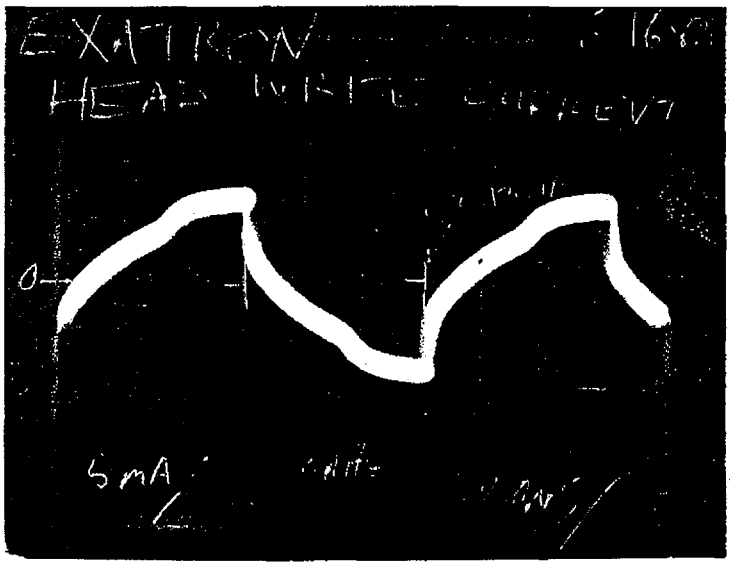


5V/DIVISION - 20 μS/DIVISION - @8KHZ

24 μS
GOOD

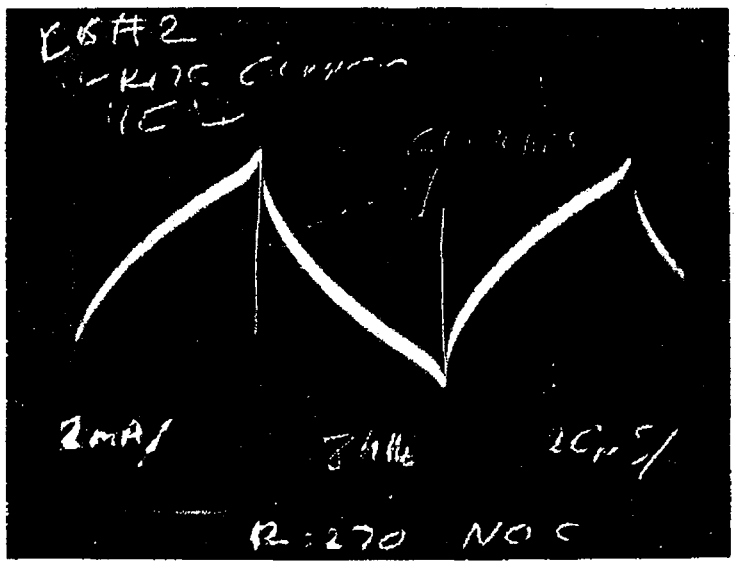
* to the 2/3 FINAL VOLTAGE VALUE (0V DIFFERENTIAL)

#1



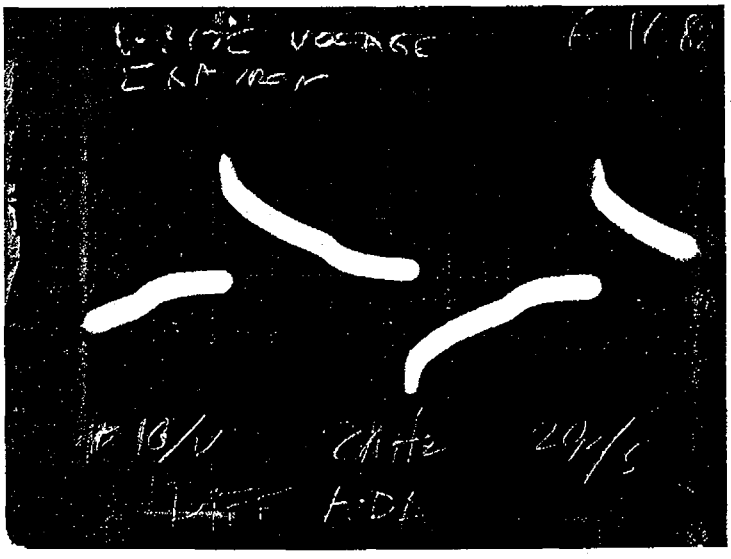
EXATRON HEAD WRITE CURRENT
5 mA/ 20 μS/ 8 kHz

#2



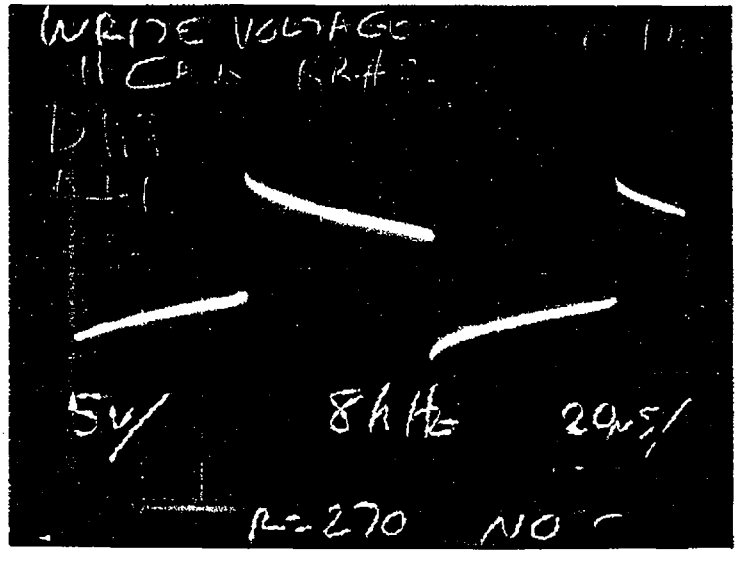
BB#2 HEAD WRITE CURRENT
2 mA/ 20 μS 8 kHz

#3



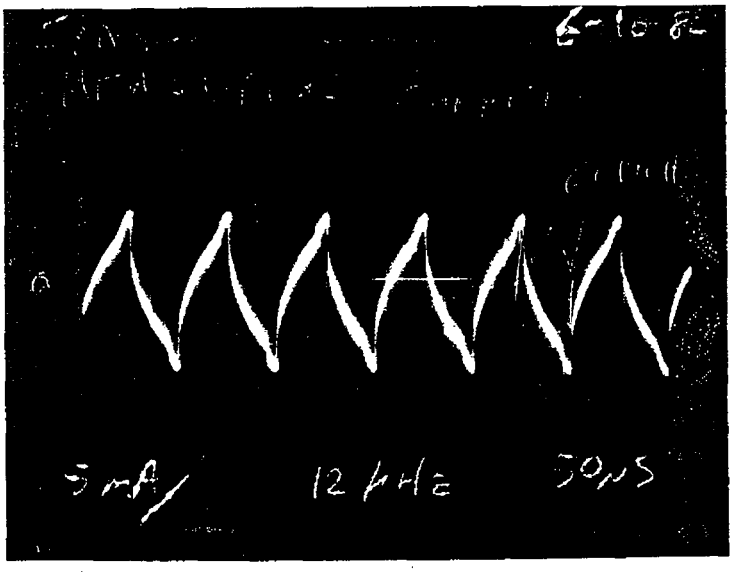
EXATRON HEAD WRITE VOLTAGE
10V/ 20 μS/ 8 kHz

#4



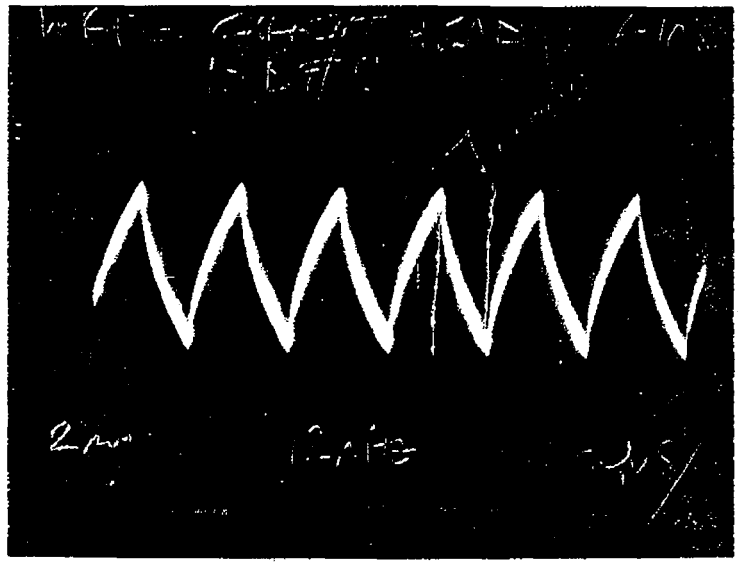
BB#2 HEAD WRITE VOLTAGE
5V/ 20 μS/ 8 kHz

#5



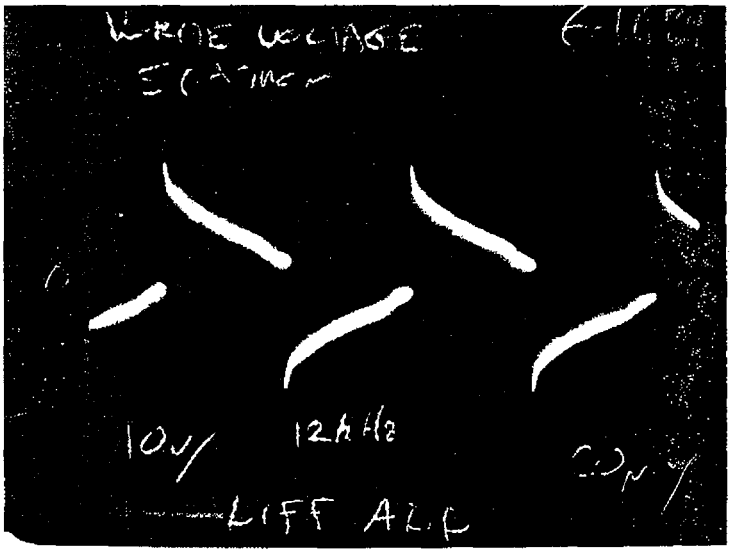
EXATRON HEAD WRITE CURRENT
5mA/ 50nS/ 12kHz

#6



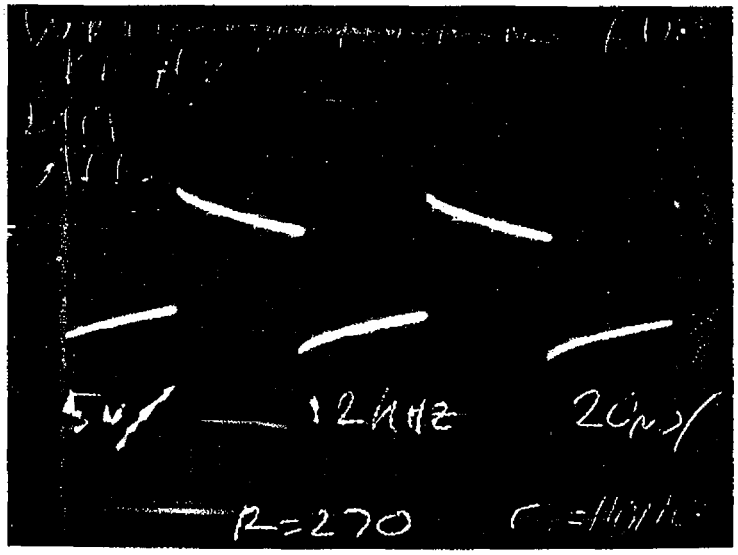
BB#2 HEAD WRITE CURRENT
2mA/ 50nS/ 12kHz

#7



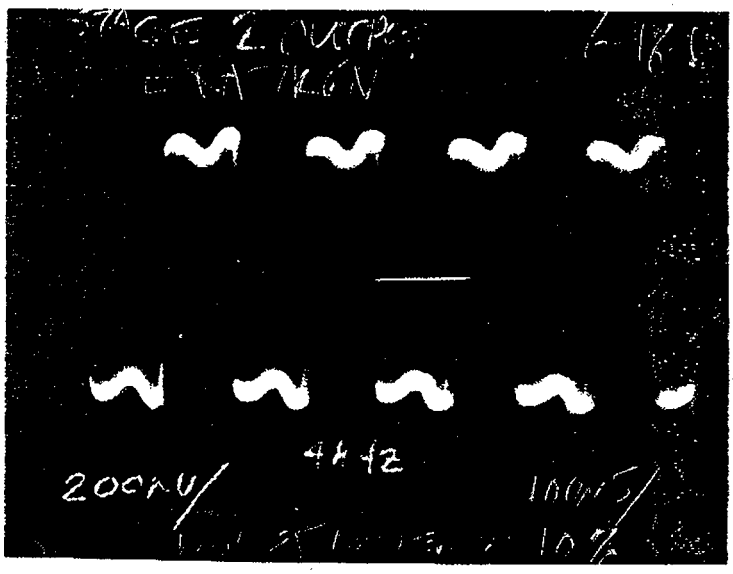
EXATRON HEAD WRITE VOLTAGE
10V/ 20nS/ 12kHz

#5



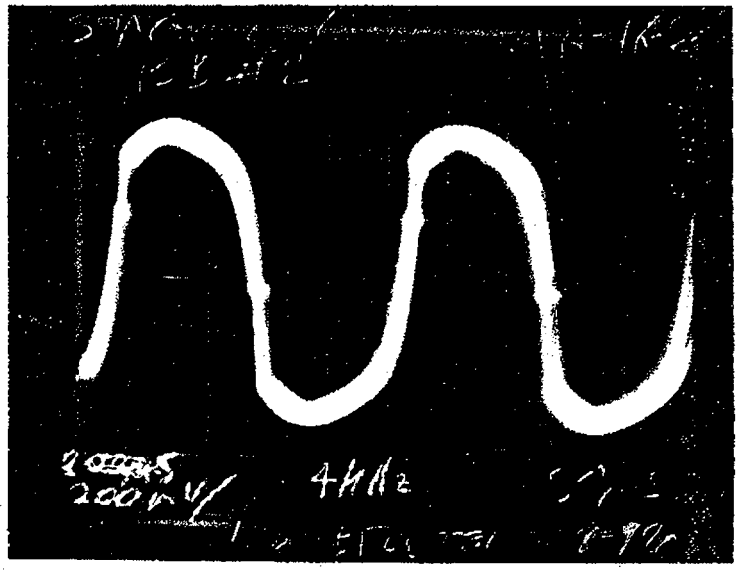
BB#2 HEAD WRITE VOLTAGE
5V/ 20nS/ 12kHz

#9



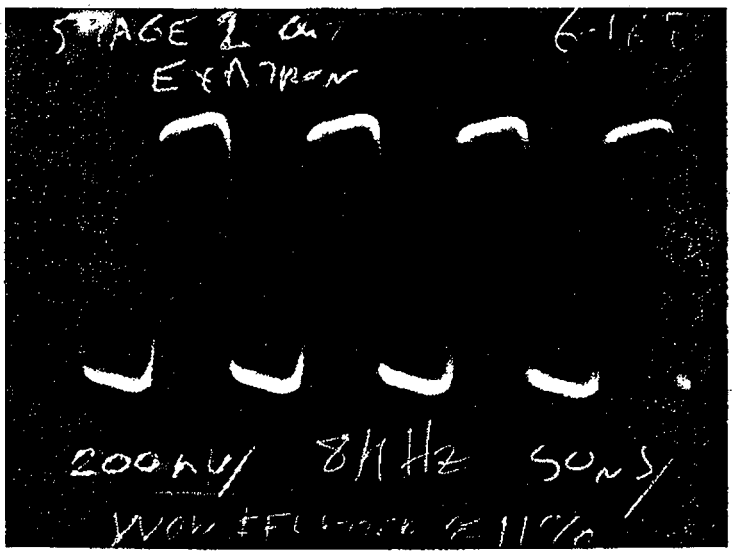
EXATRON READBACK SIGNAL FROM TAPE
STAGE 2 OUTPUT
200mV/ 100mS/ 4HHz
JITTER ≈ 10%

#10



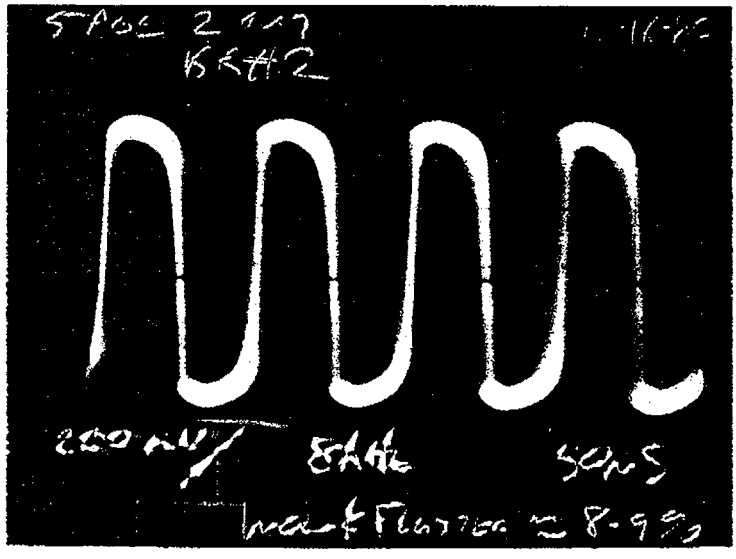
BB#2 READBACK SIGNAL FROM TAPE
STAGE 2 OUTPUT
200mV/ 50mS/ 4HHz
JITTER ≈ 9%

#11



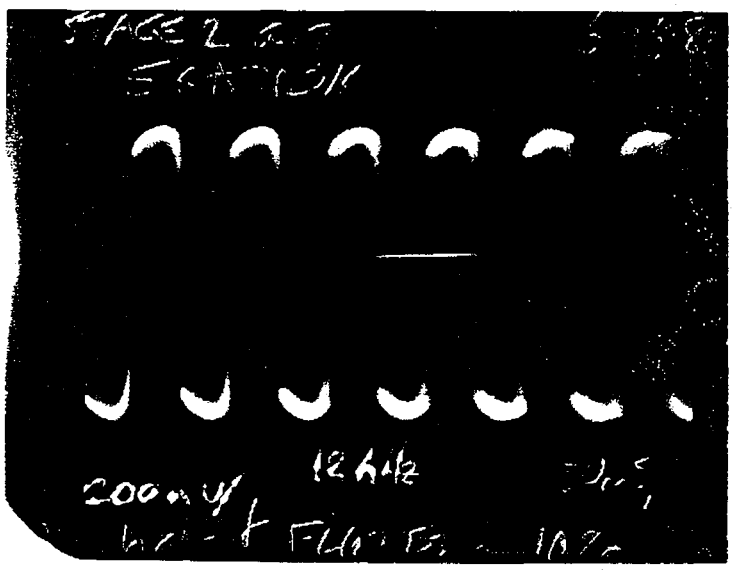
EXATRON READBACK SIGNAL
STAGE 2 OUTPUT
200mV/ 50mS/ 8HHz
JITTER ≈ 11%

#12



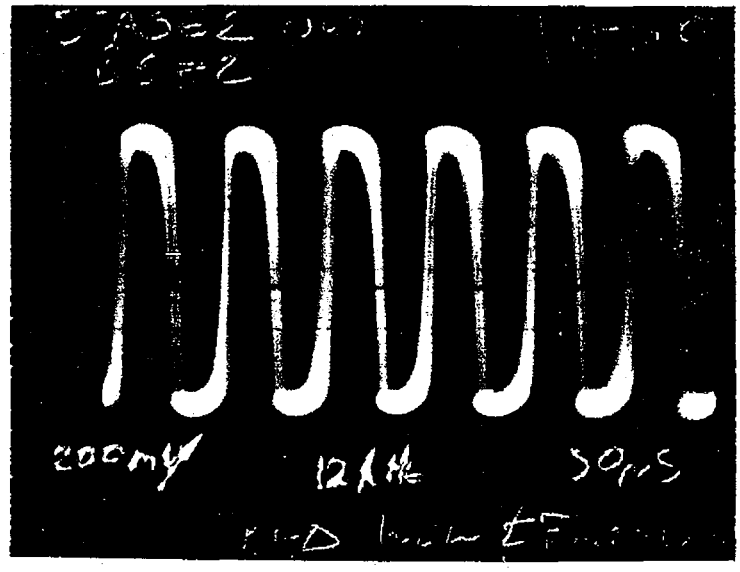
BB#2 READ BACK SIGNAL
STAGE 2 OUTPUT
200mV/ 50mS/ 8HHz
JITTER ≈ 9%

#13



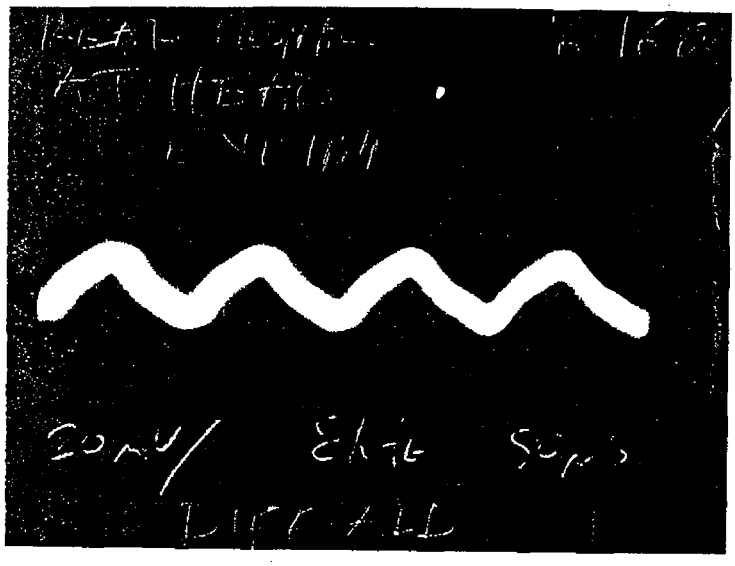
EXATRON READBACK SIGNAL
STAGE 2 OUTPUT
200mV/ 50μS/ 12kHz
JITTER ≈ 10%

#14



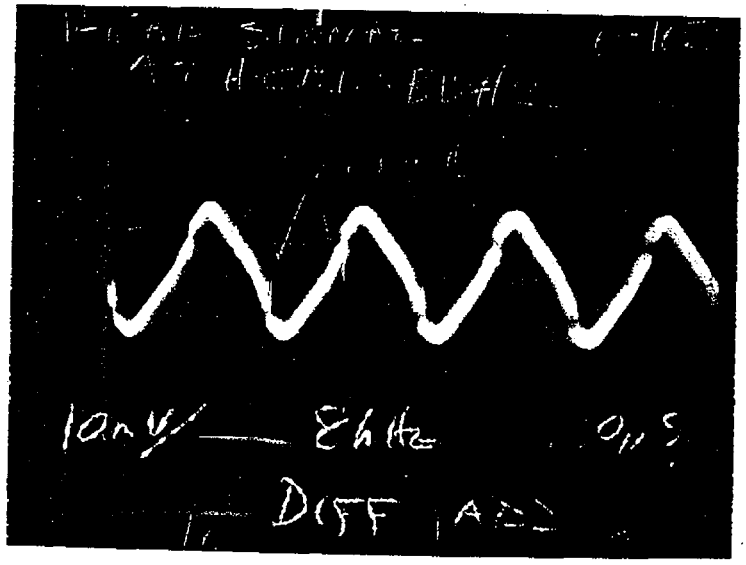
BB#2 READBACK SIGNAL
STAGE 2 OUTPUT
200mV/ 50μS/ 12kHz
JITTER = BAD

#15



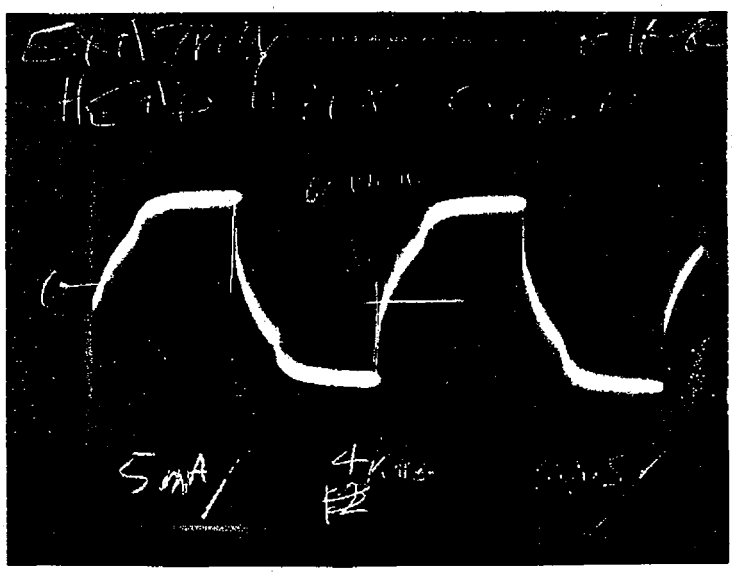
EXATRON READ BACK VOLTAGE AT HEAD 1X PROBES
20mV/ 50μS/ 8kHz
TWO PROBES, DIFFERENTIAL MODE
PLAYBACK OF TAPE RECORDED ON THIS

#16

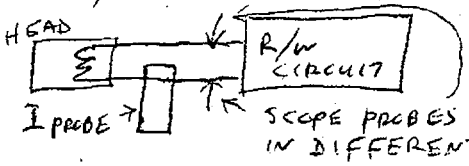


BB#2 READBACK VOLTAGE AT HEAD 1X PROBES
10mV/ 50μS/ 8kHz
PLAYBACK OF TAPE RECORDED ON THIS UNIT

#17



EXATRON HEAD WRITE CURRENT
5mA/DIV — 50nS/DIV AT 4kHz



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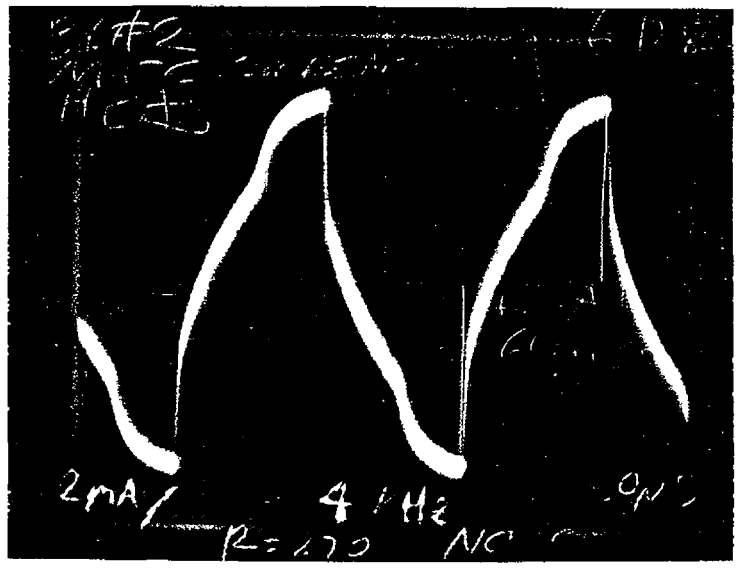
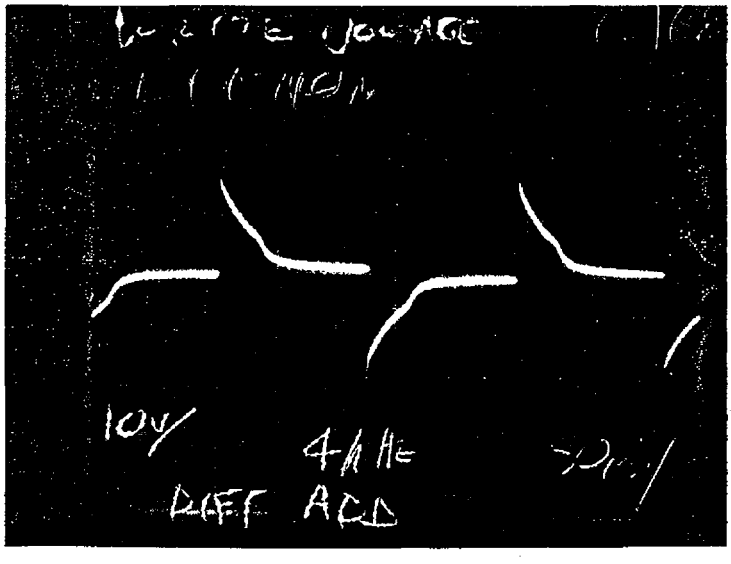


BB#2 HEAD WRITE CURRENT
2mA/ 50nS/ 4kHz

DRIVE RESISTOR = 270Ω
NO CAPACITOR

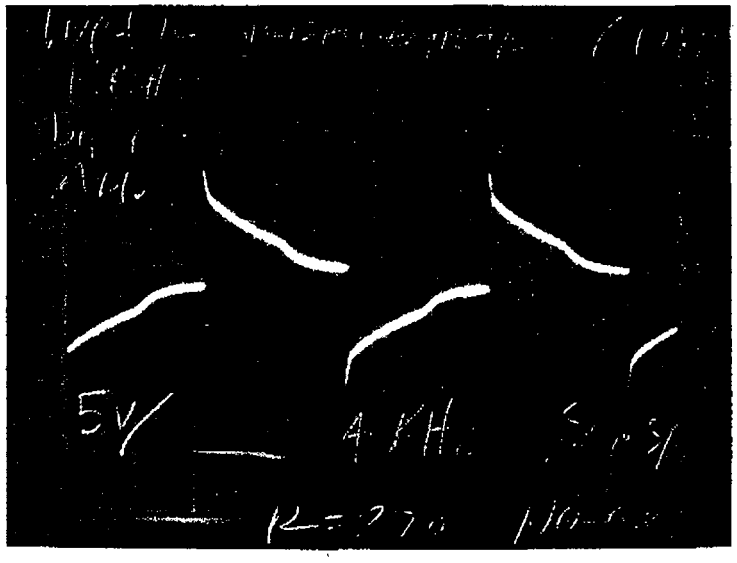
#19



EXATRON WRITE VOLTAGE
ACROSS HEAD
10V/ 50nS/ 4kHz

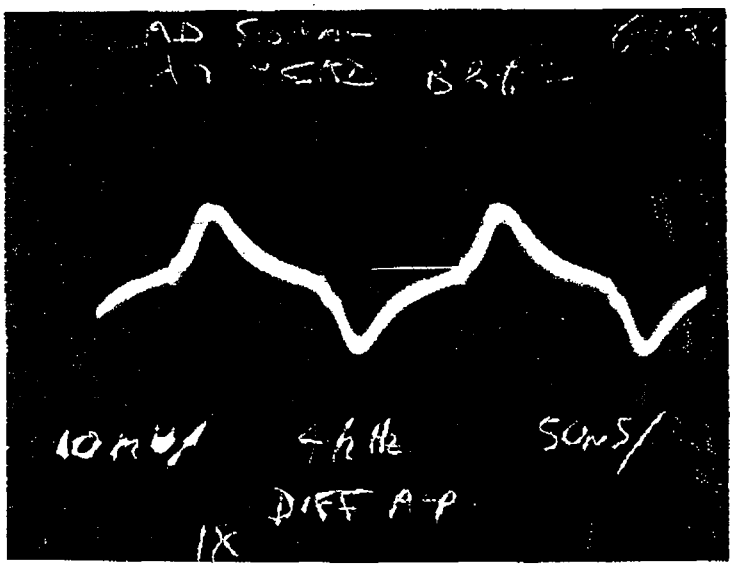
TWO TYPE TEK P6053B PROBES
SCOPE IN DIFFERENTIAL MODE

#20



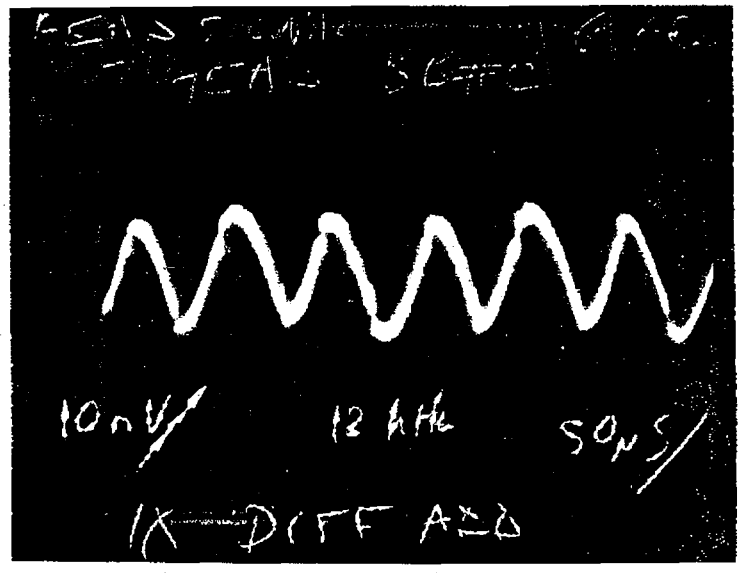
BB#2 HEAD WRITE VOLTAGE
5V/ 50nS/ 4kHz

#21



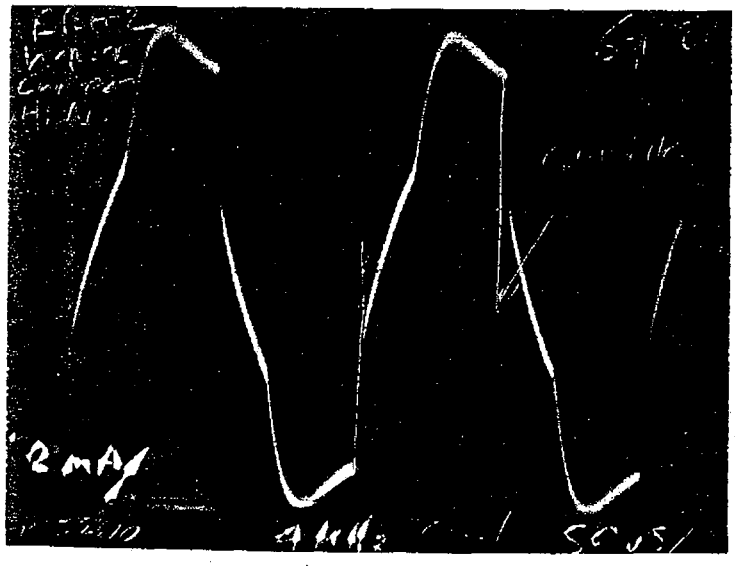
BB #2 READBACK VOLTAGE AT HEAD 1X PROBES
10mV/ 50nS/ 4kHz

#22



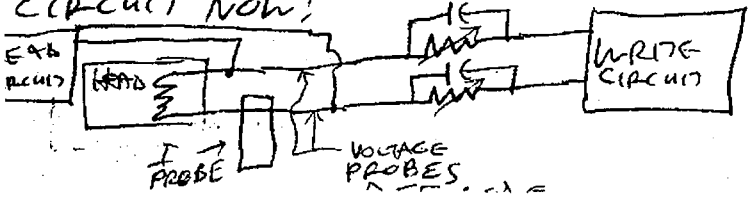
BB #2 READBACK VOLTAGE AT HEAD 1X PROBES
10mV/ 50nS/ 12kHz

#23



BB #2 HEAD WRITE CURRENT
2mA/ 50nS 4kHz R=270
C=.1nf

CIRCUIT NOW:



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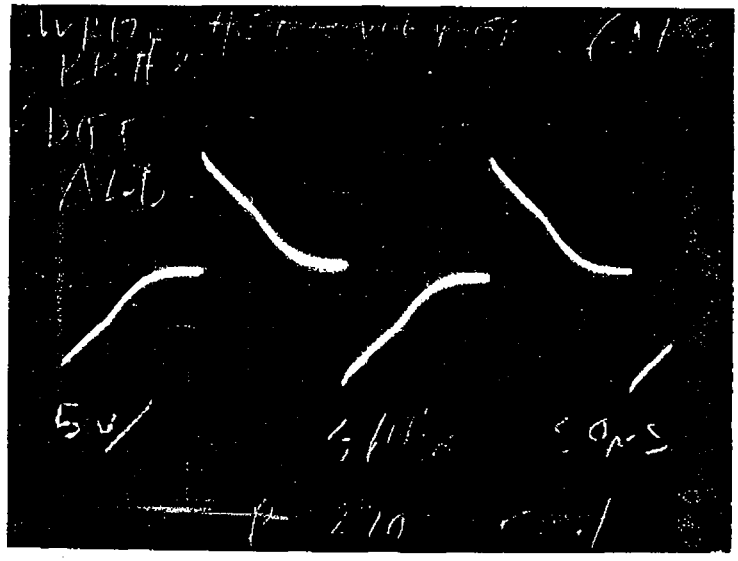
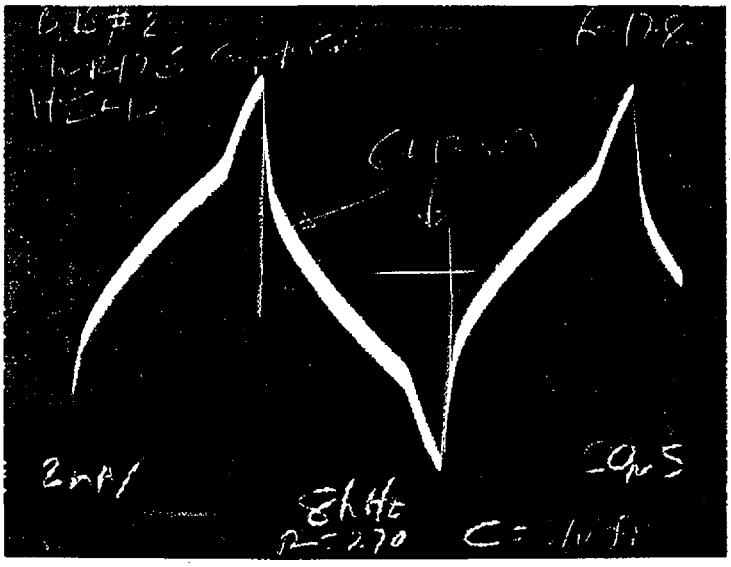


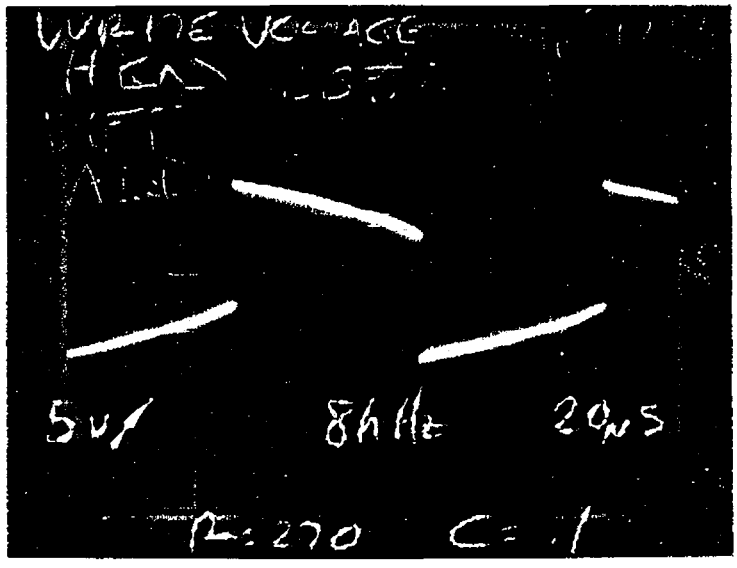
BB #2 HEAD WRITE VOLTAGE
5V/ 50nS 4kHz
R=270 C=.1nf

#25



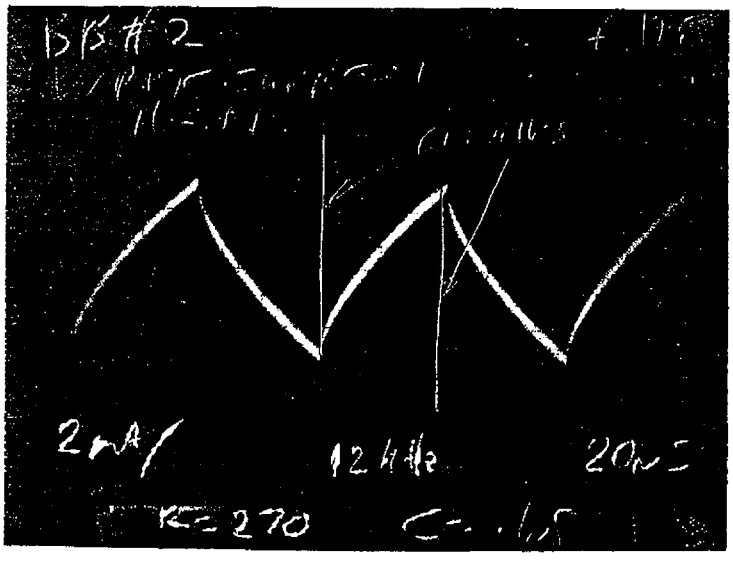
BB #2 HEAD WRITE CURRENT
2mA / 20μS / 8kHz
R=270 C=.1μF

#26



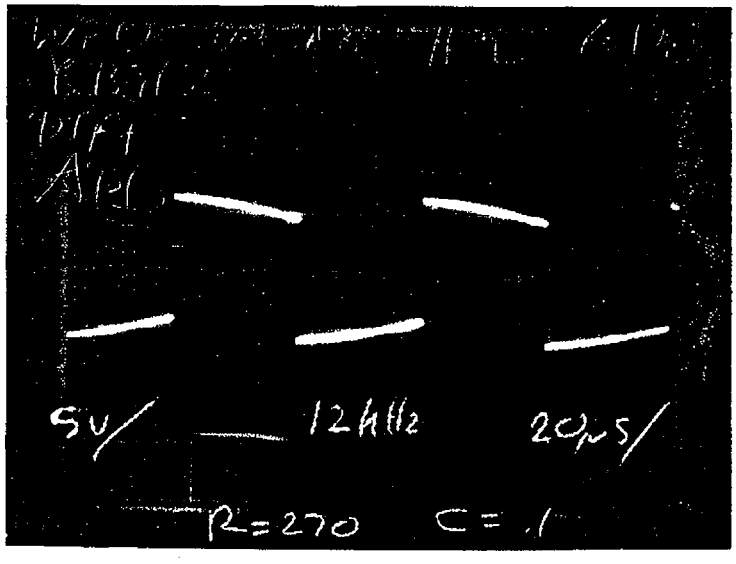
BB #2 HEAD WRITE VOLTAGE
5V/ 20μS/ 8kHz
R=270 C=.1μF

#27



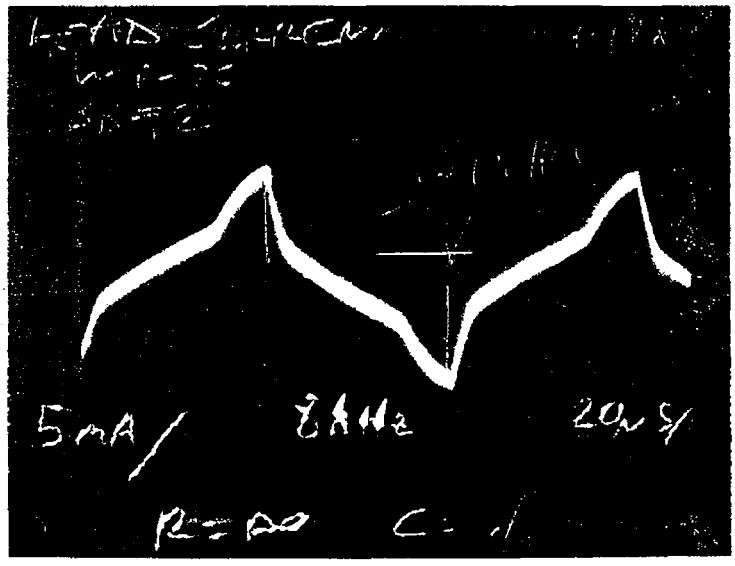
BB #2 HEAD WRITE CURRENT
2mA/ 20μS/ 12kHz
R=270 C=.1μF

#28



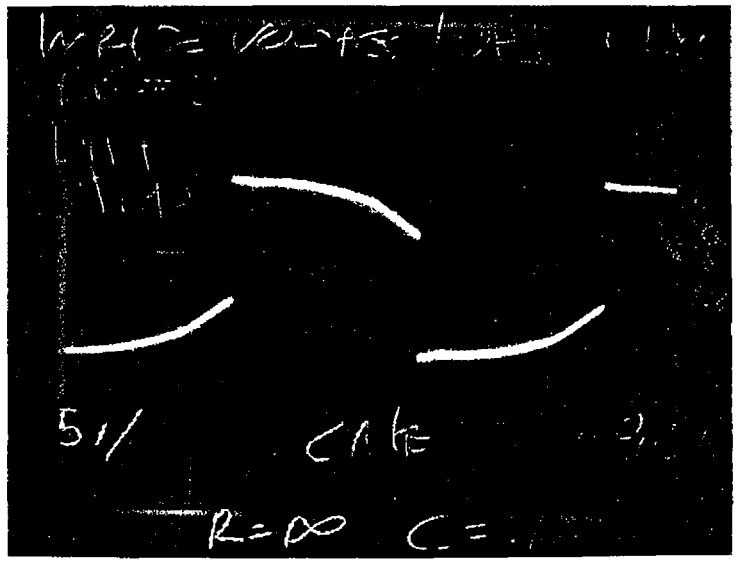
BB #2 HEAD WRITE VOLTAGE
5V/ 20μS/ 12kHz
R=270 C=.1μF

#29



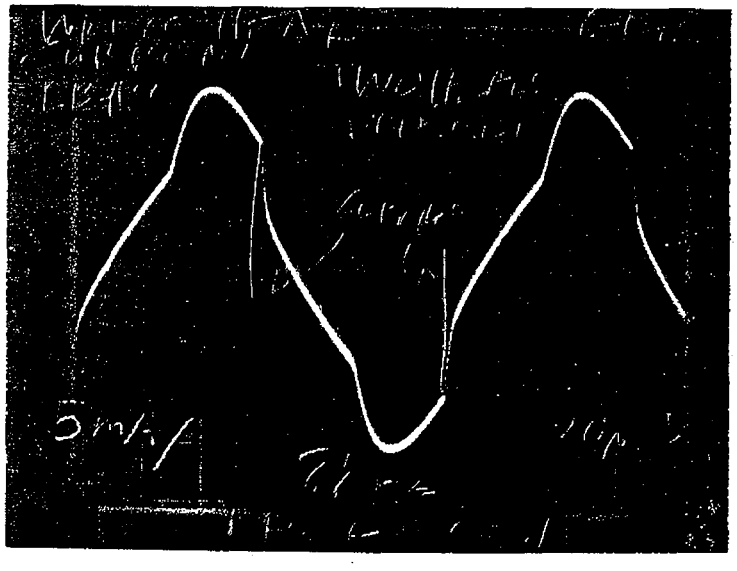
BB #2 HEAD WRITE CURRENT
5 mA/ 20NS/ 8MHz
R=∞ C=.1NF

#30



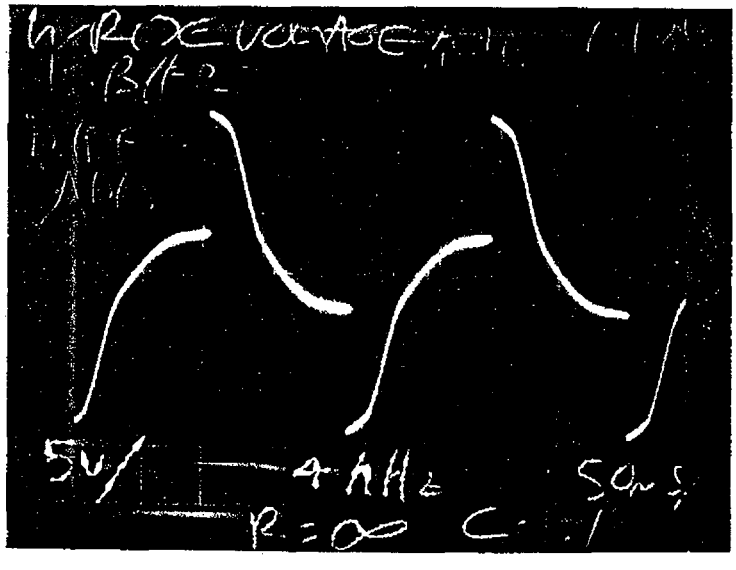
BB #2 HEAD WRITE VOLTAGE
5V/ 20NS/ 8MHz
R=∞ C=.1NF

#31



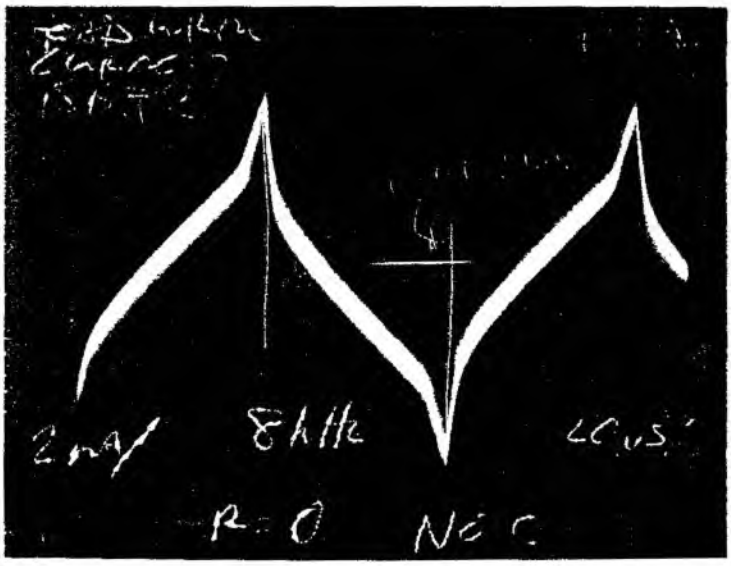
BB#2 WRITE CURRENT FOR
TWO HEADS IN PARALLEL
5MA/ 20NS 8MHz
R=∞ C=.1NF

#32



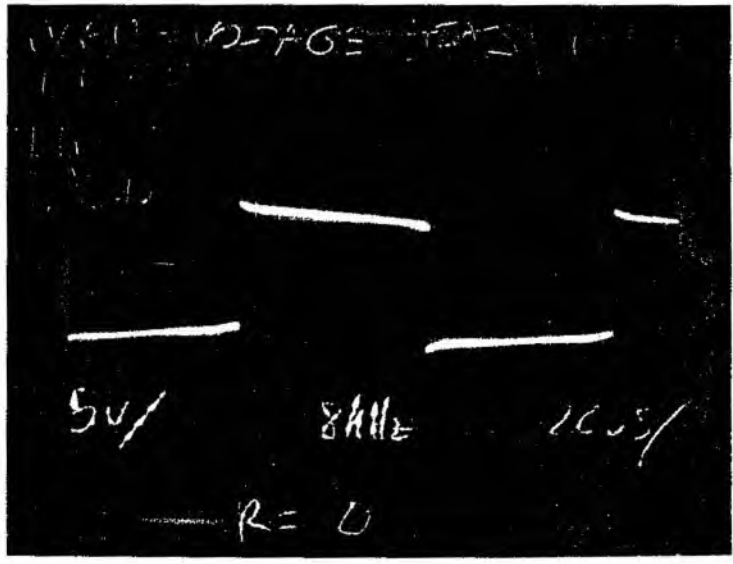
BB #2 HEAD WRITE VOLTAGE
5V/ 50NS/ 4MHz
R=∞ C=.1NF

#33



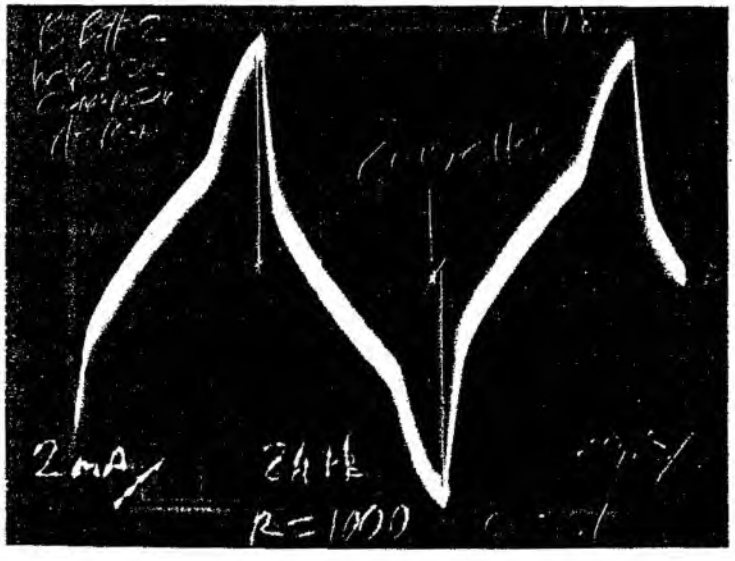
BB #2 HEAD WRITE CURRENT
2mA/ 20uS/ 8kHz
R=0

#34



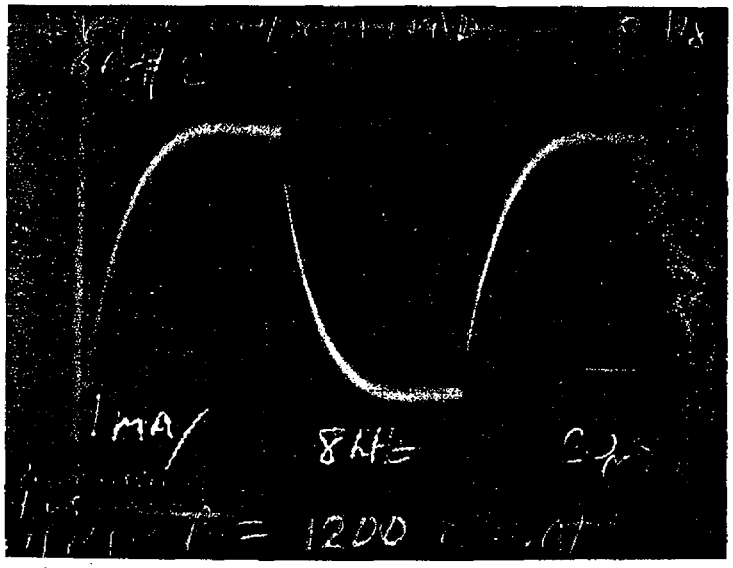
BB #2 HEAD WRITE VOLTAGE
5V/ 20uS/ 8kHz
R=0

#35



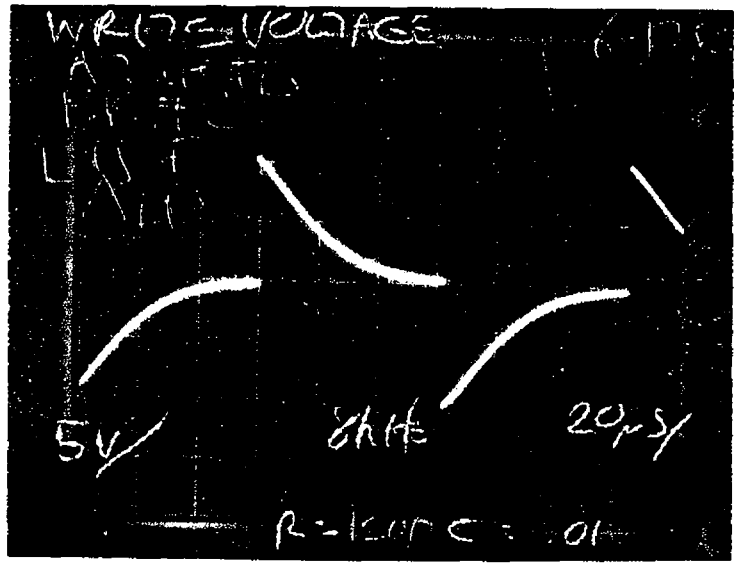
BB #2 HEAD WRITE CURRENT
2mA/ 20uS/ 8kHz
R=1000 C=.1uF

#36



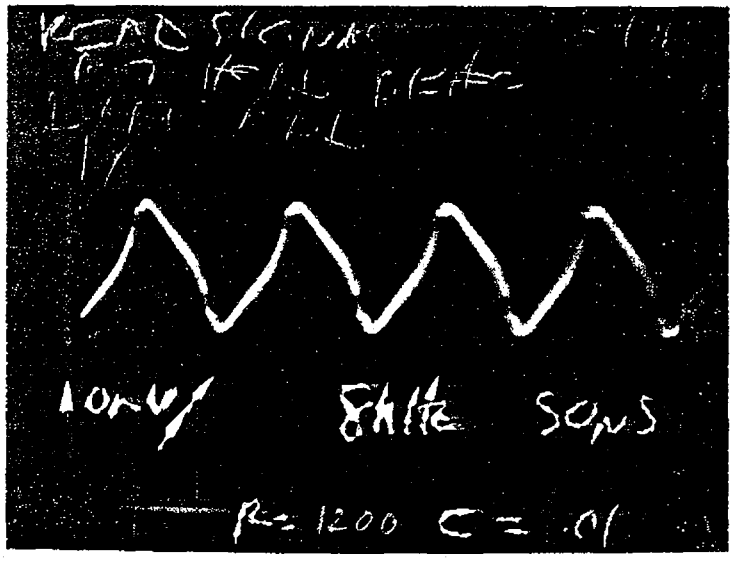
BB#2 HEAD WRITE CURRENT
1mA / 20μS / 8kHz
C = .01μF R SET FOR
BEST WAVEFORM, R = 1200

#37



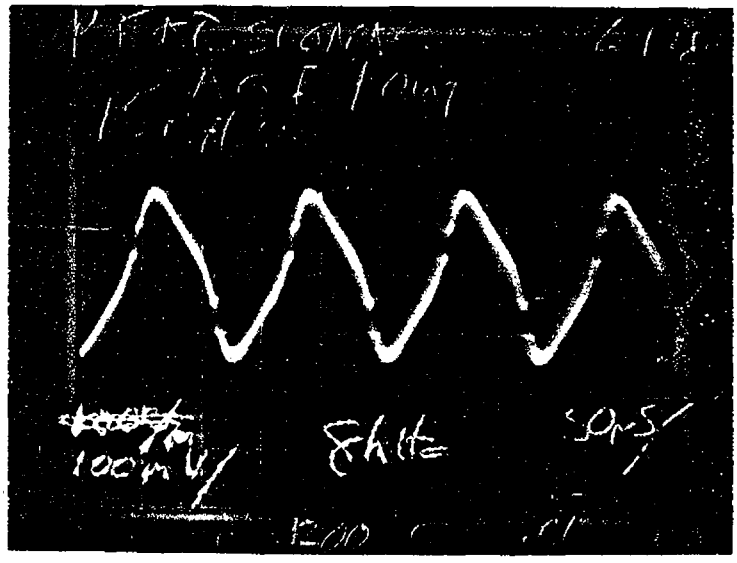
BB#2 HEAD WRITE VOLTAGE
5V/ 20μS/ 8kHz
R = 1200 C = .01μF

#38



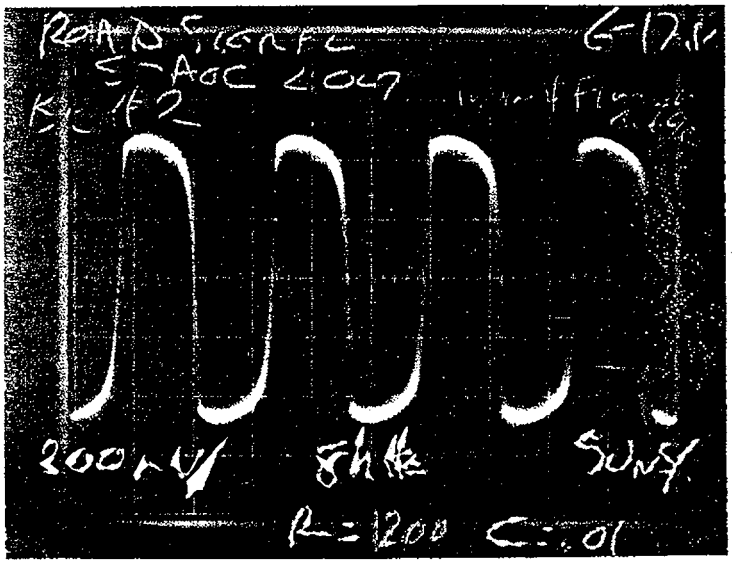
BB #2 READBACK VOLTAGE AT HEAD
10mV/ 50μS/ 8kHz
1X PROBES DIFFERENTIAL MODE
TAPE WRITTEN USING R = 1200
C = .01μF

#39



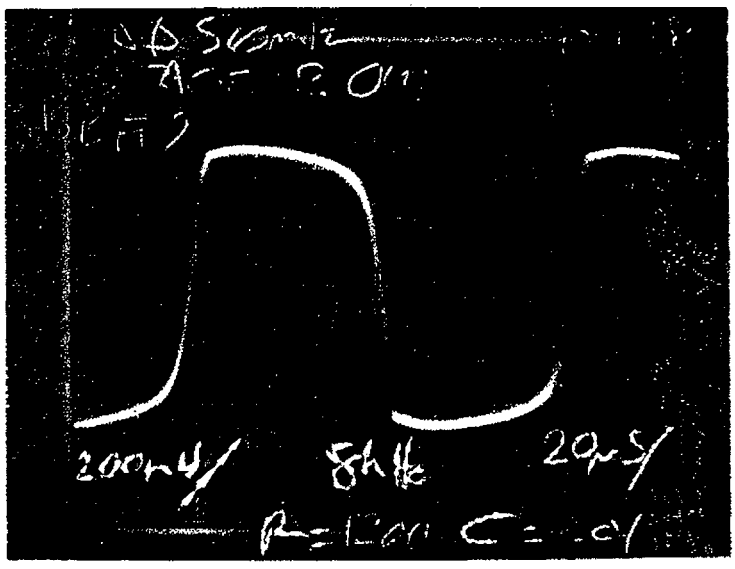
BB#2 READBACK VOLTAGE
STAGE ONE OUTPUT
100mV/ 50μS 8kHz

#40



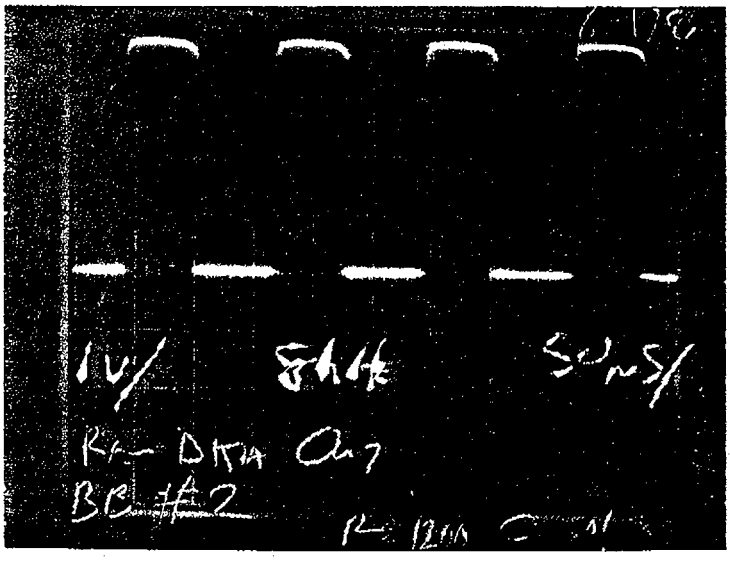
BB#2 READBACK SIGNAL
AT STAGE 2 OUTPUT
200mV/ 50nS/ 8kHz

#41



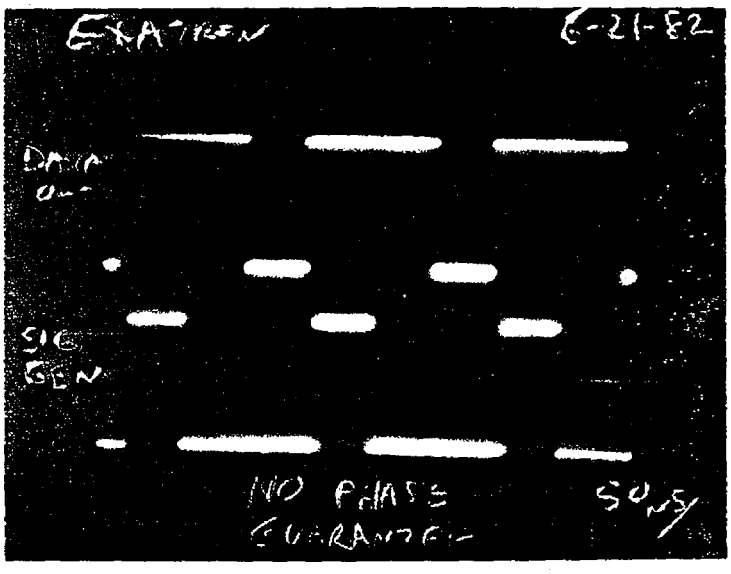
BB#2 READBACK SIGNAL
AT STAGE 2 OUTPUT
200mV/ 20nS/ 8kHz

#42



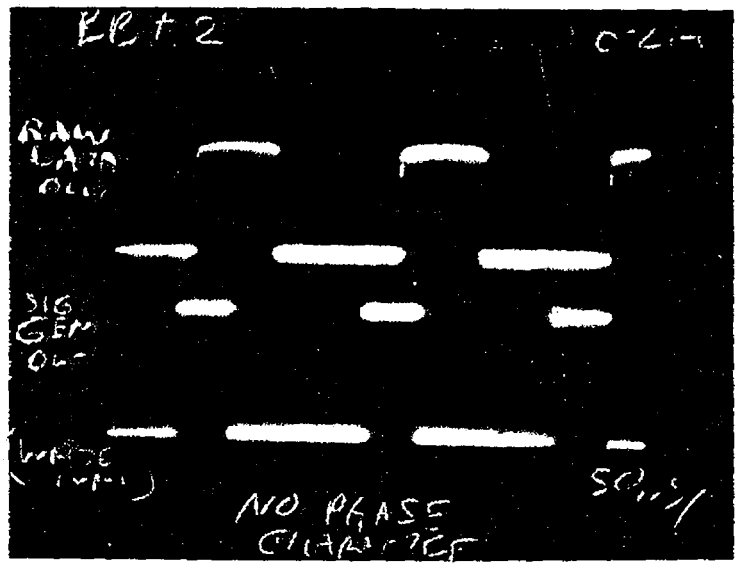
BB#2 READBACK SIGNAL
RAW DATA OUTPUT
1V/ 50nS/ 8kHz

#43



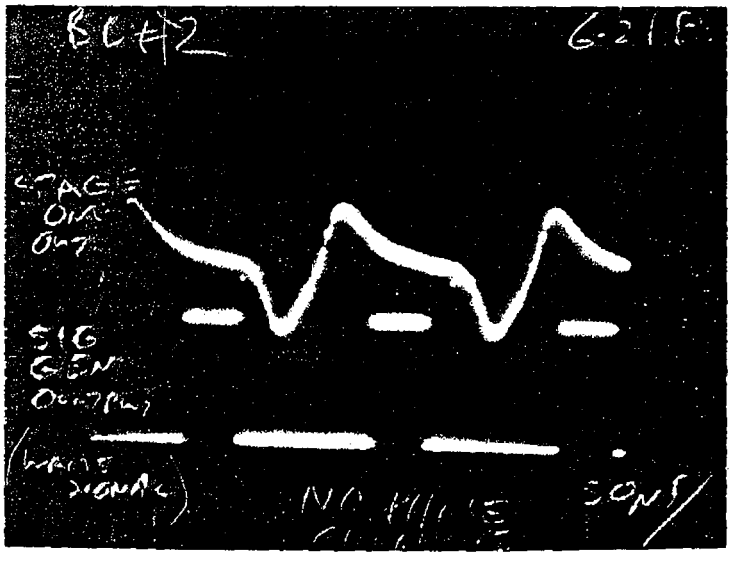
EXATRON - DATA OUT DUTY CYCLE COMPARED TO WRITE DUTY CYCLE FOR NON-SYMMETRICAL WAVEFORM
DATA OUT UPPER TRACE
NOTE: PHASE INVERSION
1/4 ALSO NO PHASE SYNC BETWEEN SIGNALS DUE TO SCOPE SETUP

#44

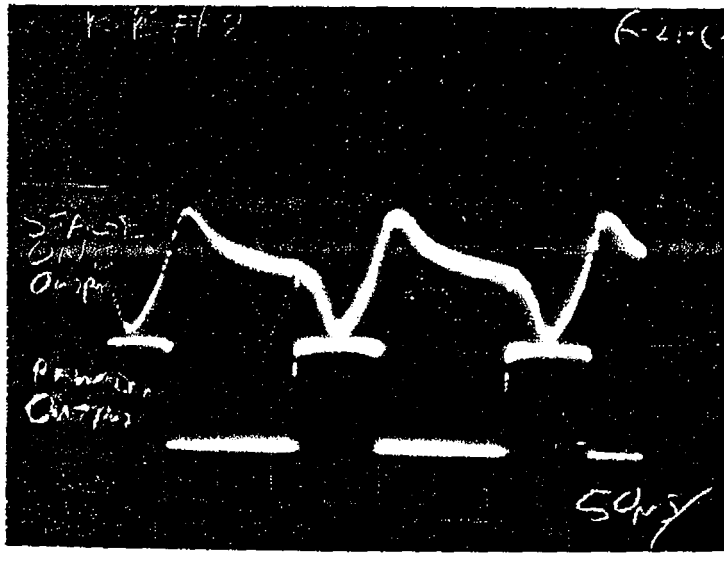


BB#2 DATA OUTPUT DUTY CYCLE COMPARED TO WRITE DUTY CYCLE
DATA OUT UPPER TRACE
NOTE: PHASE INVERTED FROM EXATRON - ALSO NO PHASE SYNC BETWEEN SIGNALS DUE TO SCOPE SETUP

#47



BB#2 STAGE 1 OUTPUT COMPARED TO WRITE SIGNAL NOTE: SIGNALS NOT PHASE SYNCED DUE TO NATURE OF SETUP



BB#2 STAGE 1 OUTPUT COMPARED TO RAW DATA OUTPUT - SIGNALS ARE SYNCED IN THIS CASE
NOTE: PROBLEM CURED BY CHANGING COUPLING CAP TO .0022uF

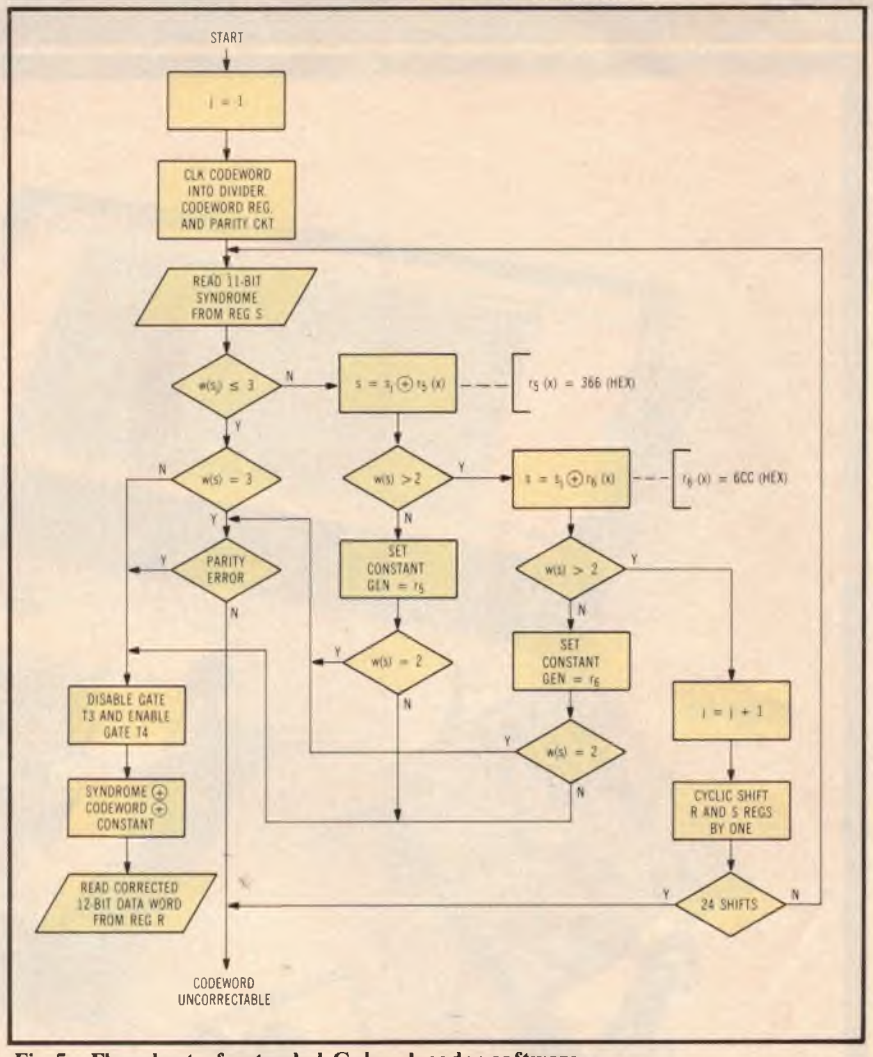


Fig 5 Flowchart of extended Golay decoder software

software. In the communication interface application both encoder and decoder operate in real time at a line data rate of 32k bps.

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1. M. Golay, "Binary Coding," *IRE Trans*, PGIT-4, 1954, pp 23-28
2. H. Shapiro and D. Slotnick, "On the Mathematical Theory of Error-Correcting Codes," *IBM Journal*, Jan 1959, pp 25-34
3. T. Kasami, "A Decoding Procedure for Multiple Error Correcting Cyclic Codes," *IEEE Transactions on Information Theory*, IT-10, Apr 1964, pp 134-139
4. W. Peterson and E. Weldon, Jr, *Error-Correcting Codes*, 2nd edition, MIT Press, 1972
5. A. Tietavainen, "On the Nonexistence of Perfect Codes Over Finite Fields," *Siam Journal of Applied Math*, vol 24, Jan 1973, pp 88-96

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M. Golay, "Notes on Digital Coding," *Proceedings IRE Correspondence*, p 657

R. W. Hamming, "Error Detecting and Error Correcting Codes," *Bell System Technical Journal*, 29, 147, 1950

M. Liccaido, "Polynomial Error Detecting Codes and Their Implementation," *Computer Design*, Sept 1971, pp 53-59

W. Peterson and D. Brown, "Cyclic Codes for Error Detection," *Proceedings of the IRE*, Jan 1961, pp 228-235

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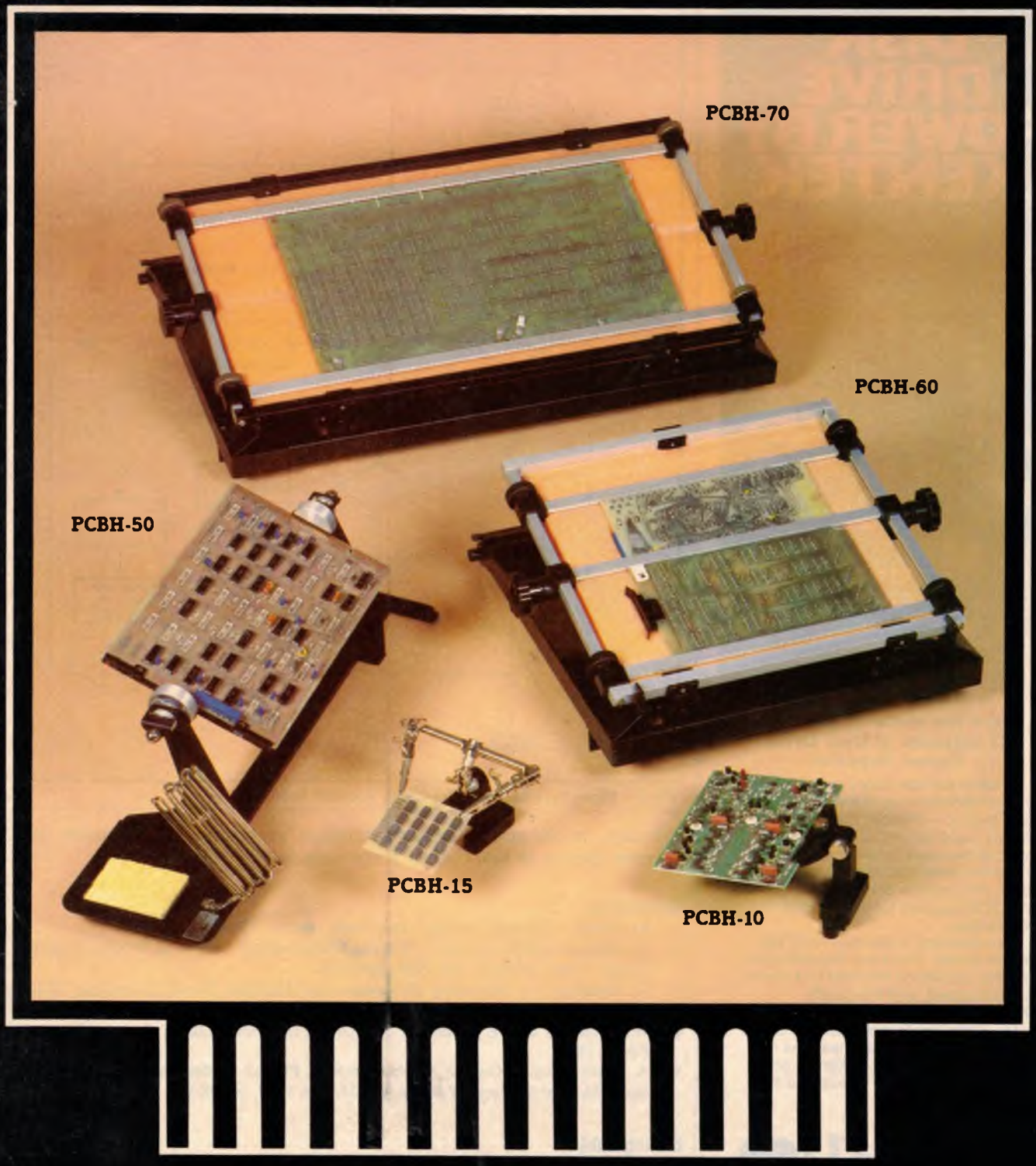
High 704 *Average 705* *Low 706*



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CIRCLE 69

FORWARD-LOOKING ERROR CORRECTION VIA EXTENDED GOLAY

The addition of an overall parity bit to the standard Golay code extends detection to four single-bit errors

by Lawrence J. Rennie

Theory and design of a forward error correcting scheme, using the extended Golay (24,12) code, was incorporated into a developmental data adapter unit for use in a data communication system. This scheme was selected because the Golay (23,12) code is the only perfect binary code known to have the ability to detect and correct up to three randomly spaced errors in the received codeword. Extending the codeword from 23 to 24 bits by adding an overall parity check bit expands the error detection capability to four errors. Perfect binary codes are scarce. In fact, the single error correcting Hamming codes and the triple error correcting Golay code are the only known nontrivial perfect binary codes.

The Golay (23,12) code is a member of a unique family of binary codes, called perfect or lossless codes. To illustrate that a perfect binary code is unique, consider the following: let S_n represent the set in n space consisting of all binary sequences of length n. Clearly the total number of points in S_n equals 2^n. Now let C_n be a subset of S_n consisting of all points in S_n that have a mutual distance of $d \geq 2e + 1$ from each other and let A_n be the number of points in such a subset. Distance d between two binary sequences is equal to the number of positions in which the two sequences disagree. For example, sequences 1011010 and 0010111 differ in four positions and therefore have a distance $d = 4$ from each other. C_n represents a codepoint set for a code that can correct e or fewer errors. Consider a codepoint x in C_n and let T_x represent all the points in S_n that are within a distance $d \leq e$ from x. This set of points can be visualized as a sphere in n space with x at its center. Likewise, let T_y represent the n space sphere of all points a distance $d \leq e$ from another codepoint y. If $x \neq y$, then T_x and T_y are disjoint because, if they are not disjoint, there exists a point z common to both T_x and T_y. If this is the case, x and y have a distance $\leq 2e$, which is a contradiction to the definition of codepoint set C_n. The number of points in the T_x or T_y sphere is

$$1 + \binom{n}{1} + \cdots \binom{n}{e} = \sum_{m=o}^{e} \frac{n!}{(n-m)!m!}$$

Since the number of codepoints equals the number of spheres, the total number of code points, A_n, in S_n is bounded by the number of points in S_n divided by the number of points in the sphere; eg,

$$A_n \leq \frac{2^n}{\sum_{m=o}^{e} \frac{n!}{(n-m)!m!}} \qquad (1)$$

Any code for which Eq (1) is an equality is maximally efficient and is referred to as a perfect, lossless, or close

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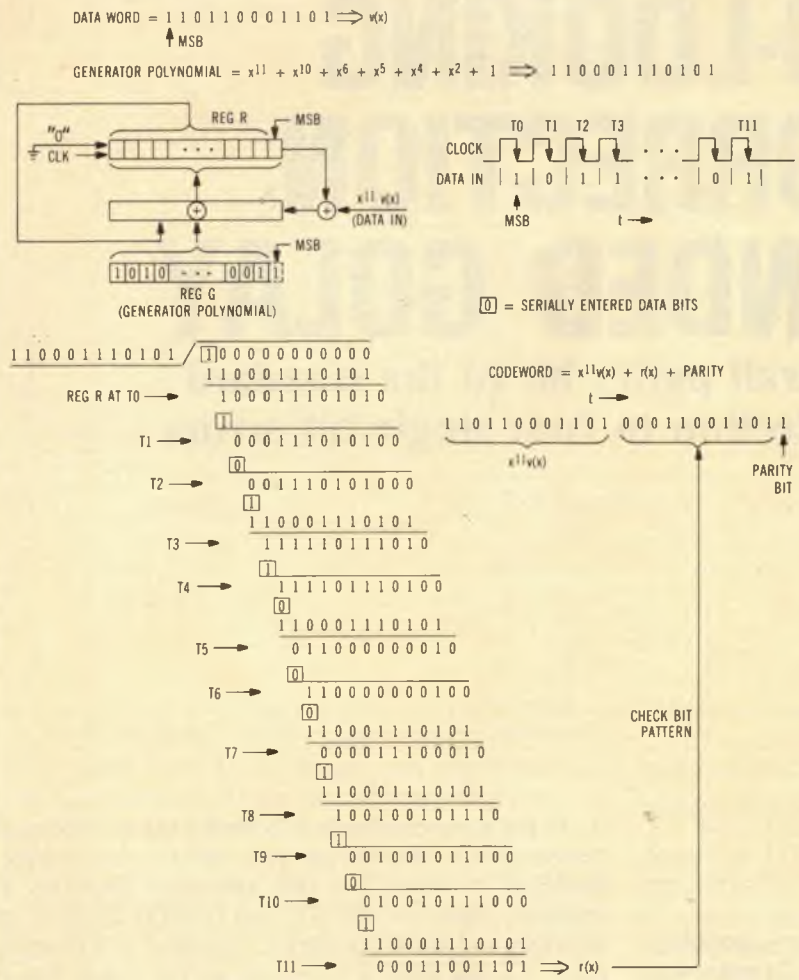


Encoder example

The encoding algorithm is exemplified in Fig A. Operation of the serial divider circuit used to generate the 11-bit check bit pattern is clearly illustrated. The remainder register R is initially cleared to all zeros and the generator polynomial register G holds the 12-bit generator polynomial for the Golay code.

Generator polynomial register G and the XOR operation are implemented by XOR gates placed between the flipflops of the remainder register R. Note from the example that it is not necessary to implement the MSB position of g(x) physically because, when g(x) is added modulo 2 to the partial remainder, the MSB of g(x) always contributes logic 0 to the new partial remainder.

Twelve clock pulses are required to complete the division with the check bit pattern appearing in the remainder register R after the twelfth clock pulse. As shown in Fig 3, the 11-bit check bit pattern is appended to the 12-bit data bit word, along with an overall parity bit on the 23-bit Golay codeword to form the 24-bit extended Golay codeword.

packed code, since the spheres formed by the codepoints completely exhaust S_n. For e = 1 in Eq (1)

$$A_n \Big|_{e=1} \leq \frac{2^n}{n+1} \qquad (2)$$

The only perfect binary codes that satisfy the equality in Eq (2) are the Hamming codes. For A_n to be an integer, n must be of the form $2^r - 1$ where r is an integer. For e = 2, Golay[1] and Shapiro and Slotnick[2] show that no perfect code exists. For e = 3 Golay noted that

$$1 + \binom{23}{1} + \binom{23}{2} + \binom{23}{3} = 2^{11} = 2048$$

which suggested a perfect n = 23 bit code containing $A_n = 2^{23}/2^{11} = 2^{12} = 4096$ codewords and correcting any three or fewer errors.

This led Golay to discover the perfect Golay (23,12) code. Shapiro and Slotnick proved there are no others for e = 3. The question of the existence of other perfect binary codes for any value of e was finally answered by Tietavainen.[5] He proved that, other than the trivial perfect code cases and the Golay code, there are no others.

The extended Golay (24,12) code is comprised of the Golay (23,12) code with an overall parity bit appended to the 23-bit Golay codeword to form the 24-bit extended Golay codeword. The Golay (23,12) code permits detection and correction of up to three errors occurring anywhere within the codeword: adding the extra overall parity bit permits the decoder to detect, but not correct, four errors. (See Fig 1.)

Cyclic codes

The Golay (23,12) code is a member of the family of codes called cyclic codes. Cyclic codes are linear codes

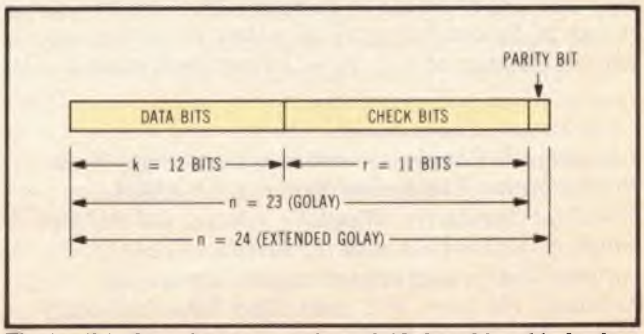
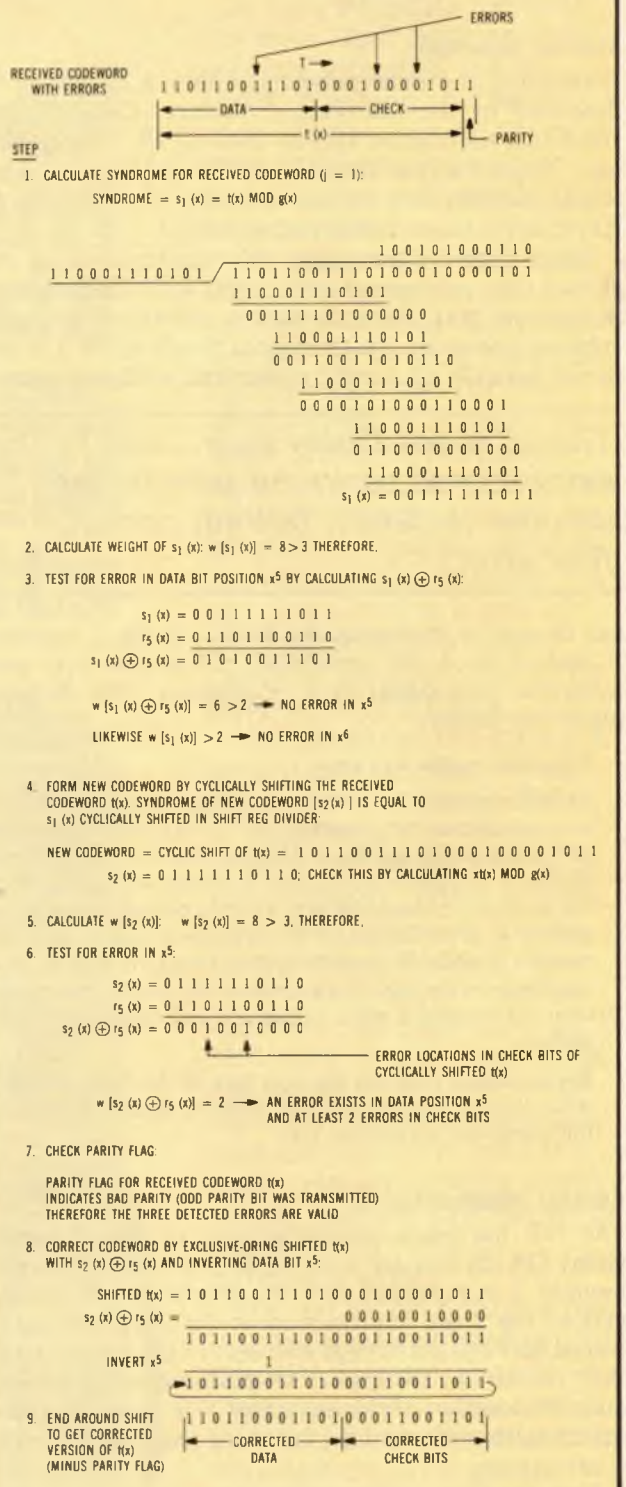


Fig 1 (24,12) codeword consists of 12 data bits, 11 check bits, and one parity bit.

Decoder example

The decoding algorithm is illustrated in Fig B. The codeword used in the example is the codeword derived in the encoding algorithm example of Fig A. Fig B shows that three errors have been inserted into the codeword; one error in the data bits; two errors in the check bits. The first operation performed is the calculation of the received codeword syndrome [$s_j(x)$, j = 1]. The computer then reads the syndrome and calculates its weight. In the example w [$s_1(x)$] = 8. Since w [$s_1(x)$] ≥ 3 (see Fig 5), tests are made for an error in bit position 5 or 6 of the data word. Both tests fail. Therefore, a new codeword, equal to a cyclic shift of the original received codeword, is formed and the tests are repeated. As stated earlier and as shown in Fig B, the syndrome of the cyclically shifted codeword is equal to the syndrome $s_1(x)$ cyclically shifted in the divider, ie, $s_2(x) = xs_1(x) \bmod g(x)$. As can be seen from the example, the weight of $s_2(x)$ is greater than three so the syndrome is tested for an error in bit position 5 of the new codeword. In the example, the test for this error is positive, ie, w [$s_2(x) \oplus r_5(x)$] = 2. Thus, in the example, there are at least two errors in the check bit positions—at the locations of the logic 1 values in $s_2(x) \oplus r_5(x)$ and an error in the fifth data bit position. The parity flag is then checked to see if four errors have occurred. In the example the parity flag indicates a parity error. Thus, the three errors found are valid and the received corrupted codeword can be corrected. The corrected codeword has to be rotated to place the original data bits in the correct data bit positions.



with the additional property that a cyclic shift of a codeword produces another codeword in the set. In the algebra of polynomials a cyclic code of length n can be represented as a polynomial of degree (n − 1) where the coefficients of the polynomial are the bits in the codeword, for example

$$1010110 \Leftrightarrow f(x) = 1x^6 + 0x^5 + 1x^4 + 0x^3 + 1x^2 + 1x + 0x^0$$
$$= x^6 + x^4 + x^2 + x$$

Since a cyclic shift of a codeword is equivalent to multiplication by x mod $(x^n - 1)$ then, if f(x) is a codeword, so are all multiples of f(x) modulo $(x^n - 1)$.

For (n,k) cyclic codes (where n equals the total number of bits in the codeword and k equals the number of data bits in the codeword), there exists a polynomial, called the generator polynomial g(x). Every codeword in the set can be expressed as a multiple of g(x). To fulfill this property it can be shown that g(x) must be a divisor of $x^n - 1$ and have degree (n − k). For the Golay (23,12) code such a generator polynomial is

$$g(x) = x^{11} + x^{10} + x^6 + x^5 + x^4 + x^2 + 1 \quad (3)$$

In terms of matrices, g(x) can be used to form a set of k vectors that are linearly independent and span the codeword space, ie, a set of basis vectors for the codeword space.

Since each codeword in the set is a multiple of g(x), the codeword t '(x) associated with a data word v(x) can be described as follows

$$\frac{x^{(n-k)}v(x)}{g(x)} = q(x) + \frac{r(x)}{g(x)}$$

and

$$t'(x) = x^{(n-k)}v(x) + r(x)$$

where r(x) = the remainder polynomial. Note that subtraction modulo 2 is equivalent to addition modulo 2.

The extended codeword t(x) is the codeword t′(x) with an overall parity bit appended.

Encoder algorithm

Formatting the data polynomial into a codeword is described by the following procedure. Calculate the remainder polynomial r(x) by dividing $x^{(n-k)}\,v(x)$ with g(x). Append r(x) to v(x) to form the codeword. Calculate an overall parity bit and append it to $x^{(n-k)}\,v(x)$ + r(x) to form the extended codeword t(x).

Calculating the remainder r(x) requires dividing the shifted data polynomial $x^{(n-k)}\,v(x)$ with the generator polynomial g(x). Since division is actually a shift and subtract operation, the functional circuit in Fig 2, comprised basically of a shift register and modulo 2 adder,

The extended Golay code...adding the extra overall parity bit permits the decoder to detect, but not correct, four errors.

can be used to implement the divisor. In Fig 2, registers R and G hold the remainder polynomial r(x) and generator polynomial g(x), respectively. The division algorithm follows

- Initialize register R to zero.
- Serially exclusive-OR (XOR) the shifted data polynomial, most significant bit (MSB) first, $x^{(n-k)}\,v(x)$ with the output of the remainder register R. Use the output of the XOR gate to enable or disable the modulo 2 subtraction (addition) of the generator polynomial g(x) with the partial remainder in register R. If the output of the XOR gate is logic 1, then the modulo 2 adder is enabled and $r(x) \oplus g(x)$ is entered into register R on the next clock cycle. If the output is a logic 0 then the modulo 2 adder is disabled and register R is right shifted.
- Repeat step 2 until the last v(x) data bit has been entered. After the last data bit has been entered, register R contains the remainder polynomial r(x).

Encoder implementation

The full hardware implementation of the extended Golay (24,12) encoder is shown in Fig 3. Note that the modulo 2 summations and the generator polynomial g(x) of Fig 2 are implemented in Fig 3 by XOR gates placed between the storage elements of the synchronous shift register R. The logic 1 bit positions of g(x) determine the location of the individual XOR gates. To form the complete codeword the following sequence of events is performed.

First, the 12-bit data polynomial v(x) is simultaneously clocked, MSB first, into the codeword output multiplexer (MUX) and into the shift register divider and parity generator. Data are routed to the encoder output by MUX 1.

After the twelfth clock pulse, register R will contain the remainder polynomial r(x). Control signal T1 then switches MUX 1 to the divider output and disables the divider feedback gate. The next 11 clock pulses clock out the remainder polynomial r(x) from register R and clock zeros into register R in preparation for the next 12 data bits.

After the last remainder bit is clocked out of the divider, MUX 2 switches the parity generator bit to the output line to complete the 24-bit codeword. These steps are repeated to encode the next 12 data bits.

Decoder algorithm

The error correcting scheme selected for the Golay decoder design is an error correcting scheme proposed by Kasami.[3] Kasami's method is a modification to the error trapping Meggit decoder discussed in Peterson's book.[4] Before considering the actual algorithm, the relationships among the following polynomials involved in the decoding scheme should be noted

Transmitted codeword polynomial (without parity bit)	$= t'(x)$
Received codeword polynomial (without parity bit)	$= t(x)$
Generator polynomial	$= g(x)$
Error pattern polynomial	$= e(x)$
Message portion of received polynomial	$= t_m(x)$
Check bit portion of received polynomial	$= t_p(x)$
Error bit pattern in the check bits	$= e_p(x)$
Error bit pattern in the message bits	$= e_m(x)$
Syndrome of received polynomial	$= s(x)$
Remainder polynomial generated by $e_m(x)$	$= r_m(x)$

now

$$\frac{t(x)}{g(x)} = q(x) + \frac{s(x)}{g(x)}$$

where

$$t(x) = t'(x) + e(x)$$

Substituting and noting that t′(x) is a multiple of g(x)

$$\frac{t(x)}{g(x)} = \frac{t'(x) + e(x)}{g(x)} = q_t(x) + \frac{e(x)}{g(x)} = q_t(x) + q_e(x) + \frac{s(x)}{g(x)}$$

Thus, syndrome s(x) is determined only by the error pattern polynomial e(x). Since

$$e(x) = x^{(n-k)}e_m(x) + e_p(x) \text{ then,}$$

$$\begin{aligned} s(x) &= e(x) \bmod g(x) \\ &= [x^{(n-k)}e_m(x) + e_p(x)] \bmod g(x) \\ &= e_p(x) + x^{(n-k)}e_m(x) \bmod g(x) \\ &= e_p(x) + r_m(x) \end{aligned} \qquad (4)$$

Eq (4) says if all the errors are confined to the check bit positions [ie, $r_m(x) = 0$], then s(x) will equal $e_p(x)$, since the degree of g(x) is greater than the maximum degree of $e_p(x)$.

Since a cyclic shift of a codeword produces another codeword in the set, if the codeword can be rotated so that all the errors fall within the check bit positions, the syndrome, s(x), of this codeword will also be the error pattern. However, if the errors are spaced so that it is impossible to rotate all the errors into the check bit positions at the same time, the decoding process becomes more complex. In this case, as expressed in Eq (4), the syndrome becomes s(x) = check bit position errors plus remainder due to message position errors.

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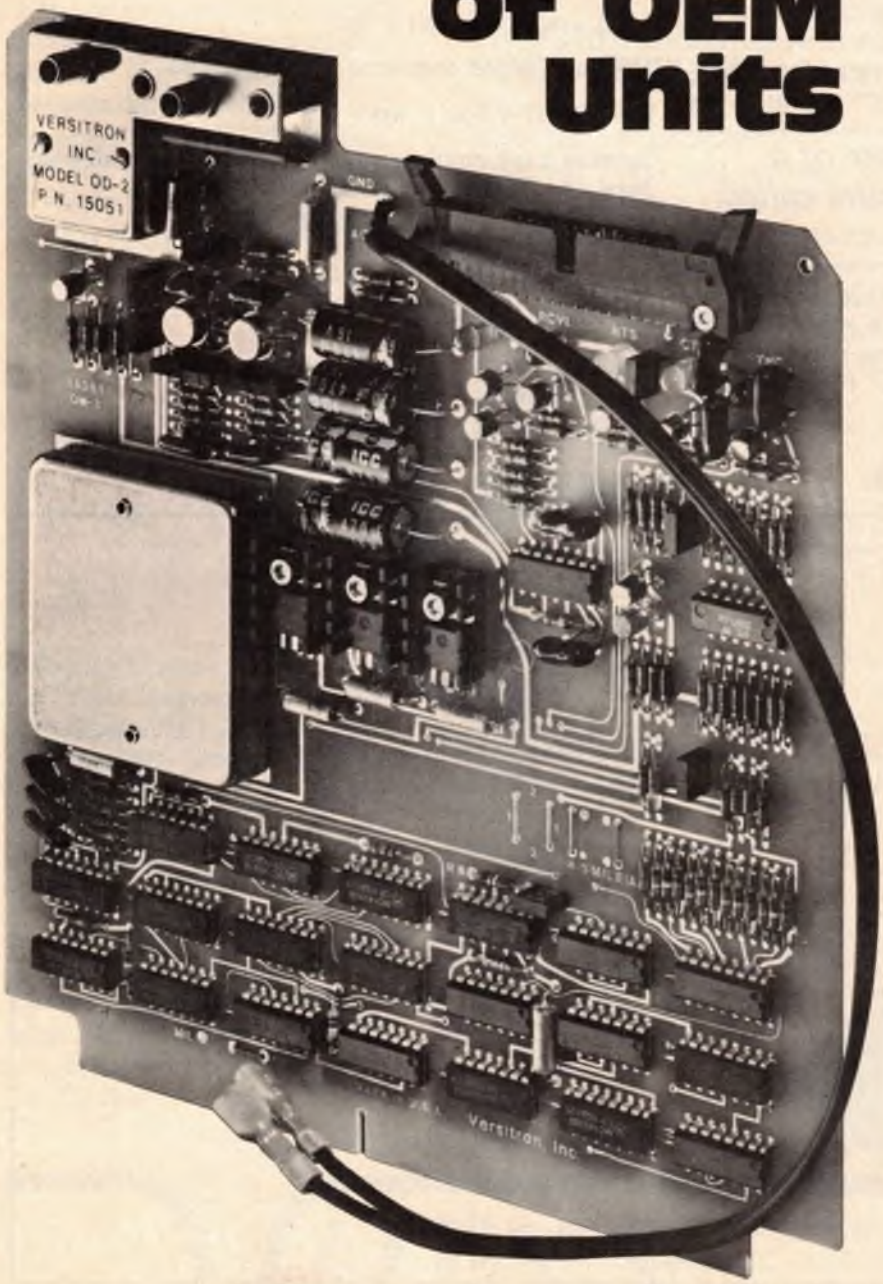

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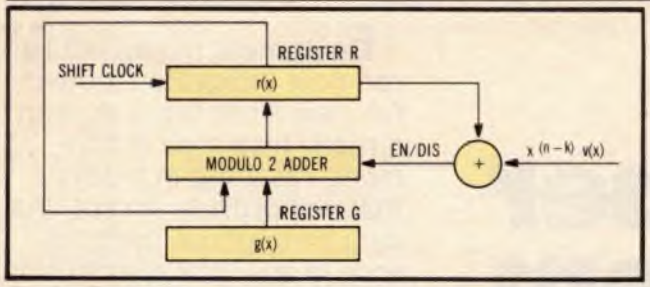

Fig 2 Shift register and modulo 2 adder. Combination, in effect, divides shifted data polynomial by generator polynomial.

In this case the complete error pattern is not obvious unless the message position error pattern $e_m(x)$ can be determined. When $e_m(x)$ can be determined, $r_m(x)$ can be calculated and the errors in the check bit positions, $e_p(x)$, can be determined from Eq (4) [eg, $e_p(x) = s(x) - r_m(x)$].

Kasami proves that a codeword constructed using the Golay (23,12) code, with an error pattern of weight 3 or less, can be cyclically shifted so that one of the following two conditions is met: all the errors appear in the

The Golay code is a member of a unique family of binary codes called perfect or lossless codes.

check bit positions; or two errors appear in the check bit positions and the third error appears in either the fifth or sixth bit of the message bit positions, denoted by x^5 or x^6, respectively. For $e_m(x) = x^5$ the remainder polynomial is

$$r_m(x) = r_5(x) = x^{(n-k)}e_m(x) \bmod g(x)$$
$$= x^{(23-12)}x^5 \bmod g(x) = x^{16} \bmod g(x)$$

Now substituting for g(x) from Eq (3) we get

$$r_5(x) = x^9 + x^8 + x^6 + x^5 + x^2 + x$$

Similarly for $e_m(x) = x^6$ we get

$$r_6(x) = x^{17} \bmod g(x) = x^{10} + x^9 + x^7 + x^6 + x^3 + x^2$$

Note the $r_6(x)$ is simply a cyclic shift of $r_5(x)$. In general, the syndrome of xt(x) is the syndrome of t(x) cyclically shifted once to the left. This can be easily shown by noting that the generator polynomial g(x) is a divisor of $x^n + 1$. Another important point to note before the decoding algorithm is presented is that three or fewer errors occurring in the codeword with at least one of the errors falling in the message bit positions will always cause the weight of s(x) to be ≥ 4. The proof of this follows.

Let s(x) be the syndrome associated with a transmitted codeword t′(x) corrupted with an error pattern e(x), ie

$$[t'(x) + e(x)] \bmod g(x) = s(x)$$

Define a second codeword a(x) as follows

$$a(x) = t'(x) + e(x) - s(x)$$

Because it is a multiple of g(x), a(x) is a valid codeword. Now, the distance d between a(x) and t′(x) is

$$d = w[t'(x) - a(x)] \geq 7, \quad w = \text{"weight of"}$$

Substituting for

$$a(x),\ w[e(x) - s(x)] \geq 7$$

if

$$w[e(x)] \leq 3$$

then

$$w[s(x)] \geq 4, \text{ QED}$$

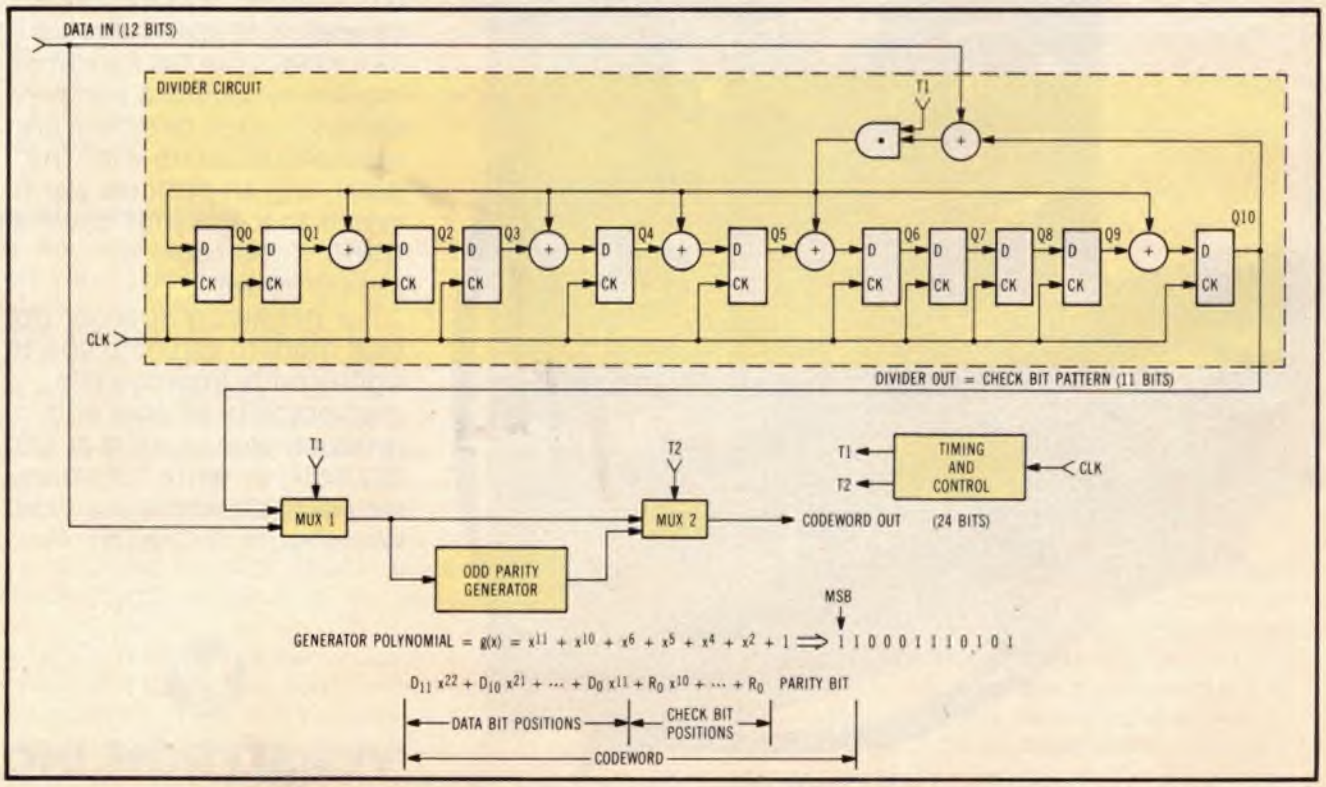

Fig 3 Extended Golay encoder hardware. Note use of XOR gates between storage elements of shift registers for modulo 2 addition.

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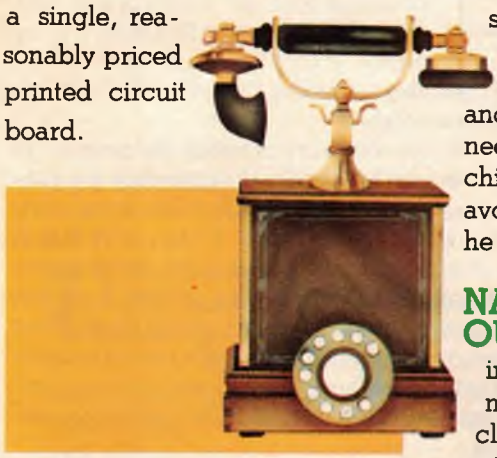

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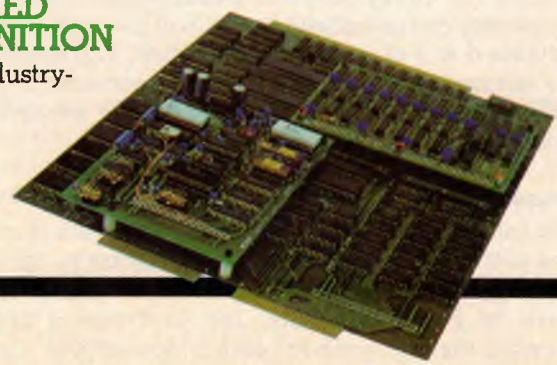

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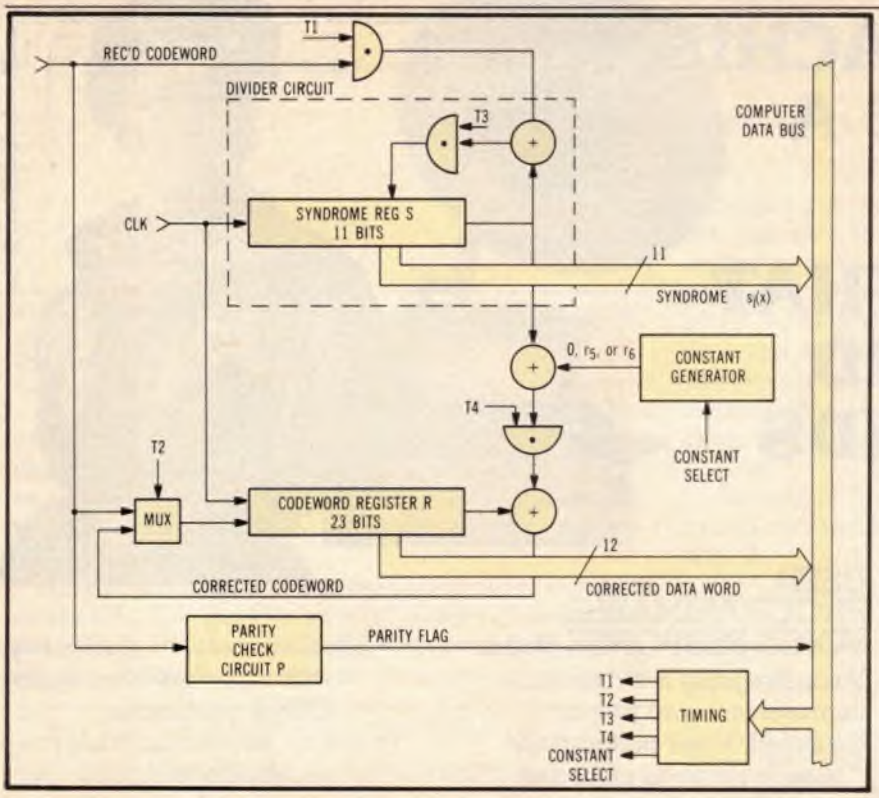

Fig 4 Block diagram of extended Golay decoder hardware

Based upon these facts, Kasami developed the following algorithm for detecting and correcting three or fewer errors in the received codeword

- Calculate the syndrome $s_j(x)$ of the received codeword ($j = 0$ on the first pass). If $w[s_j(x)] \leq 3$, then all the errors are confined to the parity check positions and the syndrome polynomial is equal to the error pattern polynomial.
- If $w[s_j(x)] > 3$, then check to see if the fifth or sixth bit positions of the data word have errors by subtracting modulo 2 $r_5(x)$ or $r_6(x)$, respectively, from $s_j(x)$. If $w[s_j(x) - r_m(x)] \leq 2$, then there is an error in the fifth ($m = 5$) or sixth ($m = 6$) message bit position and $s_j(x) - r_m(x)$ is the error pattern for the check bit positions.
- If $w[s_j(x) - r_m(x)] > 2$, then cyclically shift the received codeword one bit position and repeat steps 1 and 2. It can easily be proved that the syndrome of a cyclical shift of a codeword v(x) is equal to a cyclical shift of the syndrome in the shift register divider. Up to 23 shifts can be required to correct to some valid codeword, or to find the received codeword uncorrectable.

Since the Golay code is a perfect code, the received codeword, corrupted with errors, will always be within a distance $d \leq 3$ of some valid codeword. This means that the received codeword will always be corrected to some valid codeword (granted, it may be the wrong codeword) unless four errors are detected.

Decoder implementation

The extended Golay (24,12) decoder uses both hardware and software. A functional block diagram of the hardware is given in Fig 4 and a flowchart of the software is given in Fig 5. Basically, the hardware is used to generate the syndrome for each codeword and the software is used to calculate the weights of the syndrome and to control the overall operation of the decoder. Referring to the block diagram in Fig 4, the received codeword is serially and simultaneously shifted into the shift register divider, the codeword register R, and the parity check circuit P. The shift register divider divides the received codeword polynomial t(x) by the generator polynomial g(x) to generate the syndrome polynomial s(x). The shift register divider is identical to the shift register divider incorporated in the encoder.

After the 23-bit codeword has been shifted into the divider, the shift register S contains the first syndrome, $s_j(x)$ ($j = 1$). The computer then reads the 11-bit syndrome (see Fig 4) and calculates its weight. If $w[s_j(x)] < 3$, a valid correcting pattern has been found and all the errors are confined to the check bit positions. In this case, the syndrome is equal to the error pattern. If the $w[s_j(x)] = 3$, the parity flag is checked. If the parity flag indicates a parity error, at least 3 errors occurred and the codeword is corrected. If the parity flag indicates no parity error, at least four errors have occurred, possibly including the parity bit, and the codeword is uncorrectable.

If $w[s_j(x)] > 3$, the codeword is tested for an error in either the fifth or sixth message bit position by subtracting $r_5(x)$ or $r_6(x)$ modulo 2, respectively, from $s_j(x)$. If in either case, $w[s_j(x) + r_m(x)] = 2$, the parity flag is checked and, if a parity error is indicated, three errors have occurred and a valid correcting pattern has been found. If the parity flag indicates no parity error, four errors have occurred and the codeword is uncorrectable. If $w[s_j(x) + r_m(x)] > 2$, the codeword and syndrome are cyclically shifted and testing for a valid correcting pattern is repeated.

When a valid correcting pattern is found, the contents of the syndrome register S are set equal to the error correcting pattern and signal T4 enables a gate to serially XOR the correcting pattern with the codeword. The correcting pattern is either the syndrome itself or the syndrome XORed with $r_m(x)$ plus the error in message bit position 5 or 6. After the correcting pattern has been XORed with the codeword, the 12 corrected message bits are read by the computer.

Summary

The actual design and use of an extended Golay (24,12) encoding/decoding scheme can detect and correct up to three randomly spaced errors and detect up to four randomly spaced errors in the codeword. The encoder and decoder reside in a communication interface unit that links synchronous and asynchronous multirate data terminal equipment with a communication network.

The encoding scheme is straightforward and presents few problems. The decoding scheme however, is more complex. A decoding scheme presented by Kasami forms the basis of the decoder.

The encoding scheme is hardware based while the decoding scheme is implemented in both hardware and

ENCODING/DECODING TECHNIQUES DOUBLE FLOPPY DISC CAPACITY

Double-density storage increases standard disc capacity without requiring modifications to the drive unit. Evaluation of different encoding, decoding, and format schemes shows how each impacts critical design considerations

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Ever increasing data storage requirements have caused designers to investigate new methods of expanding the 410k-byte single-density capacity of the standard 8" (20-cm) floppy disc. Double-density encoding, double-sided recording, and double-track density are the methods most often evaluated. Of these three, only double-density encoding has the advantage of doubling the system disc capacity with the same floppy disc drive used for single density. Additionally, improvements in head and media resolutions have made double-density encoding a highly reliable storage technique.

To double disc data density, one of several different encoding and decoding schemes can be implemented. Of these, modified frequency modulation encoding has become virtually the industry standard because of support by IBM as well as by several floppy disc controller chip manufacturers. With this method, twice as many data bits can be written on the disc medium than with single-density encoding. This increased storage impacts the design of the disc controller and the format of the medium. It also makes the decoding of data bits more susceptible to bit shift problems, in which bits are shifted away from their nominal positions. These effects must be carefully considered in the design of a double-density disc controller if soft error rates comparable to those of single-density drives (1 in 10^9 bits) are to be maintained.

Single-Density Encoding Schemes

The fact that double-density controllers are more complex in design is easily explained by examining the differences between single- and double-density encoding. Parameters of various single- and double-density schemes are compared in the Table.

Frequency modulation (FM), based on the IBM 3740 method of encoding (Fig 1), is the industry standard

Single- and Double-Density Encoding Parameters

Parameter	Recording Technique FM	MFM	M²FM	GCR
Bit Cell	4 μs	2 μs	2 μs	1.6 μs
Flux Changes/Cell	2	1	1	1
Flux Changes/in	6536	6536	6536	8170
Data Rate (kilobits/s)				
Storage Device	250	500	500	625
System	250	500	500	500
Frequency Ratios	2/1	2/1	2.5/1	3/1
Bit to Bit Spacings	2 μs	2 μs	2 μs	2 μs
	4 μs	3 μs	3 μs	3.2 μs
		4 μs	4 μs	4.8 μs
			5 μs	
Diskette Capacity (kilobytes)	410	820	820	820

method of single-density encoding. With this scheme, a clock bit is written at the beginning of each bit cell, and data bits are written between clock pulses. Each bit cell is 4-μs wide with the data bit written in the middle of the cell, or 2 μs after the clock bit. Effectively, this scheme amounts to two flux changes per bit cell.

To decode a data bit in single-density recording, the data separator generates a 2-μs data window 1 μs after the clock pulse. Therefore, the data window—centered around the expected position of the data bit—allows the presence or absence of a data bit to be detected. Due to the 2-μs size, bits, even if shifted, are still likely to remain inside the window.

A constant bit cell reference, provided by the clock bit, simplifies encoding and decoding with this scheme (Fig 2). Many large scale integrated (LSI) disc controller chips are available to handle single-density data encoding and disc drive interfacing. The data separator circuit required to decode single density usually consists of simple timing circuits that generate the 2-μs data window.

Higher-Density Encoding Schemes

Three double-density encoding schemes are presently used to increase floppy disc capacity: modified frequency modulation (MFM), modified-modified frequency modulation (M^2FM), and group coded recording (GCR). Each scheme increases disc capacity by replacing clock bits with data bits, using slightly different techniques. In each scheme, data rate as well as drive capacity is increased. The increased data rate might not affect controller design since most controllers incorporate a data buffer to transfer data asynchronously. Encoding schemes, however, do affect disc controller design.

MFM Encoding

With available head and media technology, MFM encoding is the most easily implemented and may become the industry double-density standard. It is used in the IBM System 34 and in all available double-density LSI disc controller chips. MFM encoding doubles floppy disc data capacity to 820k bytes by replacing the clock bit positions (used in FM encoding) with data bits (Fig 1). This scheme reduces the size of the bit cell by one-half to 2 μs, thereby doubling data bit capacity.

Clock bits are still used, but are written only when data bits are not present in both the preceding and the current bit cell. As a result, there is only one flux change per bit cell. Clock bits are written at the beginning of the bit cell, while data bits are written in the middle, or 1 μs after the bit cell's leading edge.

To decode data bits in MFM encoding, a data separator must generate a 1-μs data window and a 1-μs data window complement for a clock window. Because not every bit cell has a clock pulse, the data/clock windows cannot be timed from the clock pulse. Instead, the data separator must continuously analyze the bit position inside the windows so that the data/clock windows remain synchronous with the data/clock bits. Ideally, the bit will appear at the center of the window. However, data bits can shift outside the 1-μs data window due to bit-shift effects.

Consequently, data separator design, as well as overall disc controller design, for double-density encoding is more complex than for single-density encoding. Present LSI controller chips can handle the drive interface, double-density encoding function, and bit-shift pattern detection. However, bit-shift compensation circuits and a high resolution analog data separator must be added (Fig 2).

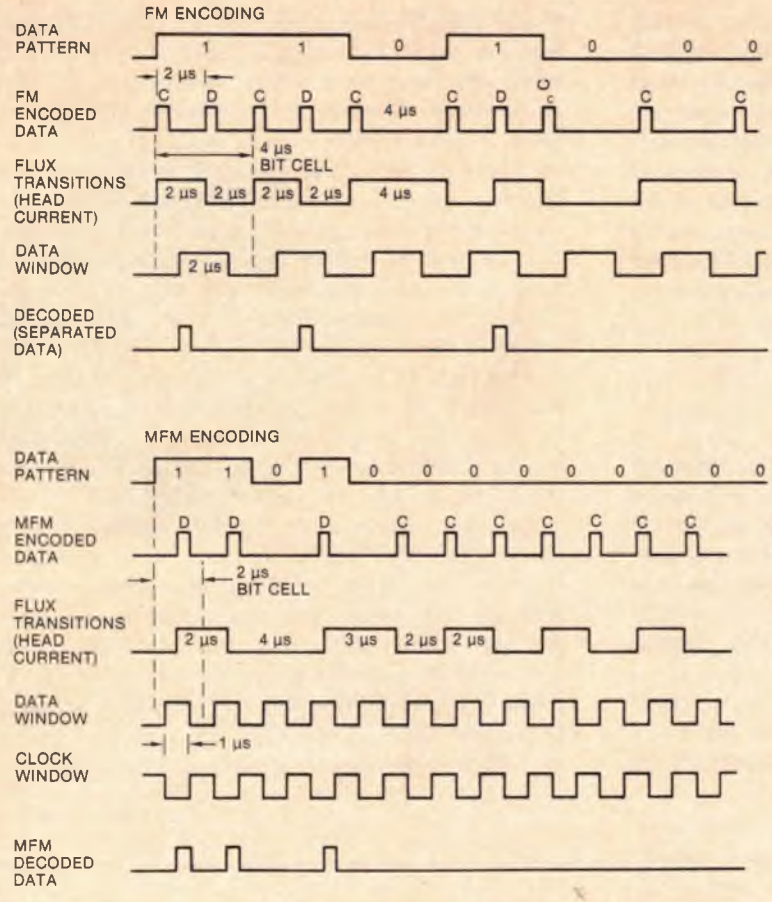

Fig 1 FM vs MFM encoding schemes. MFM encoding doubles number of data bits on disc media by replacing clock bits used in FM encoding with data bits. Scheme reduces bit cell width from 4 to 2 μs and reduces data window to 1 μs

Despite these constraints, disc controller design for MFM is simpler than that for either of the other two double-density encoding schemes.

M²FM Recording Scheme

Until recently, M²FM has been the commonly used double-density encoding scheme, because the resolution of the medium and the read/write head was not adequate for the 1-μs data window used in MFM. In M²FM, a clock is written only if no data or clock bit is present in the preceding bit cell, and no data bit occurs in the current cell. Because clock pulses are relatively isolated on the medium, the effect of bit shift on clock pulses is minimal. Therefore, a narrower clock window can be used to decode the clock pulse. The width of the data window can thus be increased to 1.2 μs, which allows more margin for shifted data bits.

Today's ceramic based read/write heads have much better resolution than those used in the past. This head design reduces the effects of bit shift, and makes the window margin provided by M²FM unnecessary. Additionally, M²FM is subject to a droop problem, which occurs in the read amplifier circuit when a low frequency pattern is read.

GCR Encoding

GCR encoding evolved from methods used in magnetic tape recorders. This method translates four data bits

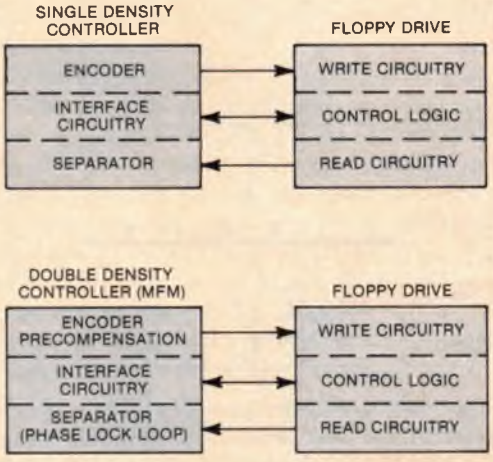

Fig 2 Single- vs double-density circuits. Effects of bit shift require more complex circuits for double-density floppy disc controllers than for single-density controllers. In addition to different encoding circuits, bit-shift compensation circuits are necessary, as well as high resolution analog data separator

into a 5-bit code during a write (Fig 3). During a read, the 5-bit code is retranslated to four data bits; no clock bits are generated. Using data rates specified by drive manufacturers, this scheme results in an 80% increase in density rather than a 100% increase. If the data rate is increased to provide double density, the number of flux changes per inch increases beyond reliable limits for floppy disc drives. This method requires more circuits to code, decode, and provide necessary lookup tables, and costs more than either of the other two double-density encoding schemes.

Bit-Shift Calculations

Bit shift occurs on any NRZ (nonreturn to zero) recorded medium—single or double density. Using the NRZ method, data are recorded by reversing polarity of current flow for each flux transition. This shift is, however, more noticeable with double density due to smaller bit cells and resulting smaller data/clock windows. Some aspects of bit-shift phenomena are predictable; other aspects are not.

Predictable bit-shift effects result from normal read/write head operation. Data are written when the read/write head generates a flux change in the gap of the head, which causes a change in magnetization of the medium oxide. In reading, a current is induced into the read/write head when a flux transition on the medium is encountered. The current change is not instantaneous, since it takes a finite time to build up to peak and then to return to zero (Fig 4). If flux transitions are close together, the current buildup after one flux transition declines, but it does not reach zero before a second transition begins. When current pulses are summed by the read/write head, the peaks are shifted. A negative flux change, for example, appears late because it has been added to the remnant of a positive transition.

This type of bit shift is predictable. Spacing between bits results in greater bit shift on the inner tracks (43 to 76) of the floppy disc (Fig 5). On those tracks, bits can be expected to shift up to 350 ns. On the outermost tracks (00 to 42), bit shift is negligible.

However, other causes for bits shifting from the position where they are written are not predictable. Variations in disc drive rotational speed can cause bits to shift by a constant, but unpredictable, amount. Drives are specified as 360 r/min ±2% rotational speed. The 2% variation includes a 1% allowance for 120-Vac line frequency variations and a 1% allowance for belt pulley tolerances. These variations will shift bits by as much as ±40 ns from their originally written positions.

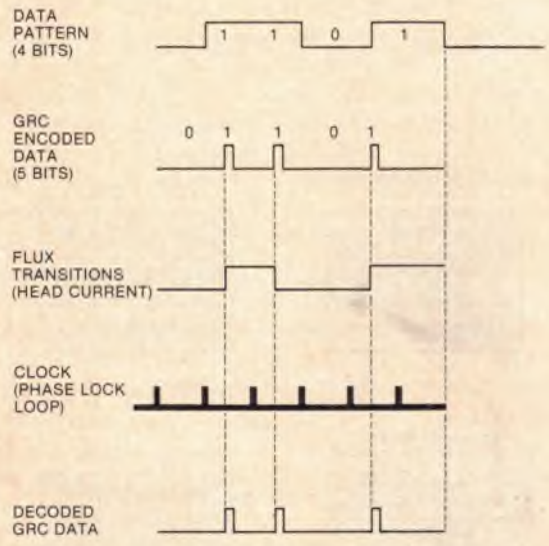

Fig 3 GCR encoding scheme. Four data bits are translated into 5-bit code during write; for example, data pattern 1101 is encoded into serial bit stream 01101, according to GCR encode rules. To decode, data window is generated around expected position of each bit. Result is serial read data of 01101, which must be decoded to 1101 by lookup table circuitry

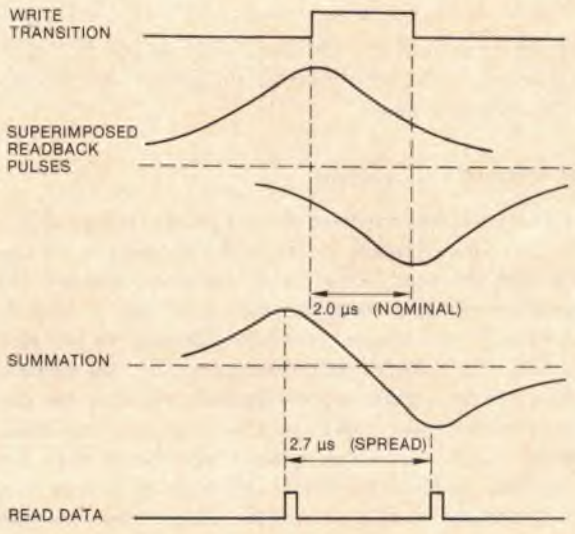

Fig 4 Bit-shift effects. During reading, bits are shifted predictably from their written positions as result of normal read/write head operation. When flux change occurs on medium, current is induced into read/write head. Current change is not instantaneous, since finite time is required to build up to peak and then to return to zero. If flux transitions are close together, current buildup after one flux transition declines, but does not reach zero before second transition begins. Peaks shift when current pulses are summed by read/write head

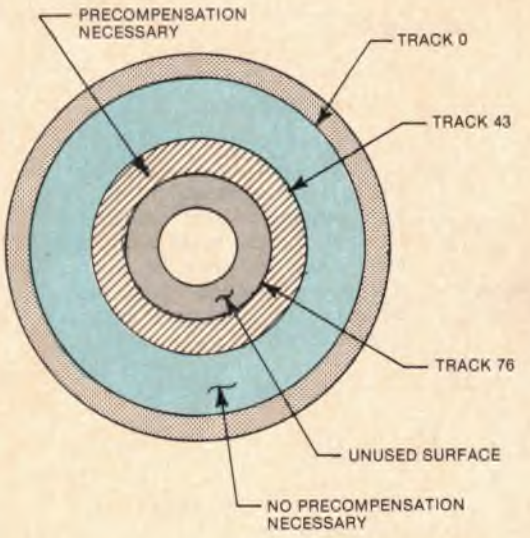

Fig 5 Bit shift vs track position. Significant bit shift occurs on innermost tracks of floppy disc (43 to 76) because bits on these tracks are packed closer together and therefore are more susceptible to bit shift. On outermost tracks (00 to 42) bit density is less, so that predictable bit shift is minimal

Instantaneous speed changes, although smaller than rotational speed changes, also cause bits to appear shifted; this shifting effect varies from drive to drive. Write over, or incomplete erasure of, previously recorded data can also shift bits. These shifts can range up to ±50 ns; again, they are variable and unpredictable. Other variable components of bit shift include electrical noise, radial alignment (offtrack), and nonsymmetry of the read/write head and associated electronics.

A bit shift of up to ±450 ns can be expected. This number is obtained using observed figures for predictable and unpredictable components of bit shift.

Double-Density Controller Chip Design

Both predictable and unpredictable bit shifts must be accommodated in the design of a double-density disc controller if data are to be read reliably. Controller chips reliably perform MFM encoding and decoding. To compensate for predictable bit shift, however, compensation circuits must be added, and the data separator circuit must generate and position a high resolution data window so that a bit can be read reliably even if unpredictably shifted.

Despite the problems posed by bit shift, double-density controller design has been simplified with the recent introduction of LSI controller chips. For example, the NEC uPD765 and the Western Digital FD1791 perform MFM encoding and decoding as well as pattern detection to provide signals that identify which bits will be predictably shifted. These chips also perform serial/parallel conversion, generate cyclic redundancy check (CRC) characters for error detection, provide write current switches to reduce write current as density increases on the track, perform address mark detection for the IBM double-density format, and furnish intelligent status reporting. Both chips interface to commonly available 8-bit microprocessor based interface systems. Although they differ in software overhead and in hardware interface signals, the two chips are functionally the same.

Discrete logic circuit implementation of the same controller chip functions typically requires at least 60 to 70 integrated circuits (ICs), including a dedicated microprocessor, although greater format flexibility is possible than with the LSI chips, which require fixed gap lengths in the formats. Bipolar logic implementations of the same controller chip functions also result in a larger part count. Because some error detection functions can be performed in software, the bipolar parts count is somewhat less than that of discrete logic parts. Still, either method is substantially more complicated than the LSI chip implementation.

Bit-Shift Compensation Circuits

Since some aspects of bit shift can be predicted, it is possible to compensate for this shift within the design of the disc controller. Two methods currently being used are precompensation and postcompensation.

With precompensation, bits are deliberately shifted in the direction opposite that of the expected shift. As data are being written, the LSI controller chip detects bit patterns. From these bit patterns, the controller calculates which bit will shift in which direction. Since bit shift is negligible for the first 43 tracks of data, the controller issues no precompensation signals until after track 43.

For example, a 4-bit pattern of 0110 on an inner track would cause the third bit to appear as much as 350 ns later than its nominal position. The controller chip, after detecting this late bit-shift pattern, would generate an early signal, indicating that the third bit should be written earlier to make it appear closer to its nominal position when read. Conversely, if the third bit were going to appear early, a late signal would be generated so that the bit could be written later.

How early or late the bit should be written is a function of its position in the data pattern and its track position, among other factors. The shift at middle and outer tracks can range from 50 to 350 ns. For optimum precompensation in all cases, 150 to 175 ns of precompensation is recommended for both early and late bits. Timing circuitry that achieves this precompensation includes counters, shift registers, delay lines, and 1-shot delay circuits.

For example, a 1-shot precompensation circuit (Fig 6) is connected to the controller chip early- and late-bit signals. Based on precompensation of 175 ns, a 300-ns delay is used for an on-time bit, a 125-ns 1-shot delay is used for a bit to be written early, and a 475-ns 1-shot is used for a bit to be written late. The trailing edge of

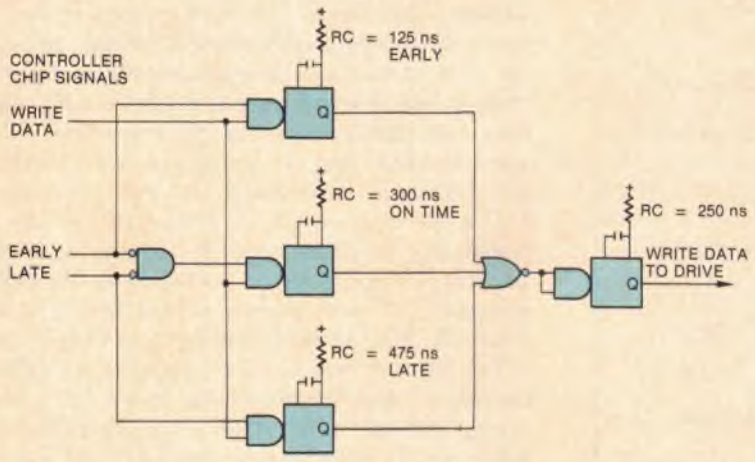

Fig 6 Precompensation circuit. To compensate for predictable bit shift, circuit writes early bits that would normally be shifted late during reading. Conversely, bit expected to appear early is written late

each of these 1-shot pulses fires a fourth 1-shot to provide a standard width write pulse to the disc drive.

Postcompensation alters the read signal rather than the write signal. Since bit shift is, in part, a function of read channel frequency response (phase characteristics), postcompensation circuitry changes the read signal after track 60 to compensate for bit shift. This IBM method is relatively new; floppy discs written on System/34 are incompatible with disc drives that do not use postcompensation.

Data Separation

Substantial reductions in the amount of bit shift can be achieved using either a pre- or post-compensation method. However, unpredictable bit shift can still occur. Therefore, special design consideration must be given to the type and resolution of data separator used in reading data bits from the disc.

The bit stream transferred from the disc to the controller consists of composite clock and data bits. With single density, a data bit is decoded by a data window that is generated from the clock bit. In double density, the lack of consistent clock bits makes it impossible to generate a data window in this manner. Instead, the separator circuit must first determine the nominal position of clock and data bits and then generate a 1-μs clock and data window that is centered around the bit positions. The more accurately the bit position can be determined and the tighter the resolution of the data window, the lower the soft error rate of the disc.

The 1-μs data window must be centered on a bit that can potentially shift as much as $\pm$450 ns. This shift leaves less than a 50-ns margin to the edge of the window; a data bit appearing on the edge of the data window could be read as a clock bit. The total error from the data separator circuit must therefore be less than $\pm$50 ns.

To determine the nominal bit position around which to center the window, the data separator must track data bit frequency changes. In this manner, even if an unpredictable bit shift occurs, the data separator can adjust the window's position to compensate for the change. Otherwise, the shifted bit could be positioned outside the window. To remain within the error rate specified by drive manufacturers, not more than 1 in 10^9 bits can appear outside the window. With present technology, only an analog data separator based on a phase-lock loop technique can provide the necessary reliability.

Digital data separators have lower resolution than an analog phase-lock loop type of separator, and cannot accurately determine the nominal position of the data bit around which to position the window. As a result, error rates higher than those specified may result from the use of digital data separators.

For clarity, the performance of a typical digital data separator is examined. To generate a data window, a crystal clock is divided down by a value preloaded in a counter to create a 50/50 data/clock window. Assuming that a 20-MHz clock is used, the smallest increment to which the window can be adjusted is the least significant bit (LSB) of the counter, which in this case is 50 ns. The separator determines the nominal bit position around which to center the data/clock window by sampling bit positions within the window. From sampling results, the data separator adjusts the window position using a feedback mechanism that changes the preload value in the counter. This effectively shifts the window position relative to the nominal bit position.

The 50-ns resolution, however, creates a problem. As shown in Fig 7, if a bit is shifted a maximum of 450 ns in one direction, the digital data separator will compensate by moving the window 1 LSB or 50 ns in that direction. If a subsequent bit is then shifted 450 ns in

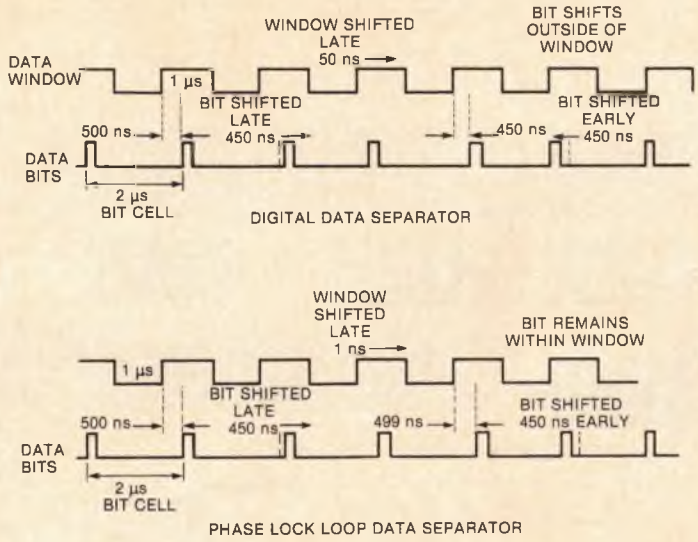

Fig 7 Data separator timing diagrams. Unpredictable bit shift is handled differently by digital and analog data separators. Typical digital data separator, using 20-MHz clock, provides 50-ns resolution. Assuming two worst case bit shifts in opposite directions, data bit would appear outside data window. Analog data separator, however, provides 1-ns resolution. As result, it can handle unpredictable bit shift more reliably than digital data separator

the opposite direction, that bit will appear 50 ns outside the window, resulting in a misread.

An analog phase-lock loop separator, on the other hand, has tighter resolution (±1 ns) and handles bit frequency changes more reliably (Fig 7). With this method, a phase-lock loop locks onto the basic frequency of data bits read off the disc, and determines nominal bit positions for data and clock bits by sampling every bit (clock and data). It uses the phase relationship between a bit and its window to vary the position of the window. By sampling each bit, the phase-lock loop determines the phase error between a bit and the frequency being generated.

Changes in the data window position depend both on an integration factor and on the amount of bit position error. For an integration factor of 100:1, the data window would move 1 ns per bit cell for each 100-ns change in bit position, until the entire error had been compensated.

Using the same example as described for the digital data separator, the phase-lock loop would detect the data bit shifted late by 100 ns. Then, the data window would be adjusted so that it appeared 1-ns late. If the next bit is shifted early, the analog separator would also detect that shift and position the next data window, not late, but early. In this manner, the phase-lock loop reliably tracks frequency changes. A block diagram of a typical phase-lock loop circuit is shown in Fig 8.

Double-Density Formats

In double density, data are encoded differently from single density, but are formatted more or less identically on the disc. Each of the 77 data tracks on a standard 8″ (20-cm) floppy disc is organized in data records, which are also referred to as sectors. Two methods of sectoring currently exist: hard and soft. In the more prevalent soft sectoring, the number of sectors and their length can vary. Optimum sector size for systems with small main memories and smaller data bases may be as low as 128 bytes. For those systems with larger main memories and large data bases, 256 or 512 bytes per sector may be optional.

Soft sectoring is supported by IBM in both double- and single-density controllers. The double-density format shown in Fig 9 is used in the IBM System/34 and will likely become the industry standard. It is also the format supported by available LSI disc controller chips. Similar in most respects to the standard single-density format, the double-density format has the same number of sectors (26), each with twice as many bytes (256).

Double-density format differs from single-density format in the way an address mark is detected. An address mark flags the beginning of every index, identification (ID), and data field. In both single- and double-density recording, the address mark is unique in terms of its clock pattern; the single-byte single-density address mark contains two or three missing clock pulses.

This method is modified for double density because dropping two or three clock bits in a row could cause the data separation circuit to lose synchronization. In double density, each of the first three bytes of a 4-byte address mark has one active data bit followed by four zero data bits. According to double-density encoding protocol, the three zero data bits should have an associated clock pulse. However, to make the address mark unique, the middle clock pulse is dropped. The respective address marks for index, identification, and data fields are made unique by their associated data pattern. For example, an index address mark has three C2 bytes (hexadecimal), followed by an FC byte; an ID address mark has three A1 bytes followed by an FE byte; and

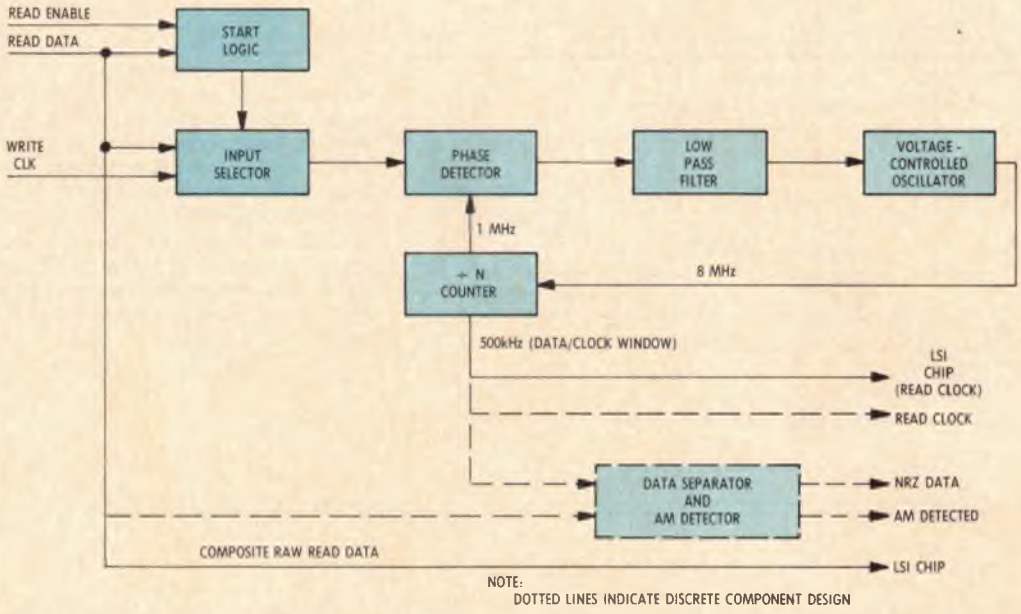

Fig 8 Analog phase-lock loop data separator. Input selector selects write clock signal as input to phase detector until start logic has detected synchronized area preceding address mark of formatted disc. At that point, input selector switches from write clock to read data as input to phase detector. Phase detector then begins sampling difference between read data and output of voltage controlled oscillator (VCO). A ÷ N counter continually divides VCO frequency down to same frequency as read data. Finally output of ÷ N counter becomes data/clock window

data has three A1 bytes followed by an FB byte. This bit pattern is automatically generated by the controller chip, as is the CRC character at the completion of the data and ID field.

Obviously, LSI controller chips simplify disc formatting, but offer some limitations on format flexibility. If a designer chooses to configure a custom format, certain design guidelines for gap length must be observed if data are to be recorded reliably.

Gap 1 of 22 bytes must be present if an index address mark is used to separate the index address mark from the first identification field. Gap 2 of 22 bytes, which separates the identification and data fields, is necessary to protect the ID field from erasure during a write. Gap 3 of 54 bytes is a speed tolerance gap, which again protects the ID field if the medium is interchanged between drives with different rotational speeds. Gap 4 is also a speed tolerance buffer. This gap length is determined by the difference between the format length and the actual track capacity, which may vary from drive to drive.

A double-density format (shown in Fig 9) is, with some exceptions, the same as a single-density format with gaps and data fields that are twice as long.

Summary

Improvements in head and media resolution have made double-density encoding a reliable method of doubling the capacity of a floppy disc from 410k to 820k bytes. A minifloppy drive, using double density, can increase its capacity from 110k to 220k bytes. Research analysis into the problems of bit shift has enabled designers to reliably compensate for bit-shift effects so that a minimum soft error rate in excess of 1 in 10^9 is possible with double-density encoding. LSI controller chips have made double-density system design less complex, less time consuming, and therefore less costly. In addition, double-density floppy discs with doubled capacity can be implemented on single-density drives. These capabilities

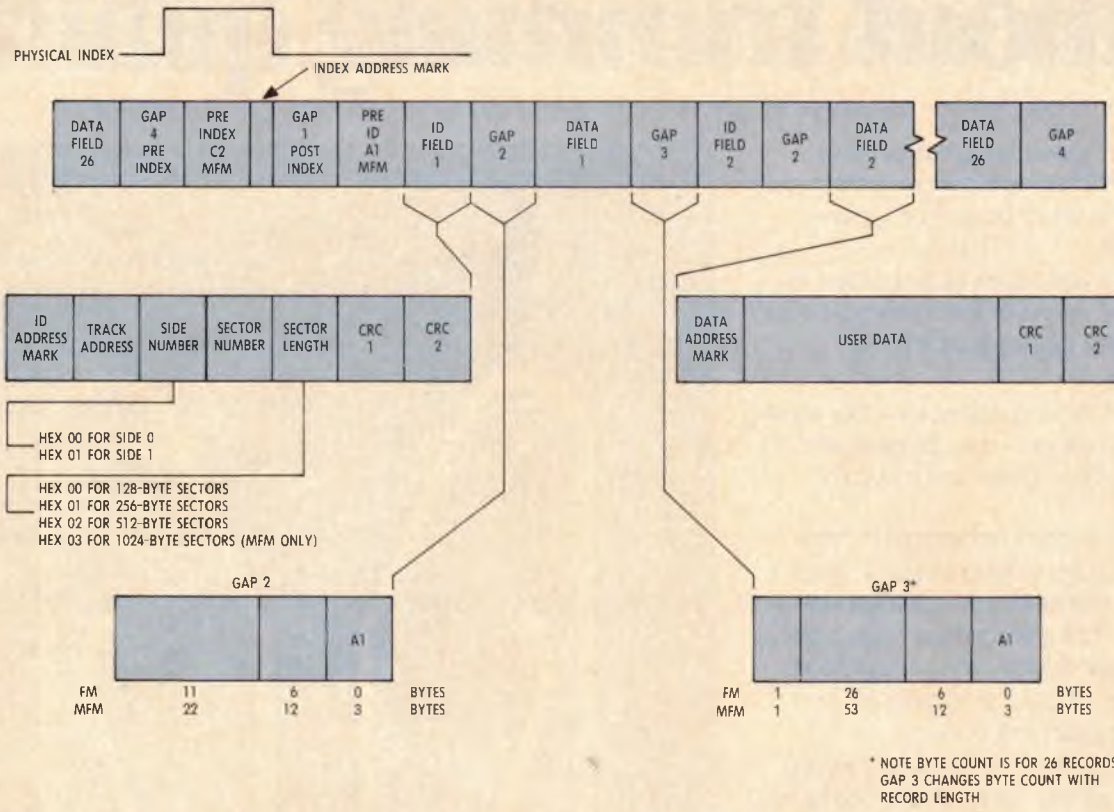

Fig 9 Double-density format. Defacto industry standard MFM double-density format. Within each sector, 4-byte address mark flags beginning of every index, identification, and data field. Address marks are distinguished from data by missing middle clock pulse in each of first three bytes. Index, ID, and data field address marks each have unique data clock pattern

should broaden the applications of floppy disc drives and make systems with multiple floppy disc drives more compact.

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Larry H. Wall is manager of product engineering at Shugart, and is responsible for the electrical components within floppy disc drives. His experience includes the design of an IBM compatible VFO. He holds a BSEE degree from California Polytechnic State University and is currently working on a masters degree in engineering management at Santa Clara University.

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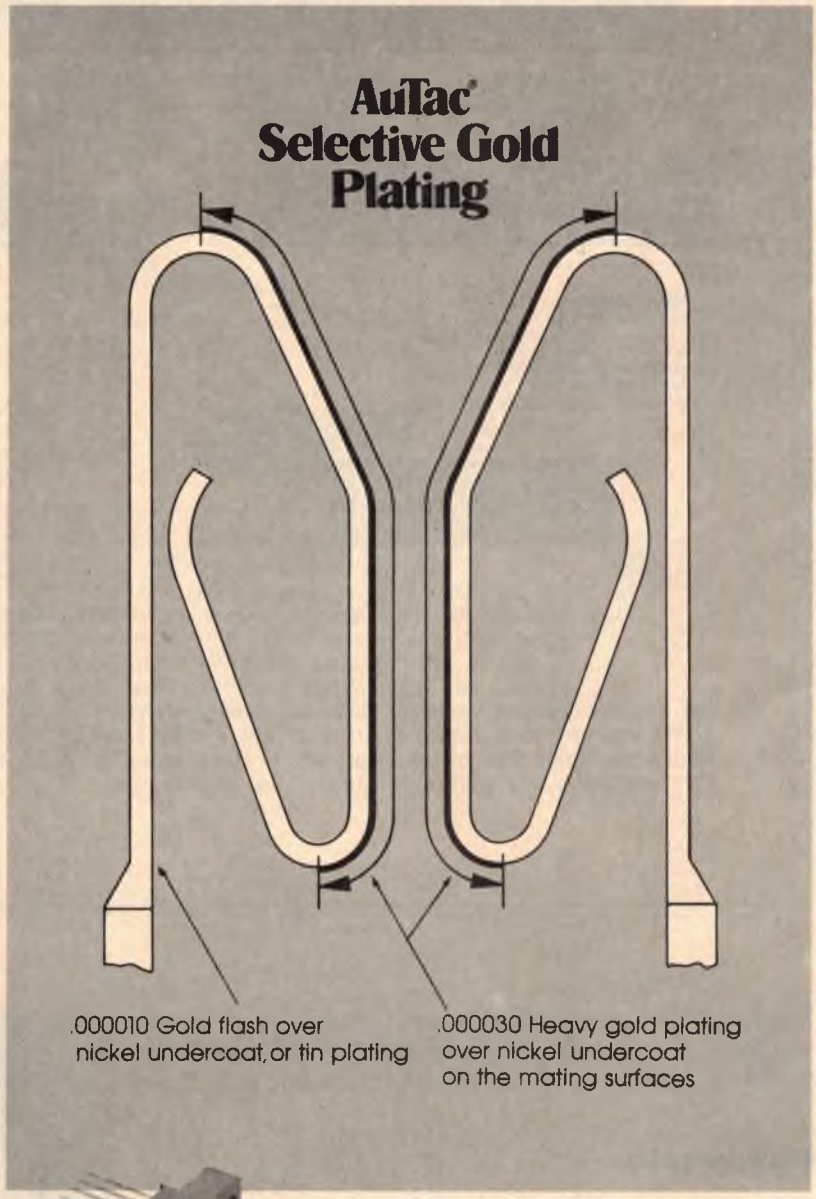

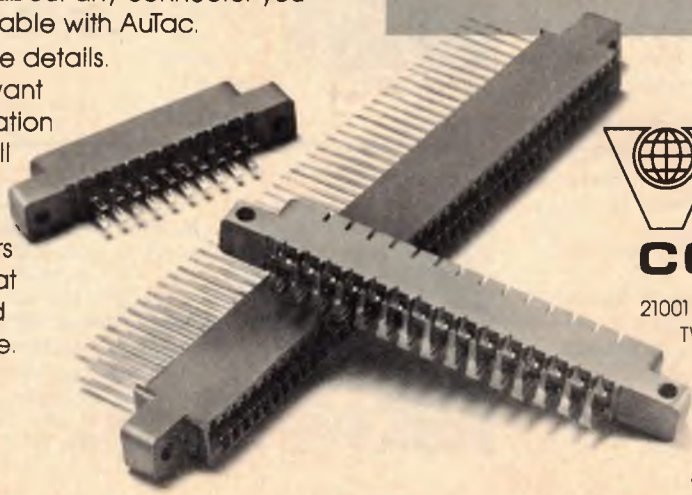

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CIRCLE 78 ON INQUIRY CARD

Program noise-bandwidth and rms-voltage computations into a calculator

Often, while designing analog circuits like amplifiers and filters, you have to compute and recompute equivalent noise bandwidth (NBW) and rms output-voltage response (V_{eq}) to a broadband noise input. To cut the work and ensure correct results, use a programmable calculator. With the proper program, calculated results should fall within 2% of the measured values.

Before rushing to a calculator, however, look at two important equations used for determining rms-noise voltages. One deals with periodic waveforms and the other with nonperiodic. Note that spectra for periodic waveforms have a finite number of frequency components; but the number for nonperiodic waves is infinite. For example, in a periodic waveform made up of just two frequencies, f_1 and f_2, with respective rms amplitudes V_1 and V_2,

$$V_{eq} = \sqrt{V_1^2 + V_2^2}$$

The equivalent rms voltage equals the root of the sum of the squares of the individual rms voltages.

With all frequencies present, nonperiodic-waveform spectra are continuous and best represented by spectral-density functions. Thus the total rms voltage of a nonperiodic waveform:

$$V_{eq} = \sqrt{\int_0^\infty [V(f)]^2 \, df},$$

where V(f) is a continuous spectral-density function, with dimensions

$$V_{rms}/\sqrt{Hz}.$$

For broadband (white) noise applied to a circuit whose transfer function is H(f),

$$V_{eq} = K\sqrt{\int_0^\infty [H(f)]^2 \, df} \qquad (1)$$

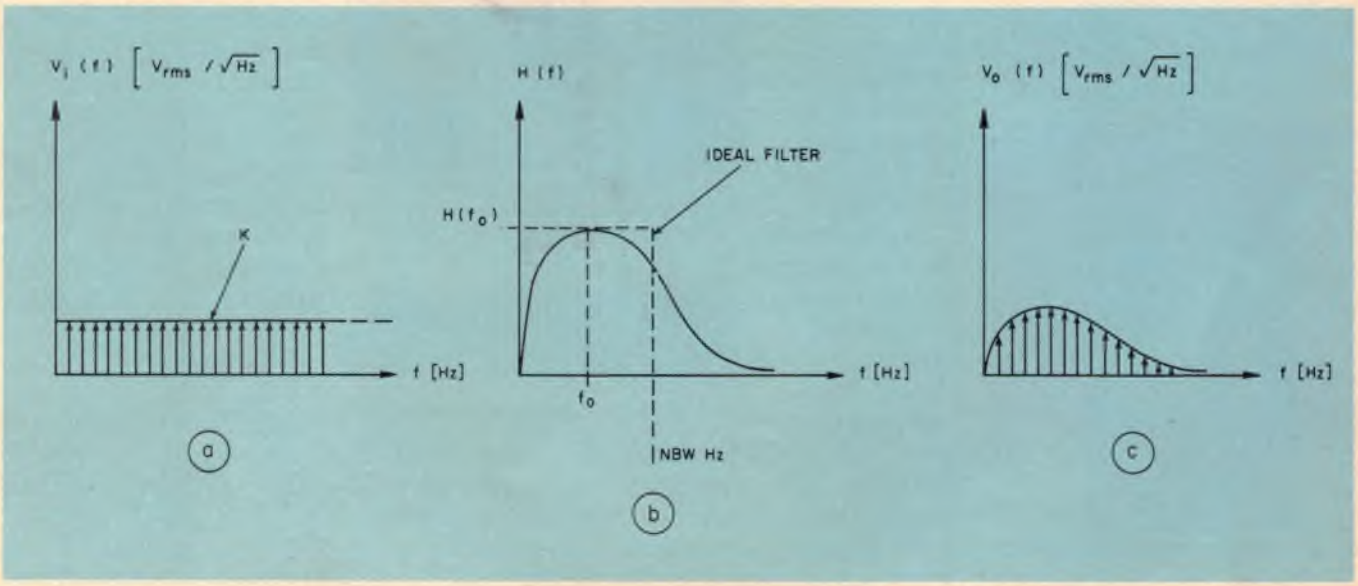
Thus, knowing a circuit's transfer function and the spectral density of its broadband-noise input, K, lets you calculate the rms output voltage that a true-rms meter would indicate.

For equivalent noise bandwidth, useful in linear-circuit analysis,

$$NBW = \frac{1}{[H(f_0)]^2} \int_0^\infty [H(f)]^2 \, df, \qquad (2)$$

where f_0 is the frequency at which H(f) is maximum.

Leland R. Hudson, Electronics Engineer, Naval Weapons Center, Code 3314, China Lake, CA 93555.



1. **Broadband-noise performance** of a circuit with transfer function H for white-noise input (a) is the same as that of an ideal filter with $H(f_0)$ gain and NBW bandwidth (b). The spectral density (c) combines (a) and (b).

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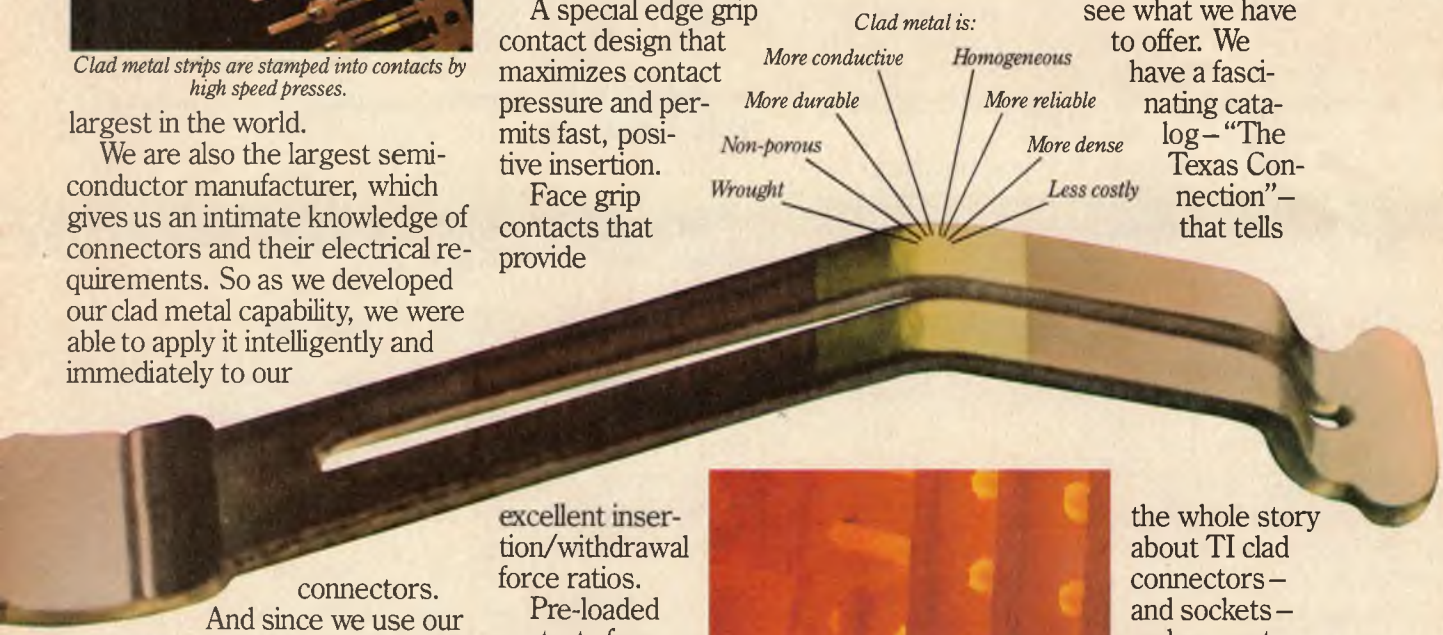

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TEXAS INSTRUMENTS
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CIRCLE NUMBER 62

Table 1. RMS and NBW program

User instructions

Step	Procedure	Enter	Press	Display
1	Partition the calculator	3	OP 17	719.29
2	Enter program (Bank 1,2,3, and 4)			
3	Initialize the program		E′	
4	Define transfer function squared, $H(f)^2$, by starting at Step 459 with LBL A′; end function with RTN statement. Assume f is already in the display register. There are 258 steps available to define $H(f)^2$, and Registers R_{16} through R_{29} are available.	$H(f)^2$	GTO A′LRN	461 92
5	Enter lower integration limit	f_{min} (Hz)	A	f_{min}(Hz)
6	Enter # decade in integration	# decades	B	f_{max} $\int_{f_{min}} [H(f)]^2 df$
7	Calculate NBW			
	a (Hz)		D	NBW (Hz)
	b (dB)		R/S	NBW (dB)
8	Display $H(f_o)$		E	$H(f_o)$
9	Enter spectrum of white noise	$K(V_{rms}/\sqrt{Hz})$	C	V_{rms}

```
 719.29
000  76 LBL
001  10 E'
002  25 CLR
003  69 DP
004  00  00
005  03  3
006  05  5
007  03  3
008  00  0
009  03  3
010  06  6
011  00  0
012  00  0
013  01  1
014  03  3
015  69 DP
016  01  01
017  03  3
018  01  1
019  01  1
020  06  6
021  00  0
022  00  0
023  03  3
024  01  1
025  01  1
026  04  4
027  04  4
028  03  3
029  69 DP
030  02  02
031  04  4
032  03  3
033  00  0
034  00  0
035  03  3
036  03  3
037  03  3
038  05  5
039  03  3
040  02  2
041  69 DP
042  03  03
043  02  2
044  02  2
045  03  3
046  05  5
047  01  1
048  03  3
049  03  3
050  00  0
051  00  0
052  00  0
053  69 DP
054  04  04
055  69 DP
056  05  05
057  98 ADV
058  98 ADV
059  91 R/S
060  76 LBL
061  11  A
062  42 STO
063  14  14
064  69 DP
065  00  00
066  02  2
067  01  1
068  03  3
069  00  0
070  02  2
071  04  4
072  03  3
073  01  1
074  00  0
075  00  0
076  69 DP
077  01  01
078  05  5
079  05  5
080  02  2
081  03  3
082  04  4
083  06  6
084  05  5
085  06  6
```

```
086  06   6
087  04   4
088  69 DP
089  02   02
090  69 DP
091  05   05
092  43 RCL
093  14   14
094  99 PRT
095  91 R/S
096  76 LBL
097  12   B
098  42 STO
099  09   09
100  69 DP
101  00   00
102  01   1
103  06   6
104  01   1
105  07   7
106  01   1
107  05   5
108  01   1
109  03   3
110  01   1
111  06   6
112  69 DP
113  01   01
114  01   1
115  07   7
116  03   3
117  06   6
118  06   6
119  04   4
120  00   0
121  00   0
122  00   0
123  00   0
124  69 DP
125  02   02
126  69 DP
127  05   05
128  43 RCL
129  09   09
130  99 PRT
131  98 ADV
132  25 CLR
133  42 STO
134  07   07
135  42 STO
136  13   13
137  76 LBL
138  17 B'
139  53   (
140  43 RCL
141  14   14
142  65   ×
143  43 RCL
144  07   07
145  22 INV
146  28 LOG
147  54   )
148  36 PGM
149  09   09
150  11   A
151  53   (
152  24 CE
153  65   ×
154  01   1
155  00   0
156  54   )
157  36 PGM
158  09   09
159  12   B
160  01   1
161  00   0
162  36 PGM
163  09   09
164  13   C
165  36 PGM
166  09   09
167  14   D
168  99 PRT
169  44 SUM
170  13   13
171  53   (
172  43 RCL
173  09   09
174  75   -
175  01   1
176  54   )
177  32 X:T
178  43 RCL
179  07   07
180  67   EQ
181  19 D'
182  69 DP
183  27   27
184  61 GTO
185  17 B'
186  76 LBL
187  19 D'
188  43 RCL
189  13   13
190  98 ADV
191  99 PRT
192  98 ADV
193  91 R/S
194  76 LBL
195  13   C
196  22 INV
197  52 EE
198  42 STO
199  10   10
200  69 DP
201  00   00
202  02   2
203  06   6
204  05   5
205  05   5
206  04   4
207  02   2
208  06   6
209  03   3
210  05   5
211  02   2
212  69 DP
213  01   01
214  02   2
215  03   3
216  04   4
217  06   6
218  05   5
219  06   6
220  06   6
221  04   4
222  00   0
223  00   0
224  69 DP
225  02   02
226  69 DP
227  05   05
228  43 RCL
229  10   10
230  99 PRT
231  98 ADV
232  53   (
233  43 RCL
234  13   13
235  34 fX
236  65   ×
237  43 RCL
238  10   10
239  54   )
240  42 STO
241  11   11
242  69 DP
243  00   00
244  01   1
245  03   3
246  03   3
247  01   1
248  03   3
249  06   6
250  04   4
251  03   3
252  01   1
253  07   7
```

```
254  69 DP
255  01  01
256  03  3
257  05  5
258  00  0
259  00  0
260  06  6
261  04  4
262  00  0
263  00  0
264  00  0
265  00  0
266  69 DP
267  02  02
268  69 DP
269  05  05
270  69 DP
271  00  00
272  04  4
273  02  2
274  03  3
275  05  5
276  03  3
277  00  0
278  03  3
279  06  6
280  69 DP
281  04  04
282  43 RCL
283  11  11
284  69 DP
285  06  06
286  98 ADV
287  91 R/S
288  76 LBL
289  14  D
290  29 CP
291  25 CLR
292  42 STO
293  07  07
294  76 LBL
295  38 SIN
296  09  9
297  42 STO
298  08  08
299  01  1
300  42 STO
301  06  06
302  76 LBL
303  39 COS
304  71 SBR
305  30 TAN
306  16 A'
307  18 C'
308  69 DP
309  26  26
310  97 DSZ
311  08  08
312  39 COS
313  69 DP
314  27  27
315  97 DSZ
316  09  09
317  38 SIN
318  01  1
319  42 STO
320  06  06
321  71 SBR
322  30 TAN
323  16 A'
324  18 C'
325  32 X:T
326  42 STO
327  15  15
328  35 1/X
329  65  ×
330  43 RCL
331  13  13
332  95  =
333  42 STO
334  12  12
335  69 DP
336  00  00
337  03  3
338  01  1
339  01  1
340  04  4
341  04  4
342  03  3
343  00  0
344  00  0
345  06  6
346  04  4
347  69 DP
348  01  01
349  69 DP
350  05  05
351  69 DP
352  00  00
353  02  2
354  03  3
355  04  4
356  06  6
357  69 DP
358  04  04
359  43 RCL
360  12  12
361  69 DP
362  06  06
363  98 ADV
364  91 R/S
365  69 DP
366  00  00
367  03  3
368  01  1
369  01  1
370  04  4
371  04  4
372  03  3
373  00  0
374  00  0
375  06  6
376  04  4
377  69 DP
378  01  01
379  69 DP
380  05  05
381  01  1
382  06  6
383  01  1
384  04  4
385  69 DP
386  04  04
387  43 RCL
388  12  12
389  28 LOG
390  65  ×
391  01  1
392  00  0
393  95  =
394  69 DP
395  06  06
396  98 ADV
397  98 ADV
398  91 R/S
399  76 LBL
400  30 TAN
401  53  (
402  43 RCL
403  14  14
404  65  ×
405  43 RCL
406  06  06
407  65  ×
408  43 RCL
409  07  07
410  22 INV
411  28 LOG
412  54  )
413  92 RTN
414  76 LBL
415  18 C'
416  22 INV
417  77  GE
418  58 FIX
419  32 X:T
420  76 LBL
421  58 FIX
```

```
422  92 RTN
423  76 LBL
424  15  E
425  69 OP
426  00  00
427  02  2
428  03  3
429  05  5
430  05  5
431  02  2
432  01  1
433  05  5
434  06  6
435  00  0
436  00  0
437  69 OP
438  01  01
439  03  3
440  00  0
441  01  1
442  03  3
443  04  4
444  04  4
445  00  0
446  00  0
447  06  6
448  04  4
449  69 OP
450  02  02
451  69 OP
452  05  05
453  43 RCL
454  15  15
455  34 FX
456  99 PRT
457  98 ADV
458  91 R/S
459  76 LBL
460  16 A'
461  92 RTN
462  92 RTN
463  92 RTN
464  92 RTN
465  92 RTN
466  92 RTN
467  92 RTN
468  92 RTN
469  92 RTN
470  92 RTN
471  92 RTN
472  92 RTN
473  92 RTN
474  92 RTN
475  92 RTN
476  92 RTN
477  92 RTN
```

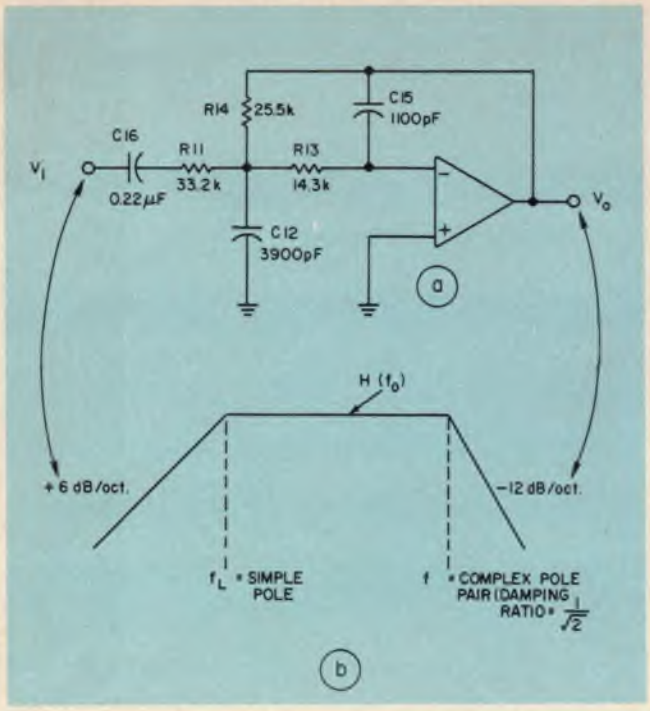
Table 2. Bandpass filter calculator operations

Operator instructions:

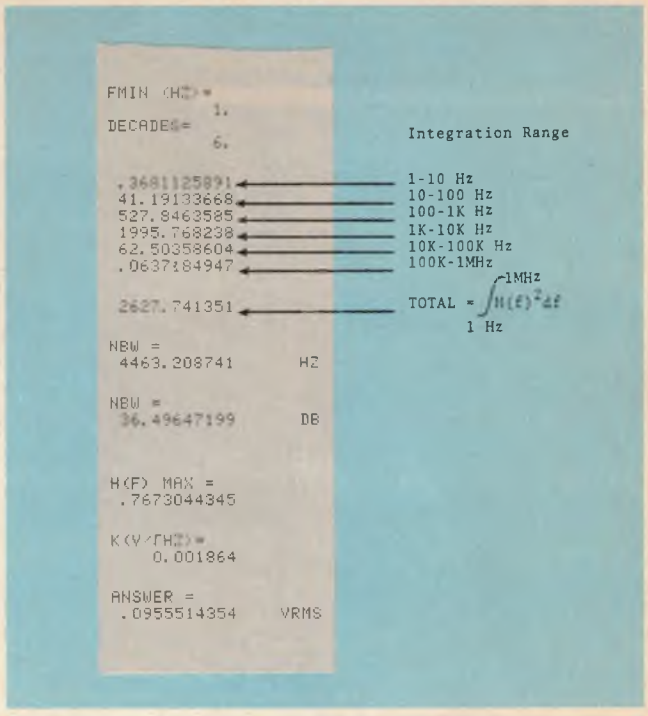
Step	Procedure	Enter	Press	Display
1	Partition the calculator	3	OP 17	719.29
2	Enter program banks 1,2,3, and 4			
3	Initialize the program		E′	2235133000
4	Define the transfer function squared (i.e., (3) squared)			
	(a) store G in R_{17}	.7680	STO 17	.7680
	(b) store f_L in R_{18}	21.79	STO 18	21.79
	(c) store f_H in R_{19}	4024	STO 19	4024
	(d) let $R_{20} = f_i$ $R_{21} = f_i/f_L$ $R_{22} = f_i/f_H$ (Note: These are temporary registers, where f_i = value of f currently in the display register.)			
			GTO A′LRN	461 92
	(e) Enter the information in routine below to calculate			
	(f) $[H(f_i)]^2$.		LRN	0.
5	Enter f_{min} = 1 Hz	1	A	1
6*	Enter # decades	6	B	2627.741351
7a*	Calculate NBW (Hz)		D	4463.208741
7b	Calculate NBW (dB)		R/S	36.49647199
8	Display $H(f_o)$		E	.7673044345
9	Enter $K = \frac{1.864 \times 10^{-3}\ V_{rms}}{\sqrt{Hz}}$	.001864	C	.0955514354

*allow about six minutes calculating time.

```
459  76 LBL
460  16 A'
461  42 STO
462  20  20
463  53  (
464  24 CE
465  55  ÷
466  43 RCL
467  18  18
468  54  )
469  42 STO
470  21  21
471  53  (
472  43 RCL
473  20  20
474  55  ÷
475  43 RCL
476  19  19
477  54  )
478  42 STO
479  22  22
480  53  (
481  53  (
482  43 RCL
483  17  17
484  65  ×
485  43 RCL
486  21  21
487  54  )
488  55  ÷
489  53  (
490  01  1
491  85  +
492  43 RCL
493  21  21
494  33 X²
495  54  )
496  34 FX
497  55  ÷
498  53  (
499  53  (
500  01  1
501  75  -
502  43 RCL
503  22  22
504  33 X²
505  54  )
506  33 X²
507  85  +
508  02  2
509  65  ×
510  43 RCL
511  22  22
512  33 X²
513  54  )
514  34 FX
515  54  )
516  33 X²
517  92 RTN
```



2. **The bandpass filter** (a) transfer function is governed by a simple pole at f_L and a complex pole-pair at f_H (b).



3. **Solutions for the filter circuit** list NBW in Hz and dB relative to 1 Hz. Also the rms-output voltage is listed.

Now see what happens when you combine Eqs. 1 and 2:

$$V_{eq} = K \times H(f_0) \times \sqrt{NBW}$$

This equation further explains equivalent noise bandwidth in another light: The rms output due to input noise equals that for an ideal-bandpass system of gain $H(f_0)$ and bandwidth NBW (Fig. 1).

Start calculating

You can get the values that you need from Eqs. 1 and 2 using Texas Instruments' TI-59 programmable calculator and PC-100A printer. Table 1 lists the program and user instructions. This program requires Integration Routine ML-09 in TI's 58/59 Master Library Module (1977).

Here are the program inputs:

- H(f).
- f_{min}, the low-frequency integration limit.
- The integration range in frequency decades (which also defines the upper-frequency of integration).
- K.

Here are the program outputs:

- NBW (in Hz).
- NBW (in dB referenced to 1 Hz).
- $H(f_0)$.
- V_{rms}.

Trying a sample calculation for the bandpass filter in Fig. 2a, with the transfer function shown in Fig. 2b, find noise bandwidth in Hz and dB, and the output for a broadband-noise input of $K = 1.864 \times 10^{-3} V_{rms}/\sqrt{Hz}$.

To solve the problem, use the following expression for the transfer function:

$$\frac{V_o}{V_i}(jf) = H(jf)$$

$$= \frac{jG\left(\frac{f}{f_L}\right)}{\left(1 + j\frac{f}{f_L}\right)\left[1 - \left(\frac{f}{f_H}\right)^2 + j\sqrt{2\left(\frac{f}{f_H}\right)}\right]},$$

which leads to

$$|H(jf)| = H(f)$$

$$= \frac{G\left(\frac{f}{f_L}\right)}{\sqrt{1 + \left(\frac{f}{f_L}\right)^2}\sqrt{\left[1 - \left(\frac{f}{f_H}\right)^2\right]^2 + 2\left(\frac{f}{f_H}\right)^2}},$$

where

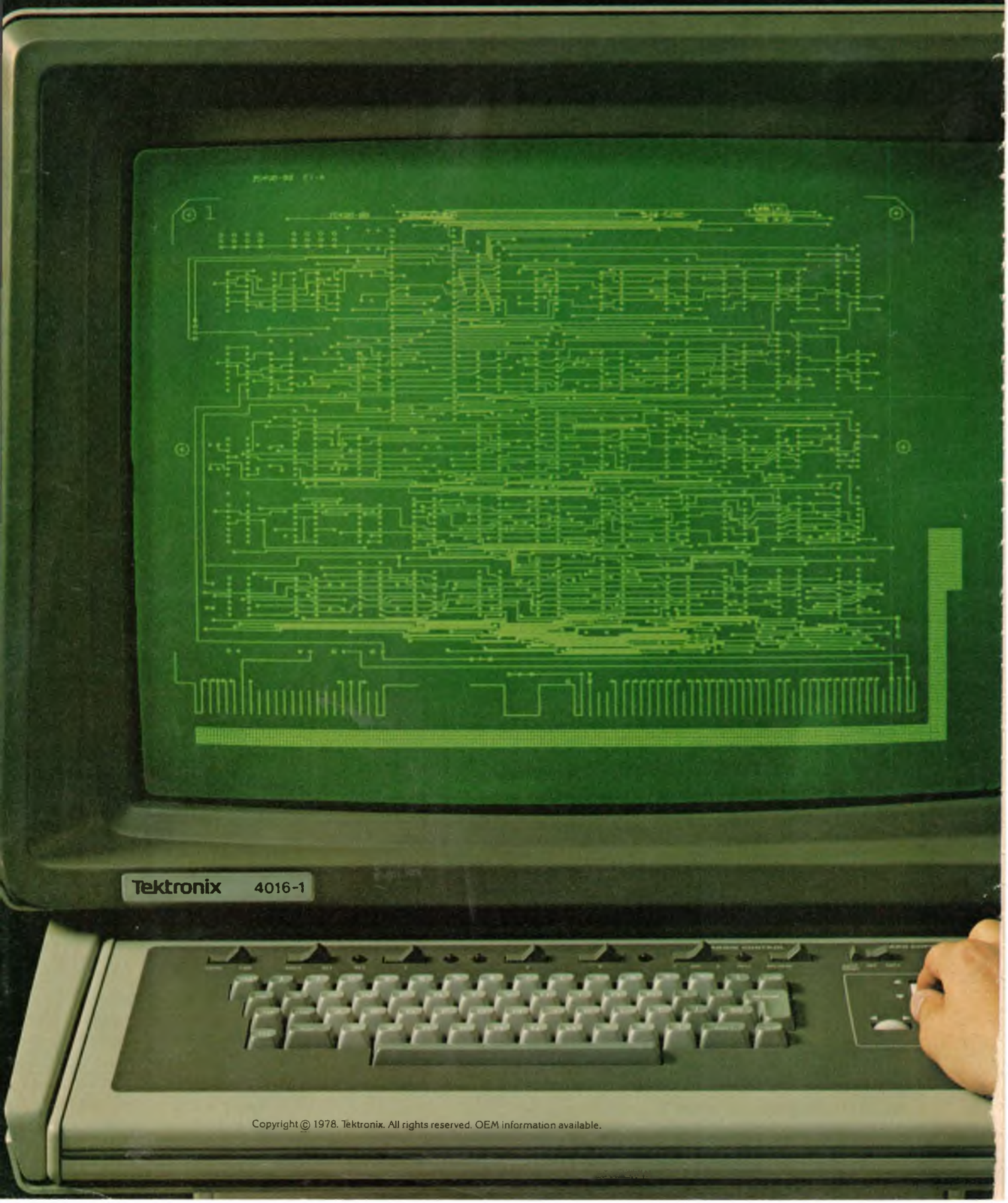
$$G = R_{14}/R_{11}$$

$$f_L = 1/2\pi R_{11}C_{16}$$

$$f_H = 1/2\pi\sqrt{R_{13}R_{14}C_{12}C_{15}}$$

These intermediate results are incorporated in Table 2. So, to calculate the noise parameters of the bandpass filter, follow the step-by-step procedure in the table. Fig. 3 shows the output of the sample program. It shows that the frequency decades from 1 to 10 Hz and 100 kHz to 1 MHz contribute only slightly to the total rms output voltage.■■

From the graphics leader



New Home Computer That Can Emulate Others Threatens to Shake Up the Industry

By Richard A. Shaffer
Staff Reporter of The Wall Street Journal

The rapidly growing personal-computer business appears headed in a new direction: Machines made by one company soon may be able to emulate those made by any other.

Such a development probably would cut sharply the profitability of the computers themselves, forcing manufacturers to seek their margins in software, the instruction programs that enable the machines to keep books, print paychecks and play games.

Many people expected the change to come in about a year, when new Japanese equipment would emulate International Business Machines Corp.'s personal computer. Instead, a U.S. company seems to be taking the first step.

Commodore International Ltd., Norristown, Pa., plans to make a personal computer that can emulate those of Apple Computer Inc., Tandy Corp., IBM and others but that would sell for a much lower price—less than $1,000. (Competitors' models sell for two to four times as much.)

Universal-Machine Concept

Aided by one of several special circuits plugged into its back, the Commodore machine will be able to read and operate from programs recorded on magnetic disks for Apple, Tandy, IBM or other computers without modification, the company says. The Commodore machine thus would have immediate access to the largest libraries of financial, text-editing and business programs for personal computers without the need for expensive development on Commodore's part.

"Commodore seems to be moving toward the universal-machine concept, which we all expected the Japanese to do first," says Ulric Weil, who follows the computer industry for Morgan Stanley & Co.

"If Commodore does what it says it will," predicts Mr. Weil, "the hardware side of the personal-computer market will take on a commodity aspect." By that, he means the machines themselves will be comparable in capability and highly competitive in price.

Shipments of the new Commodore machine are scheduled to begin in September, the company says, and the product will be shown for the first time this spring. Commodore won't say where it will introduce the machine, but industry people expect it to appear at a week-long international trade fair that begins April 21 in Hanover, West Germany.

"This is a very important product for us," says Jack Tramiel, Commodore vice chairman and chief executive, who discussed the new computer in Las Vegas Friday during the Winter Consumer Electronics Show.

Rumors that Commodore had developed an inexpensive substitute for Apple computers, known as an emulator, started circulating at the trade show Thursday when Commodore displayed a new computer, the Model 64. Apple stock dropped nearly $2 a share in over-the-counter trading that day.

The Commodore 64 isn't an Apple emulator, but it does appear to match the performance of the Apple II computer and it will retail for $595. A comparable Apple II retails for $1,650. Sales of the Model 64 are supposed to begin this spring.

Commodore International Limited

"We're the American Japanese," says Commodore's chief executive. "We don't want to invent anything; we just want to make sure we have the best."

The microprocessor inside the Model 64, known as a 6510, is an improved version of the one inside the Apple II, called a 6502. Many Apple programs will run on the Commodore machine if entered from the keyboard.

But Commodore says it hasn't any plans to enable the Model 64 to use all Apple II software without modification or to read recorded Apple programs. Charles Winterble, the company's chief engineer, says such an adaptation could be accomplished at "negligible" manufacturing cost.

Commodore says it does plan to offer a plug-in circuit that will give the Model 64 access to programs written for computers that use Z-80 microprocessors and the so-called CP/M operating system. (An operating system is an underlying program that does housekeeping chores for a computer.) Observers at the Las Vegas trade show generally regarded Commodore's planned use of the Z-80 circuit as an effort by the company to capture some of the market for Tandy's Radio Shack line of personal computers.

The Commodore emulator scheduled to become available later this year also will rely on the 6510 microprocessor. Through a slot in its back, the machine will be able to accept other microprocessors, such as the Intel Corp. 8088 used in the IBM personal computer, Commodore says.

The Commodore emulator will be offered in two versions, one with color video display and the other with black-and-white display. Memories of each machine will be able to store and retrieve between 128,000 and 256,000 characters of information.

Some personal-computer industry experts doubt that Commodore can carry out its plans to market emulators. Steven P. Jobs, Apple's chairman and one of its founders, says he isn't worried by Commodore's strategy.

"I think the Apple II has a chance of becoming a commodity product," Mr. Jobs says. "Sooner or later, someone will figure out a less expensive way to build a computer that will run Apple programs. But I'm sure we'll still manage to compete, in the same way that Sony still manages to make a profit even though other companies make turntables that will play the same records that Sony turntables will."

As for the proposed Commodore emulators, Mr. Jobs says he questions whether such products could be made without violating Apple patents.

"I take all competition seriously," Mr. Jobs says, "but in this case, I have to force myself. I'll believe it when I see it."

'The American Japanese'

Commodore has been discounted before. Its first entry into the personal-computer market, a machine known as PET (for Personal Electronic Transactor), was widely regarded as a computer with few virtues and several shortcomings. But the PET became popular, and its success is a principal factor in the steady rise of Commodore's earnings from 16 cents a share in 1977 to $2.46 a share in the fiscal year ended last June.

Many of Commodore's computers are sold as consumer products. Although the emulators probably would sell mostly to business and professional customers, Mr. Tramiel says there is a possibility that the new machines could cut into sales of Commodore's existing product line.

"We'd prefer to compete with ourselves than to have someone else compete with us," he says. "We're the American Japanese. We don't want to invent anything; we just want to make sure we have the best."

Things fell into place last week for Lexicon

By TIM SMART
Herald Business Writer

The stock of Lexicon Corp., the Fort Lauderdale-based manufacturer of portable terminals and computer hook-ups, was among the most active stocks on the over-the-counter market last week.

More than 186,000 shares traded Monday, as the stock gained 5/16 to 2½ bid. Trading had increased to more than 234,000 shares Tuesday and by Friday the stock was at 3-1/16 bid. That was a gain of 40 per cent for the week, one of the largest on the over-the-counter market.

The reason for this activity?

Increased awareness among investors of Lexicon's newest product, the super-lightweight, Lex-21 portable computer terminal that is small enough to fit snugly underneath an airplane seat, says Fort Lauderdale stockbroker Allan Edwards.

Announcements

Two recent announcements — that Mitel Inc. was purchasing 250 of the $1,195 terminals for use by its executives, and that Western Union had approved the use of the Lex 21 for its electronic mail system — have sparked investor interest in the small company, Edwards said.

"I feel that the company is really proving itself with its product," said Edwards of Oppenheimer & Co.'s Fort Lauderdale office.

"I feel if they can take the ball, you're going to see a very solid earnings picture for the company," he said.

Things haven't always looked this good for the five-year-old company, which has manufacturing facilities in Miami Lakes, but maintains corporate headquarters in northwest Fort Lauderdale.

> The year ending Aug. 31 was the first in which Lexicon made any profit.

Lexicon breezed to a remarkable start with its first product, a hand-held translator. But success proved catastrophic to the poorly-capitalized company as cash-flush competitors rushed into the market. Lexicon had orders but lacked the dollars to expand production. After three losing years, Lexicon was forced to sell the rights to its translator to a German-based computer company.

Company founder Anastasios Kyriakides, who invented the translator, relinquished the presidency of Lexicon in 1979 to Michael Levy, an engineer recruited from Racal-Milgo, another Fort Lauderdale high-technology company. Levy quickly began applying his engineering background to the development of new products: a computer-telephone link-up and a portable computer terminal.

The year ending Aug. 31 represented the first in which Lexicon made any profit, albeit only $36,245 on revenues of $1.16 million. Figures for the quarter which ended Nov. 30 are not yet available.

Referring to the Mitel Lex-21 purchase, Levy said "It's not so substantial from a dollar standpoint as so much from the creditability standpoint. Mitel is a leader in technology."

The potential of the lightweight Lex-21 computer terrminal was one reason fo heavy trading in Lexicon stock.

Lexicon Corp.

... in profile

HEADQUARTERS	Fort Lauderdale
TOP OFFICER	Michael Levy
1981 REVENUES	$1.1 million
1981 PROFIT	$36,245
ASSETS	$2.7 million

OPERATIONS: The company's production facilities in Miami Lakes produce modems — devices that allow computers to talk to each other over telephone lines — and portable computer terminals. The company is also involved in work for the government, including development and production of 'a classified microcomputer product.'

Mitel trades 'telephone tag' for electronic mail

By PATRICIA BELLEW
Herald Business Writer

Mitel Corp., a company with a penchant for bedecking its top brass with the latest in high-tech gear, was one of the first in line for the Lexicon Corp. "electronic mail" system.

"We got tired of playing telephone tag with our executives," says Ted Nanz, a vice president of the communications equipment manufacturer. "It's such a tiresome game trying to track down a traveling executive, leaving a trail of telephone messages all over the place."

Mitel Corp. recently put in an order for 250 of the Lexicon "electronic mail" systems — at about $1,000 each — and intends to distribute them to top Mitel managers

Briefly, this is how the system works: Important messages are stored in computerized "mail boxes" at corporate headquarters. Traveling executives carry a five-pound mini-computer terminal — so compact it fits in one half of an attache case — and can plug into their personal mail box back at the office by telephone. Each executive has a personal code word that electronically opens his mail box. The executives' mini-computer, once plugged into a hotel or convention-floor telephone, reads and prints out his messages.

"The beauty of the system is that it works 24 hours a day," says Nanz. "You don't have to worry about time zone your secretary being out to lunch."

Mitel, a manufacturer of computer telephone systems with U.S. headquar in Boca Raton, typically gives its top m agers "several thousand dollars worth other electronic equipment, ranging f computer equipment in each executi office to a personal mini-computer "smart telephone set" that remembers portant telephone numbers.

"We are in the high-tech busine says Nanz. "We want all our executive have hands-on experience with the 'n in communications equi-"

-MSG M#= 50091 FR=SKOT TO=ALCC SENT=11/25/81 11:40 AM
R#=082 ST=C DIV=039 CC=0117 BY=SKOT AT=11/25/81 11:40 AM
470900 TO 171624
HOPKINS & CARLEY
525 UNIVERSITY AVENUE, SUITE 1320
PALO ALTO, CALIFORNIA 94301

ATTENTION: FRANCIS M. SMALL, JR.

COPY: TOM COPELAND RFK
LEO HEITING MELS
C. B. WILSON ALCC
MIKE SILEO BUSS

FROM: BRADLEY TAYLOR BUSL
TEXAS INSTRUMENTS

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11/25/81
REV A

PRINCIPALS OF AGREEMENT

THE FOLLOWING TERMS COMPRISE AN AGREEMENT TO BE INCORPORATED IN A MORE FORMAL AGREEMENT HAVING AN EFFECTIVE DATE OF DECEMBER 24, 1981, AND TO BE PREPARED AFTER EXECUTION OF THIS PRINCIPALS OF AGREEMENT.

1. PARTIES: TEXAS INSTRUMENTS INCORPORATED (TI) AND EXATRON CORPORATION (EXATRON) AND MAJORITY-OWNED SUBSIDIARIES OF EACH.

2. LICENSED SUBJECT MATTER: APPARATUS, PROCESS, KNOW-HOW AND THE LIKE THAT TI DEEMS TO BE REQUIRED TO MANUFACTURE A DIRECT DRIVE MAGNETIC WAFER TRANSPORT MECHANISM AND COMPATIBLE MAGNETIC TAPE WAFER (HEREINAFTER "LICENSED PRODUCT").

3. GRANT: EXATRON WILL GRANT TO TI A LICENSE TO USE EXATRON TECHNOLOGY RELATED TO THE MANUFACTURE, USE AND SALE OF THE LICENSED PRODUCT, WITHOUT RESTRICTION. THIS LICENSE SHALL BE EXCLUSIVE TO TI UNTIL DECEMBER 31, 1982 AND PERPETUALLY NONEXCLUSIVE THEREAFTER.

4. DISCLOSURE: EXATRON WILL DISCLOSE TO AND DELIVER AS SOON AS POSSIBLE FOLLOWING EXECUTION OF THIS PRINCIPALS OF AGREEMENT ALL ESSENTIAL TECHNOLOGY AND KNOW-HOW REQUIRED TO MANUFACTURE THE LICENSED PRODUCT.

5. TECHNICAL DATA: EXATRON WILL ITEMIZE IN AN APPENDIX TO THE FORMAL AGREEMENT ALL DRAWINGS, SCHEMATICS, BILLS OF MATERIALS, PARTS LIST, LIST OF SUBCONTRACTS, TEST PROCEDURES, OPERATING MANUAL AND SPECIFICATIONS THAT TI DEEMS TO BE REQUIRED TO MANUFACTURE THE LICENSED PRODUCT

6. FUTURE DEVELOPMENTS: EXATRON WILL MAKE AVAILABLE TO TI ALL FUTURE ENHANCEMENTS AND IMPROVEMENTS RELATING TO LICENSED SUBJECT MATTER AT NO ADDITIONAL COST TO TI UNTIL DECEMBER 31, 1984. SUCH DISCLOSURES AS WELL AS THE INITIAL DISCLOSURE BY EXATRON WILL BE PROPRIETARY TO EXATRON AND WILL NOT BE DISCLOSED BY TI TO THIRD PARTIES WITHOUT EXATRON'S WRITTEN PERMISSION FOR A PERIOD OF THREE (3) YEARS FROM THE DATE OF RECEIPT THEREOF.

7. TECHNICAL ASSISTANCE: EXATRON WILL MAKE AVAILABLE AT TI'S REQUEST, TECHNICAL ASSISTANCE UP TO 200 MAN-HOURS THROUGH VISITS BY EXATRON CONSULTANT, MR. RYE SMITH TO TI'S FACILITIES TO FACILITATE TI'S UNDERSTANDING AND USE OF THE LICENSED SUBJECT MATTER. IF ADDITIONAL VISITS SHOULD BE REQUIRED, EXATRON SHALL BE COMPENSATED AT $500/MAN-DAY PLUS EXPENSES. ONE MAN-DAY SHALL BE THE MINIMUM PER VISIT.

8. PAYMENT: TI AGREES TO PAY EXATRON AN INITIAL NON-REFUNDABLE, SINGLE, LUMP-SUM PAYMENT OF $33,000 UPON DELIVERY OF ALL THE TECHNICAL DATA, AND $34,000 UPON RELEASE BY TI OF THE MUTUALLY AGREED UPON DRAWINGS TO TI'S MOLD TOOLING VENDOR, AND $33,000 UPON COMPLETION OF THE MOLD TOOLING AND ACCEPTANCE BY TI OF THE FIRST ARTICLES PRODUCED THEREFROM, AND $100,000 UPON FIRST SALE BY TI OF A LICENSED PRODUCT. TI SHALL HAVE NO OBLIGATION TO PAY ANY SUCH SUMS UNLESS THE MILESTONES TRIGGERING PAYMENT ACTUALLY OCCUR.

9. PATENTS: EXATRON HEREBY GRANTS TO TI A ROYALTY-FREE IMMUNITY FROM INFRINGEMENT OF ANY PATENTS ANYWHERE IN THE WORLD THEY OWN AND HAVE THE RIGHT TO SO GRANT, THAT RELATE TO THE LICENSED SUBJECT MATTER AND ARE ISSUED PRIOR TO DECEMBER 24, 1984, THE EXPIRATION DATE OF THIS AGREEMENT. EXATRON AGREES TO INDEMNIFY TI FROM CLAIMS OF PATENT INFRINGEMENT OR VIOLATIONS OF PROPRIETARY RIGHTS OF A THIRD PARTY.

10. CONTINGENT ROYALTIES: IF TI SELLS THE TRANSPORT MECHANISM AS A COMPONENT ON A STAND ALONE BASIS, TI SHALL PAY ROYALTIES TO EXATRON OF FIVE PERCENT (5%) OF TI'S ADJUSTED NET SALES FOR EACH SUCH ITEM SOLD BY TI FOR FOUR (4) YEARS FROM THE DATE OF INITIAL SALE THEREOF BY TI. AFTER SUCH FOUR (4) YEARS THE LICENSE SHALL BE PAID-UP AND ROYALTY-FREE.

11. TERM: THE TERM OF THIS AGREEMENT SHALL BE THREE (3) YEARS, PROVIDED, HOWEVER, THAT THE IMMUNITY FROM INFRINGEMENT GRANTED HEREUNDER SHALL EXTEND FOR THE LIVES OF ALL PATENTS, AND THE LICENSE TO USE THE TECHNICAL DATA SHALL SURVIVE TERMINATION OF THIS AGREEMENT; LICENSES GRANTED HEREUNDER SHALL SURVIVE TERMINATION ON A FULLY PAID-UP BASIS IF ALL PAYMENTS HAVE BEEN MADE IN ACCORDANCE WITH PARAGRAPH 8.

12. PUBLICITY: NEITHER PARTY HERETO SHALL, WITHOUT SECURING WRITTEN CONSENT OF THE OTHER PARTY, PUBLICLY ANNOUNCE THE EXISTENCE OF THIS AGREEMENT, OR ADVERTISE OR RELEASE ANY PUBLICITY IN REGARD THERETO. THIS PROVISION SHALL SURVIVE EXPIRATION OR TERMINATION OF THIS AGREEMENT.

13. VALIDITY: THIS AGREEMENT SHALL NOT BIND EITHER PARTY HERETO UNTIL DULY SIGNED BY EACH PARTY HERETO.

AGREED TO:

EXATRON CORPORATION
INCORPORATED

TEXAS INSTRUMENTS INCORPORATED

BY
ROBERT L. HOWELL
TITLE CHAIRMAN

DATE

BY
WILLIAM N. SICK
TITLE VICE PRESIDENT

DATE

REGARDS,

TEXAS INSTRUMENTS INCORPORATED
BRADLEY TAYLOR, MANAGER
CONSUMER CONTRACT SERVICES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 10508 • LUBBOCK, TEXAS 79408
U.S. Consumer Products Group

Mail Station 5829

#1686

October 26, 1981

Robert L. Howell, Chairman
Exatron Corporation
181 Commercial Street
Sunnyvale, California 94086

Subject: Proprietary Disclosures

Gentlemen:

Exatron and TI are engaging in discussions in connection with the Exatron direct drive magnetic wafer transport mechanism and magnetic tape wafer for the purpose of possible purchase of products and/or techical know how by TI from Exatron. In the course of these discussions Exatron made a verbal and visual presentation of information on July 30, 1981 to representatives of TI of a prototype transport mechanism employing a wafer with a sliding cover. Exatron now believes information regarding the wafer with a sliding cover to be proprietary.

Exatron and TI agree that for a period of 2 years from the date of this Agreement, TI shall not disclose any information regarding the wafer with a sliding cover it received in Exatron's verbal and visual presentation presented on July 30, 1981, to any other person, firm, or corporation or use it for its own benefit, except for evaluation of possible purchase of Exatron products and/or technical know how, and shall use the same degree of care to avoid publication or use of such information as TI employs with respect to its own information of like importance which it does not desire to have published or disseminated.

Exatron and TI agree that information shall not be deemed proprietary to Exatron and TI shall have no obligation with respect to any such information which:

(i) was already known to TI as of July 30, 1981; or

(ii) is or falls into the public domain through no wrongful act of TI; or

(iii) is rightfully received from a third party without restriction and without breach of this Agreement; or

(iv) is independently developed by TI without breach of this Agreement; or

(v) is furnished to a third party by Exatron without a similar restriction on the third party's rights; or

(vi) is approved for release by the written authorization of Exatron; or

(vii) is disclosed pursuant to the requirement of a government agency or operation of law.

TI shall not be liable for (1) inadvertent use, publication or dissemination of proprietary information received hereunder provided that (a) it uses the same degree of care in safeguarding such information as it used for its own information of like importance, and (b) upon discovery of such it shall endeavor to prevent any further inadvertent use, publication or dissemination and (2) unauthorized use, publication or dissemination of proprietary information received hereunder by persons who are or have been in its employ unless it fails to safeguard such information with the same degree of care as it uses for its own proprietary information of like importance, and (3) any use, publication or dissemination, if any, of proprietary information received hereunder between July 30, 1981 and the date of execution of this Agreement by Exatron.

Nothing contained in this Agreement shall be construed as granting, conferring, or implying any rights by license or otherwise.

Except as agreed to above, during discussions and/or correspondence between representatives of Exatron and TI in connection with the Exatron direct drive magnetic wafer transport mechanism and magnetic tape wafer, it is our understanding that neither party has disclosed, intends to disclose, nor does it wish to receive any information which may be considered confidential or proprietary. Accordingly, except with respect to rights under valid patents and federal statutory copyrights, no obligation of any kind is assumed by or to be implied against either party by virtue of our discussions and/or correspondence with respect to whatever information is or has been exchanged and each party will be free to use such information without limitation. Moreover, our discussions and/or correspondence will not serve to impair the right of either party to make, procure and market products or services now or in the future which may be competitive with those offered by the other, nor require either party to disclose any planning information to the other.

Unless otherwise agreed to in writing by the parties, the foregoing understanding shall apply to any subsequent meetings or communications between us relating to the same subject matter.

Should a party hereto desire to transmit proprietary or confidential information to the other, then that party shall (1) notify the other party before any proprietary or confidential information is transmitted and (2) obtain the other party's written agreement concerning any obligations which will arise when such information is transmitted.

We would appreciate your signing and returning to us, a copy of this letter denoting your concurrence with the foregoing provisions.

Very truly yours,

TEXAS INSTRUMENTS INCORPORATED

William N. Sick
Vice President

WNS/tlr

AGREED TO:

EXATRON CORPORATION

BY: _____
Robert L. Howell,

TITLE: Chairman

DATE: 28 Oct 81

C. B. Wilson

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LICENSE AGREEMENT

This License Agreement is made as of the 16th day of December, 1981, by and between EXATRON CORPORATION, a California Corporation with offices at 181 Commercial Street, Sunnyvale, California 94086 (herein "EXATRON"), and TEXAS INSTRUMENTS INCORPORATED, a Texas corporation acting by and through its U.S. Consumer Products Group with offices at 2301 N. University, Lubbock, Texas 79408 which shall have an EFFECTIVE DATE of December 16, 1981.

RECITALS

A. EXATRON represents and warrants that it has developed and is the sole owner of all rights, title and interest in and to U.S. Letters patents 3846831, 4078194, 4013239, 4107752, and 4127878, and derivative foreign patents and certain EXATRON DATA (herein defined) which relate to magnetic tape transport mechanisms and compatible magnetic continous loop tape cassettes (hereafter later defined as "Magnetic Tape Transport System"), and further represents that it possesses certain Know-How and manufacturing technology and data relating to the design and manufacture of such Magnetic Tape Transport System; and

B. TI desires to obtain from EXATRON a license to manufacture, have manufactured, use and sell products covered by any one or more of such EXATRON PATENTS (herein defined), and to utilize EXATRON DATA in the design and manufacture of its products; and

C. The parties hereto further desire to develop and establish as an INDUSTRY STANDARD (as defined herein) the MAGNETIC TAPE TRANSPORT SYSTEM. To successfully achieve this mutual desire, the parties agree that a strategic "second sourcing" program is necessary to achieve industry acceptance of the MAGNETIC TAPE TRANSPORT SYSTEM.

NOW, THEREFORE, in consideration of the foregoing and the mutual promises hereinafter made, the parties hereto agree as follows:

PART I: DEFINITIONS

1.01 "TI" AND "EXATRON"

Texas Instruments Incorporated and Exatron Corporation, respectively, and any corporation which they respectively control through the direct or indirect ownership of more than fifty percent (50%) of its stock entitled to vote for the election of members of the Board of Directors (other than preferred stock entitled to vote upon failure of the corporation to pay dividends).

1.02 "EXATRON PATENTS"

All patents, utility models and design patents (including but not limited to those listed in Exhibit A) and applications therefor

throughout the world relating to any MAGNETIC TAPE TRANSPORT SYSTEM issued or issuing on patent applications filed prior to December 31, 1986, or if filed subsequent thereto, but receiving, or entitled to receive, the benefit of a filing date anywhere in the world prior to December 31, 1986, and includes all patents or applications for patent having an issue or filing date prior to December 31, 1986 which EXATRON now has or hereafter acquires the right to sell, transfer or grant rights thereunder to TI relating to any MAGNETIC TAPE TRANSPORT SYSTEM.

1.03 "EXATRON DATA"

Techniques, methods, drawings, designs, skills and concepts, and all documentation in the possession of EXATRON, or otherwise reasonably available to EXATRON, whether patented or not, which may be reasonably needed or required to develop, design, manufacture and/or test the MAGNETIC TAPE TRANSPORT SYSTEM, or any component thereof, and shall include, without limitation, manufacturing drawings, schematics, bills of materials, parts lists, lists of subcontractors or vendors, lists of existing purchase agreements, test procedures and data, jig specifications, special tooling specifications, operating manuals and any other written or recorded data reasonably needed or required to develop, design, manufacture and/or test the MAGNETIC TAPE TRANSPORT SYSTEM, or any component thereof.

1.04 "LICENSED PRODUCTS"

Any and all products made, made for, used, or sold by TI which are covered by or relate to EXATRON PATENTS or EXATRON DATA.

1.05 "MAGNETIC TAPE TRANSPORT SYSTEM"

A product utilizing (1) a magnetic tape transport mechanism, and/or (2) a continuous loop tape cassette to store and dispense magnetic recording tape, together with all enhancements and improvements thereto as shall hereafter be made or acquired by EXATRON through December 31, 1986.

1.06 "INDUSTRY STANDARD"

Where the MAGNETIC TAPE TRANSPORT SYSTEM is generally recognized in the small computer industry as a standard way to load and store programs in small computers.

PART II: LICENSE; SCOPE OF PERFORMANCE

2.01 GRANT OF LICENSE

For the consideration hereinafter provided, EXATRON hereby grants to TI, an irrevocable, worldwide, license, under EXATRON PATENTS and EXATRON DATA, (together with the right of sublicense as provided in Section 2.02 hereof) to manufacture, have manufactured, use, sell or otherwise dispose of LICENSED PRODUCTS. The license granted herein shall be exclusive to TI until June 30, 1983, and nonexclusive thereafter, and shall become fully paid-up upon payment of the monies

required under Paragraph 2.03. EXATRON agrees not to disclose any EXATRON DATA to any person, real or legal, during such exclusivity period (except to EXATRON suppliers who assume the obligations set forth in Part III hereof).

2.02 SUBLICENSE

TI shall be entitled to sublicense others to manufacture the LICENSED PRODUCTS but only as to products, or components thereof, manufactured for the account of TI, and then subject to the provisions of Section 3.02 hereof. TI may disclose EXATRON DATA to such sublicensees provided the sublicensee assumes the obligations set forth in Part III hereof.

2.03 RESERVATION OF RIGHTS

Notwithstanding the foregoing, nothing contained herein shall be deemed to preclude EXATRON from selling or offering for sale EXATRON's Mass Storage System known as the Stringy Floppy™ as the same is configured, produced and offered for sale on the EFFECTIVE DATE hereof, or any other product which is covered by EXATRON PATENTS or which utilizes EXATRON DATA in the design, manufacture or testing thereof.

2.04 LICENSE FEE

As consideration for the license granted herein, TI agrees to pay to EXATRON an initial non-refundable, single, lump-sum payment of $33,000 following delivery of all EXATRON DATA; and $34,000 following release by TI of the mutually agreed upon drawings and specifications for the transport plastic housing to the TI mold tooling vendor; and $33,000 following completion of the mold tooling and acceptance by TI of the first articles produced therefrom; and $100,000 following the first sale by TI of a LICENSED PRODUCT. TI shall have no obligation to pay any such sums unless milestones triggering payment actually occur. Payments shall be due and payable thirty (30) days following receipt of invoice.

2.05 DELIVERY OF EXATRON DATA

Immediately following the execution of this Agreement, EXATRON shall deliver to TI, one legible, reproducible set of the EXATRON DATA. Thereafter, and without further expense to TI, EXATRON shall provide to TI in legible and reproducible form, one set of all updates and changes to the EXATRON DATA reflecting enhancements and improvements made to the MAGNETIC TAPE TRANSPORT SYSTEM by EXATRON up to December 31, 1986. If Exatron considers such enhancements and improvements to be Confidential information and does not believe the June 30, 1985 protection period specified in Paragraph 3.02 affords Exatron sufficient protection then the parties shall negotiate in good faith an additional period for protection of such information reflecting the involved enhancements and improvements.

2.06 DISCLOSURE

In addition to the delivery of EXATRON DATA, EXATRON will disclose to TI all of its Know-How relating to the MAGNETIC TAPE TRANSPORT SYSTEM. The disclosure shall include thorough discussions, demonstrations and review of the manufacturing process steps and EXATRON DATA.

2.07 ADDITIONAL ASSISTANCE

Immediately following the execution of this Agreement, upon TI's request, EXATRON will provide during 1982, tooling design and other technical assistance to TI in respect of any tooling, manufacture process or method related to the manufacturing, without limitation, of the MAGNETIC TAPE TRANSPORT SYSTEM, and any other present or future inventions, patents or data of EXATRON related to such manufacturing. Such assistance will be given by K. Rey Smith, Consultant, or similarly qualified personnel, in the form of at least 200 man-hours of consultation at facilities designated by TI. Such consultation may not exceed three (3) man-days in any week (excluding travel time) or two (2) weeks in any four (4) week period. Travel expenses (including coach air fare) for travel outside a 500 mile radius of Los Altos, California and which has been previously authorized by TI, shall be paid by TI thirty (30) days following receipt of a voucher for such expenses. If additional consultation should be required following the 200 man-hours, EXATRON shall be compensated at $500/man-day plus expenses. One man-day shall be the minimum per visit. EXATRON shall also provide up to two (2) weeks of observation and instruction for TI's employees at EXATRON's facility.

2.08 SECOND SOURCING PROGRAM

Effective with the sale by TI of a MAGNETIC TAPE TRANSPORT SYSTEM for incorporation with or in a third party product, the parties shall each establish a program for the purpose of achieving acceptance of the MAGNETIC TAPE TRANSPORT SYSTEM, or components thereof, by other business entities for the purpose of establishing additional users and sources of such System, and for achieving acceptance of such System as an INDUSTRY STANDARD. To such end TI shall promote the availability of the MAGNETIC TAPE TRANSPORT SYSTEM through it, and shall stand ready to manufacture and supply, consistent with available resources, the MAGNETIC TAPE TRANSPORT SYSTEM to such other business entities. EXATRON shall, also consistent with available resources, do the same. The parties intend by these mutual commitments to establish, each for the benefit of the other, additional users and second sources for the MAGNETIC TAPE TRANSPORT SYSTEM. TI's acts in compliance with this Section 2.08 shall be deemed within the scope of the license granted to TI under Section 2.01 hereof. Nothing contained in this Section 2.08 shall be construed as granting or conferring any license whatsoever to such other business entities under any EXATRON PATENTS or EXATRON DATA except as provided in Section 2.02 hereof.

PART III: CONFIDENTIALITY: NONDISCLOSURE

3.01 CONFIDENTIALITY

EXATRON agrees to disclose to TI certain EXATRON DATA which it considers to be confidential and proprietary to EXATRON. EXATRON agrees to appropriately mark such data with a restrictive use legend, such as, "EXATRON Confidential".

3.02 RESTRICTIVE USE CONDITIONS

From the EFFECTIVE DATE hereof to June 30, 1982, TI wishes to receive EXATRON Confidential Information and agrees not to disclose such EXATRON Confidential Information given to it during such period to any person, real or legal, except as provided herein until June 30, 1985, and shall exercise the same degree of care to safeguard the confidentiality of such EXATRON Confidential information as TI would exercise in protecting the confidentiality of similar property of its own. After June 30, 1982, EXATRON agrees that all disclosures of its Confidential information shall be done in accordance with the conditions set forth in Section 3.03 hereof. The obligations of TI to avoid publication or dissemination of EXATRON Confidential Information will not apply to any information that:

(a) is already in the possession of TI; or
(b) is independently developed by TI; or
(c) is or becomes publicly available without breach of this Agreement by TI; or
(d) is rightfully received by TI from a third party not under an obligation of confidence to EXATRON with respect thereto; or
(e) is released for disclosure by EXATRON with its written consent; or
(f) is disclosed pursuant to the requirement of a government agency or operation of law provided that TI is obligated to use its best efforts to prevent disclosure under such circumstances; or
(g) is furnished to a third party by EXATRON without a similar restriction on the third party's rights; or
(h) is readily discernable from any product or service reasonably available in commerce.

TI shall not be liable for (1) inadvertent publication or dissemination of any EXATRON Confidential Information provided that (a) it uses the same degree of care in safeguarding such information as it uses for its own information of like importance, and (b) upon disclosure of such inadvertent publication or dissemination of such information it shall endeavor to prevent any further inadvertent publication or dissemination, and (2) unauthorized publication or dissemination of any EXATRON Confidential Information by persons who are or who have been in its employ, unless it fails to safeguard such information with the same degree of care as it uses for its own information of like importance. Moreover, TI shall not be liable for disclosures made to sublicensees, provided such disclosures are reasonably necessary to TI's or its sublicensees' use of EXATRON DATA

and provided further that TI shall obtain such sublicensee's written assent to hold such EXATRON Confidential Information in the manner required in this Section 3.02.

3.03 DATA CONTROL COORDINATOR

TI appoints the below identified person as its Data Control Coordinator for informing TI employees of TI's responsibilities hereunder and for the receipt, on TI's behalf, of all EXATRON Confidential information made after June 30, 1982. In the event it is necessary for EXATRON in compliance with this Agreement to disclose any of its Confidential information to TI after June 30, 1982, EXATRON agrees to notify TI's Data Control Coordinator in writing of this fact, and request written authorization to disclose such Confidential information pursuant to this Agreement. Upon receipt of such written authorization, such Confidential disclosure of EXATRON information to TI shall be subject to the conditions of this Part III. TI reserves the right to change it Data Control Coordinator by giving EXATRON in writing the name and address of its newly appointed Data Control Coordinator.

Jim Arnold
Texas Instruments Incorporated
P O Box 10508, M/S 5873
Lubbock, Texas 79408
Phone: (806) 741-2466

PART IV: PATENT INDEMNIFICATION; WARRANTY

4.01 OWNERSHIP

EXATRON represents and warrants that it is the sole owner of the EXATRON PATENTS and EXATRON DATA, and that it is free to enter into this License Agreement. EXATRON acquired its ownership of the EXATRON PATENTS through assignments which have been or are being duly recorded in the United States and in foreign governments for corresponding foreign patents, such United States and foreign patents being listed on EXHIBIT A hereto.

The parties agree that the ownership and license status of improvements, whether patentable or not, that are conceived or made by either of the parties during the term of this Agreement based on EXATRON DATA or EXATRON PATENTS shall be as follows:

TI Improvements:

TI shall own the entire right, title and interest to its improvements, but agrees to grant EXATRON, upon request, an irrevocable, worldwide, non-exclusive license to manufacture, use or sell products covered by patents on such improvements, or data related thereto, under reasonable terms and conditions.

EXATRON Improvements:

EXATRON shall own the entire right, title and interest to its improvements, and such improvements shall be deemed EXATRON PATENTS, if patentable, or EXATRON DATA, if not patentable, and shall be subject to the terms of this Agreement. With respect to patentable improvements, if EXATRON elects to file for patent protection thereon, any patent application or corresponding patent on the same shall be considered an EXATRON PATENT and be subject to the terms of this Agreement. If EXATRON elects not to file for patent protection on such patentable improvements, EXATRON agrees to disclose such patentable improvements to TI, and TI shall have the right to file for patent protection. If TI elects to file for patent protection on such patentable improvements, TI shall own the entire right, title and interest to such patentable improvements, subject to EXATRON having a paid-up, irrevocable, worldwide, non-exclusive license to manufacture, use or sell any product covered by any patent for such patentable improvements.

4.02 INDEMNIFICATION

EXATRON agrees to indemnify TI and to hold it harmless from all damages and all reasonable expenditures incurred by it as the result of any claim of patent infringement or violation of proprietary or contractual rights of a third party, asserted against TI by virtue of TI's or any sublicensee's manufacture, use or sale of LICENSED PRODUCTS provided that EXATRON or its designee is given prompt notice of any such claim against TI or any sublicensee, and the right to control and direct the investigation, preparation, defense and settlement of each claim, and further provided that TI and its sublicensees shall fully cooperate with EXATRON at EXATRON's expense in connection with the foregoing. Any modification or attempted modification of any LICENSED PRODUCT by TI or any TI sublicensee shall void this indemnity obligation if the infringement stems from such modification of the LICENSED PRODUCTS, unless EXATRON has authorized in writing such modification or attempted modification.

4.03 LIMITATION OF LIABILITY AND TIME TO SUE

Except as provided in Section 4.02 above, neither party shall be liable to the other for any direct, indirect, special, consequential or other damages arising out of TI's or any sublicensee's use of LICENSED PRODUCTS or the marketing, delivery, installation, furnishing, maintaining or supporting of the LICENSED PRODUCTS by TI. If for any reason any of the foregoing limitation of liability is voided or is not effective, TI agrees that (except as provided in Section 4.02 above or except as a result of acts of EXATRON's negligence or strict liability) EXATRON's liability for damages, if any, shall not exceed the Fee paid to EXATRON by TI under Section 2.03 hereof. No action, regardless of form, arising out of any of the transactions under this Agreement may be brought by either party more than two years after such action accrued.

PART V: GENERAL PROVISIONS

5.01 COMPONENT SOURCING

The parties hereto understand that TI needs to qualify responsible subcontractors for supplying any components it may need to manufacture its MAGNETIC TAPE TRANSPORT SYSTEM. Therefore, the parties agree to negotiate in good faith an Agreement for the purchase and sale of components, such as, continuous loop tapes and tape transport mechanisms, for use with or incorporation into a TI manufactured MAGNETIC TAPE TRANSPORT SYSTEM, which EXATRON has the manufacturing capability to supply TI at reasonable and competitive prices, for reasonable and competitive delivery schedules in compliance with TI specifications. Nothing contained in this Section 5.01 shall be construed as obligating either party to purchase or sell any of its products to the other party.

5.02 WAIVER, AMENDMENT OR MODIFICATION

The waiver, amendment or modification of any provision of this Agreement or any right, power or remedy hereunder shall not be effective unless made in writing and signed by the party by whom enforcement of such waiver, amendment or modification is sought. The terms of this Agreement shall not be amended or changed by the terms of any purchase order or acknowledgment for LICENSED PRODUCTS from either party even though either party may have accepted or signed such documents. No failure or delay by either party in exercising any right, power or remedy with respect to any of its rights hereunder shall operate as a waiver thereof.

5.03 NOTICE

Any notice or other communication required or permitted hereunder shall be given in writing to the other party at the address stated herein, or at such other address as shall be given by either party to the other in writing. Such notice shall be deemed to have been or made when delivered in hand or, mailed, first class postage prepaid addressed to the last known address of recipient.

5.04 ENTIRE AGREEMENT

This Agreement constitutes the entire agreement between the parties in connection with the subject matter hereof, and supersedes all prior and contemporaneous agreements, understandings, negotiations and discussions, whether oral or written, between the parties, and there are no warranties, representations or agreements between the parties in connection with the subject matter hereof except as specifically set forth and referred to herein.

5.05 SUCCESSORS AND ASSIGNS

All the terms and provisions of this Agreement shall be binding upon and inure to the benefit of the parties hereto, and their successors

and assigns and legal representatives, except that neither party may assign this Agreement nor any right granted hereunder, in whole or in part, without the other party's prior written consent.

5.06 GOVERNING LAW; SEVERABILITY

The validity, construction and performance of this Agreement and the legal relations between the parties to this Agreement shall be governed by and construed in accordance with the laws of the State of California. If any provision of this Agreement or the application of any such provision shall be held by a tribunal of competent jurisdiction to be contrary to law, the remaining provisions of this Agreement shall remain in full force and effect.

5.07 TAXES

In addition to the License Fee specified in this Agreement, TI shall pay (or reimburse EXATRON, where appropriate) for any sales or use taxes which may be imposed upon EXATRON by reason of the licensing to TI of the rights contained herein.

5.08 PUBLICITY; RELEASE OF INFORMATION

Neither party hereto shall, without securing written consent of the other party, publicly announce the existence of this Agreement, or advertise or release any publicity in regard thereto. Such consent shall not be unreasonably withheld when disclosures are required by state or federal security laws or regulations, or in each party's good faith compliance with Section 2.08 hereof. This provision shall survive expiration or termination of this agreement.

IN WITNESS WHEREOF, the parties have caused this License Agreement to be executed as of the date first above written.

EXATRON CORPORATION	TEXAS INSTRUMENTS INCORPORATED U.S. Consumer Products Group
By_____	By_____
Robert L. Howell	William N. Sick
Title Chairman	Title Vice President
Date_____	Date_____

EXHIBIT A

1. Canadian Patent No. 1044681, dated December 19, 1978, reference "Continuous Loop Tape Cassette."

2. United Kingdom Patent No. 1,529,949, dated November 18, 1975, relating to "Endless Loop Tape Cassette."

3. Canadian Patent Application No. 281,038, dated June 21, 1977, relating to "Arrangement for Controlling the Speed of a Motor."

4. U.S. Patent No. 3,846,831, dated November 5, 1974, concerning "Sound Reproducing Apparatus in Which the Drive Means Operates in Response to a Re-Recorded Control Signal."

5. U.S. Patent No. 4,013,239, dated March 22, 1977, relating to "Continuous Loop Tape Cassette."

6. U.S. Patent No. 4,078,194 dated March 7, 1978, relating to "Arrangement for Controlling the Speed of a Motor."

7. U.S. Patent No. 4,107,752, dated August 15, 1978, relating to "High Density Magnetic Storage Disk Comprising a Spiral of Magnetic Tape."

8. U.S. Patent No. 4,127,878, dated November 28, 1978, relating to "Magnetic Tape Recorder/Reproducer for Ratio Recording With Synchronized Internal and External Clock Rates."

MICROTAPE STATUS

PRESENT STATUS

11Am

* PRESENT BREADBOARD DESIGN CAN ACHIEVE 7.4K BAUD WRITE AND 9.7K BAUD READ. OUR DESIGN GOAL IS FOR 8K BAUD WRITE AND 12K BAUD READ.

* THE APPROACH TO CLOSE THE DESIGN GAP IS TO USE THE MICROCODE FEATURE OF THE 70C20 TO INCREASE SPEED IN THE TIGHT LOOP CODE.

* FEASIBILITY OF THE MICROCODE CHANGE HAS BEEN REVIEWED WITH HOUSTON AND WE HAVE GOOD SUPPORT FROM THEM. THE PEOPLE WORKING THIS PROBLEM FOR US WERE NOT AFFECTED BY THE RECENT PERSONNEL SITUATION IN S/C.

3/17/82, CBW, 39-815

PRESENT STATUS - continued

* WE ARE AT THE PRELIMINARY BREADBOARD STAGE AS FAR AS TOTAL SYSTEM OPERATION IS CONCERNED AND WILL BE FOCUSSING ON THE SUCCESSFUL INTEGRATION OF THE FOLLOWING SYSTEM ELEMENTS DURING THE REST OF MARCH.

  - COMPLETE TIGHT LOOP CODE TEST AT 7.4K WRITE AND 9.7K READ

  - COMPLETE I/O BUS CODE INTEGRATION ON BOTH CONSOLE AND PERIPHERAL CODE

  - COMPLETE FILE MANAGEMENT CHECKOUT IN THE PERIPHERAL CODE AND INTEGRATION TO PERIPHERAL I/O CODE IN CONSOLE

* THIS ACTIVITY WILL BE FOLLOWED BY A THOROUGH CHECKOUT OF THE ENTIRE SYSTEM AND THEN THE UPDATE OF TIGHT LOOP CODE USING THE MICROCODE CHANGES WORKED OUT IN CONJUNCTION WITH HOUSTON.

* IN THE EVENT WE ENCOUNTER VERY SERIOUS PROBLEMS WITH THE MICROCODE CHANGES WE HAVE THE OPTION TO ACCEPT 7.4K BAUD OPERATION. I BELIEVE THAT THIS COULD BE AN ACCEPTABLE DECISION. ONE OF THE PRIME REASONS TO CONTINUE WITH THE MICROCODE CHANGES IS TO PROVIDE A GREATER TIMING MARGIN FOR RELIABILITY.

3/17/82, CBW, 39-815

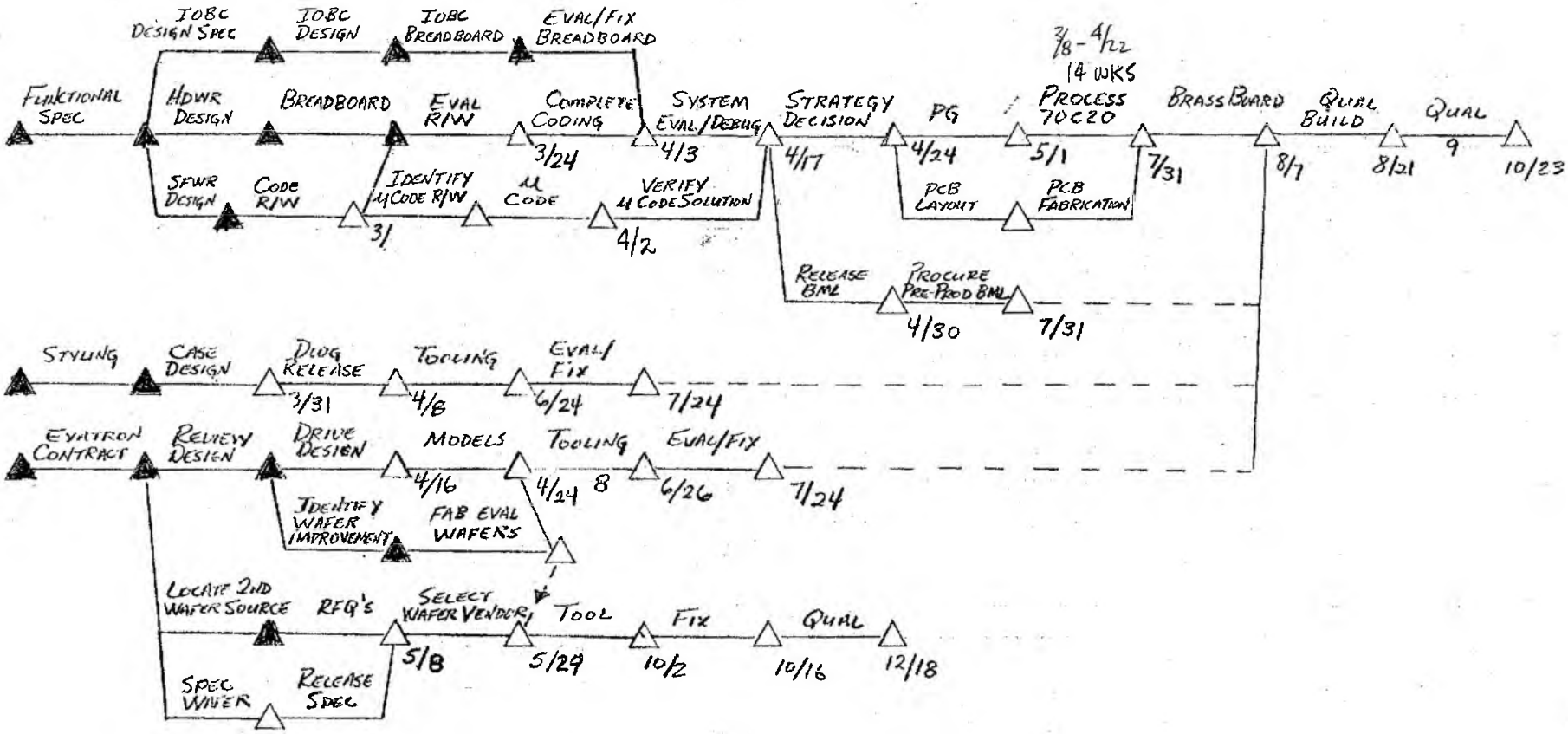
MICROTAPE STATUS

PRESENT RESOURCES

* THE FOLLOWING PEOPLE ARE WORKING ON THE MICROTAPE PERIPHERAL.

PERSON	TASK	TIME
JIM ARNOLD	PGM MGMT	PART
JERRY ROBINSON	HARDWARE DESIGN	FULL
JEF WINSOR	PERIPHERAL SOFTWARE	FULL
CRAIG BENSON	MICROCODE AND CONSOLE INT	PART
ILYA SHIMON	I/O BUS HARDWARE	PART
ROY MATNEY (HOUSTON)	MICROCODE	PART
TOM ALBERS (HOUSTON)	MICROCODE	FULL

3/17/82, CBW, 39-815



EVATRON QUAL

excellence in electronics

C.B. Wilson
Engineering Manager
Texas Instruments, Inc.
P.O. Box 10508, MS 5891
Lubbock, TX 79408
April 30, 1982

Dear C.B.,

As follow-up to our meeting of April 23 and the subsequent phone conversation, I'm outlining Exatron's overall program for wafer cartridge production as well as some of Exatron's general plans for ESF production. These items are shown in the attached charts.

The plan contained herein assumes that Exatron will tool and manufacture the wafer, as well as our standard transport and drive units. Please let us know if you have any questions or comments.

Below you will find my attempt to summarize the open issues between Exatron and Texas Instruments. Please feel free to comment on these also.

ISSUES

1. There needs to be resolution on who, Texas Instruments or Exatron, is responsible for and controls the initial set of wafer tooling. The options are:

   - Texas Instruments procure tooling, sell parts to Exatron and allow Exatron engineering access to the production for process control purposes.

   - Exatron purchase tooling from a vendor, (who will do the plastic production) and ship finished wafers to Texas Instruments. Texas Instruments would possibly consider advancing Exatron funds against the outstanding portion of license payment for this purpose.

   - Some other variation of the above.

2. There needs to be finalization of wafer drawings as soon as possible.

3. Product specifications and acceptance criteria need to be established and agreed upon.

4. Standard data and interface formats need to be devised by Exatron, but Texas Instruments will submit suggestions for its new product.

5. Product release date (to the public) has yet to be established by Texas Instruments.

6. Product delivery schedule and pricing have yet to be established.

7. Exatron needs to prove to Texas Instruments its ability to mass produce a quality product in order to receive production volume commitments from Texas Instruments.

8. Exatron must find a viable second source to independently produce and market the ESF products.

We look forward to hearing from you and to pursuing this exciting program together.

Sincerely,

Robert A. McDonald
President

RAM/jmo

Enclosure

cc Robert Howell
Rey Smith

TEXAS INSTRUMENTS
INCORPORATED

May 24, 1982

Robert McDonald President
Exatron Incorporated
181 Commercial Street
Sunnyvale, California 94086

Dear Bob,

Thank you for your letter outlining your plans for wafer production and product improvements. I would like to go over the points in your letter to continue our discussion.

1. Wafer tooling: We have decided to go ahead with prototype tooling for the wafer top case, bottom case, pressure roller hub, reel hub, and reel tray. These orders will be placed this week with final drawings planned for 5/24. These tools would be our tools but we will continue to be interested in cooperative work with you in the debug phase and for assembly. With the exception of the pressure roller hub, all these tools are one cavity prototype tools which are being produced for short turnaround and are only designed to provide limited production capability (at least 100K units). Since the roller hub is so small and simple, it seems just as quick and cheap to make an eight cavity production tool for it. We plan to have all these tools completed by mid July and our main purpose is to get clean tooling to prove the design and make any necessary corrections. As I see it, a decision on hard, high volume tooling for our requirements can be postponed until late August by taking this approach. I hope this will get both of us some further experience with the design ASAP and give you or a second source some additional time to plan hard tooling so TI may never need take that step. I would like you to let me know if this plan will cause you any difficulty. With respect to financing for your tooling, I think that it would be difficult for us to advance future license payments at this point but I will be willing to reopen this issue if you feel there is a basis for further discussion.

2. Finalization of Wafer Drawings: After our visit to your plant last week, I believe our engineers have a pretty clear idea of the final tweaks to the wafer design. At Rye Smiths' recommendation, we are going to make as few changes as possible. Enclosed is a summary of these changes and we will forward our drawings next week when they are released to the tooling vendor. If you have any suggested changes or corrections, we would like to have those and resolve them. Due to the time schedule, these changes need to be made next week.

3. Product specifications and acceptance criteria: We still need a little more time to develop a full part specification for the wafer. But, I think that one of the concerns for both Exatron and TI has been the life issue so I would like to update you on that. First, our original spec of 250 hours or 40,000 passes was based on an assumption of a constant failure rate with age and Rye has pointed out that this is probably not the case for this wafer. (But then a 250 hour MTBF is the spec for eight track cartridges.) After Rye's comment we ran some tests and after some 1600 wafer hours so far I believe that the failure distribution probably does show increasing failure rate with age, roughly a Weibull distribution with a shape factor of 1.5 (where an exponential distribution would be 1). So I am beginning to think that the way we might spec this would be to require less than 1% failures at 3 hours of operation and less than 3% failures at 10 hours of operation at a 90% confidence level. Our most recent test suggests that current parts are in this range, so with the tooling changes and process control, I would think this spec could be conservatively met.

4. Standard data and interface formats: We have already sent you data on our I/O bus for peripherals (including the tape drive). This is a distributed computing bus which I feel is good for portable products and for generality. For lowest cost desktop computers, an address/data bus is possibly better. We would certainly like your comments and following our introduction we will encourage compatible use of this bus by other suppliers. We will be able to provide you with a spec for our tape and directory format in about 6 weeks.

5. Product release date: This is a very sensitive point for TI, and I am not able to give you any definite date here. The date that is important to me is to have a qualified wafer by September.

6. Product delivery and pricing: These issues will need to be negotiated by our purchasing agent as soon as your production capabililty is assessed a bit more.

7. Wafer second source: We felt that our meeting went fairly well with NCR this week and expect some response from them in about a week. We mentioned the possibility of jointly visiting Exatron if they make a decision to proceed further. I will keep you posted.

I am most interested in continuing to discuss our respective plans for wafer tooling and assembly. In addition to NCR, we plan to talk to two or three other large companies plus Verbatim who is still an outside possibility. Also, we have some tenative ideas about sources for assembly only and would like to jointly discuss this point.

Sincerely,

C.B. Wilson
Engineering Manager
CBW/mh
enc.1

CC: Jim Arnold
Douglas Dobbs
Gary Futrell

WAFER CHANGES

HUB AND TRAY ASSEMBLY

* REDUCE TRAY DIAMETER FROM 1.380 TO 1.160

* INCREASE BEARING DIAMETER FROM .150 TO .400 (MAKE IT A PART OF THE TRAY AS OPPOSED TO PART OF THE HUB)

* REDESIGN INTERNAL MATING SURFACES FOR ULTRASONIC WELDING AND PROVIDE ENERGY DIRECTORS

WAFER CHANGES

TOP AND BOTTOM CASE

* REDESIGN TOP AND BOTTOM CASE MATING AREA WITH INTERLOCKING SECTION FOR ULTRASONIC WELDING

* PROVIDE RECESS IN TOP CASE FOR SLIDE COVER SUPPORT

* MAKE TAPE GUIDE IN BOTTOM CASE WIDER BY .044

* REDUCE HEIGHT OF TAPE GUIDE IN TOP CASE TO MATCH THE HEIGHT IN BOTTOM CASE

* FILL DEPRESED AREAS IN BOTTOM CASE PROVIDED BY REDUCED TRAY SIZE

* PROVIDE STEPPED DIAMETER AT THE TOP OF THE TRAY HUB SHAFT FOR SONIC WELDING

* PROVIDE LARGER GAP FOR MOTOR SHAFT IN THE WAFER SLOT FOR APPROPRIATE CLEARANCE

WAFER CHANGES

MATERIALS

* CHANGE HUB AND TRAY MATERIAL TO LOW FRICTION MATERIAL (DELRIN)

* CHANGE TOP CASE AND BOTTOM CASE MATERIAL FOR IMPROVED STABILITY IN 75 DEG STORAGE (ACRYLIC APPEARS OK, ANOTHER CHOICE IS POLYCARBONATE)

  - IT WILL BE POSSIBLE TO INSERT THE TOOL TO CREATE A HOLE IN THE TOP CASE WHERE THE EOT SENSOR OPERATES AND MAKE A LABEL WITH A CLEAR APERATURE TO ALSO ALLOW USE OF OPAQUE MATERIALS WHICH ARE MORE STABLE (BUT LESS EXPENSIVE THAN POLYCARBONATE)

WHAT ARE YOUR THOUGHTS?

B. C.

6-7182

M E M O R A N D U M

June 22, 1982

TO: Bob Curlee

FROM: John Thomas

SUBJECT: QUOTATION

This quotation is in response to a meeting with Jerry Robinson on June 18, 1982.

PGM - ALC

Estimated run rate - 10-20K/U Month
Production Start - October 1982

OPTIONS:

1. Second Source SPX1397-1 reflective sensor

   I could quote some figures here but the problem is that I do not have a standard that could fit within the mechanical limits of the SPX. Therefore, I would have to tool everything from the sensors on up. The tooling costs would be substantial, but the limiting item would be time, around six months to a year to get all the parts designed, qualified, and into production.

   To sum it up, I do not believe that we would give you a near-term competitive quote on this device.

2. A new reflective sensor of TI design.

   We could build a sensor that would meet your needs but the overall case dimensions would be approximately .200 thick, .300 length, and .650 wide. This could fit into your case, but would project about .050. This would require re-tooling your case. Our budgetary estimate would be:

QTY	100K	200K
$	1.00	.92

   Note: Pricing includes estimated tooling costs.

3. This we believe would be the most cost effective approach. What we could do is evaluate your needs and recommend a case change that would allow you to insert discrete sensors and emitters directly into your re-tooled case.

   We would evaluate the need and supply the necessary information on desired hole size and angle, plus build a prototype to evaluate the use of the sensor/emitter distribution.

   Budgetary Pricing (Assuming entire distribution is useable)

QTY	100K	200K
TIL32	.17	.16
TIL78	.14	.13
TOTAL $	.31	.29

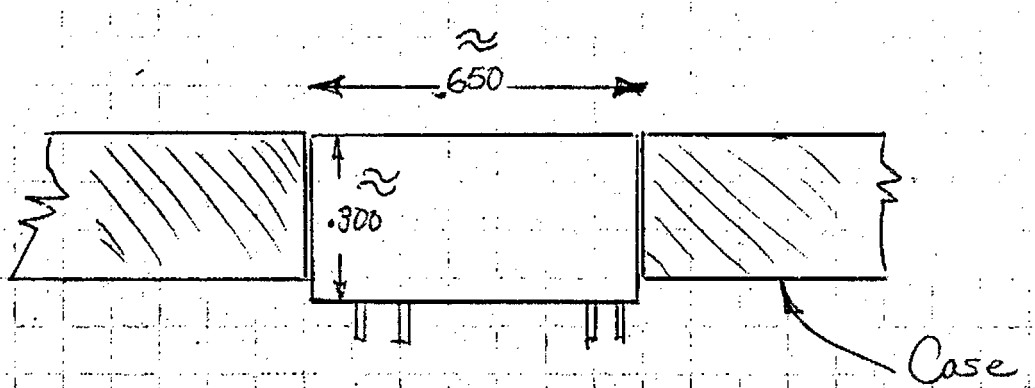
I believe that these options will give you some alternatives. If there are any questions please call.

Regards,

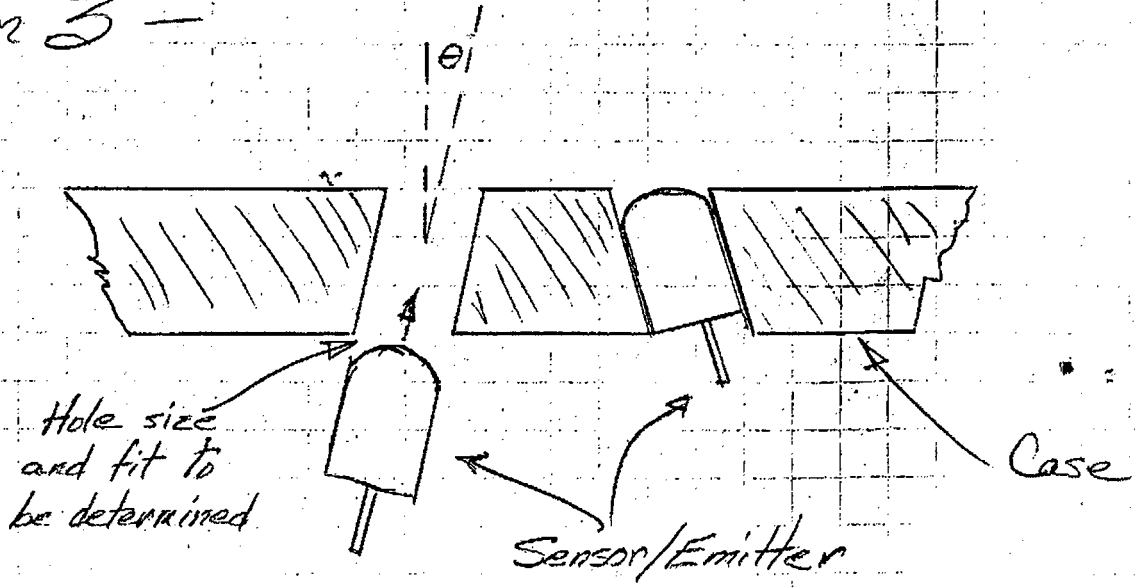
John Thomas

JFT/dr

Option 2 —

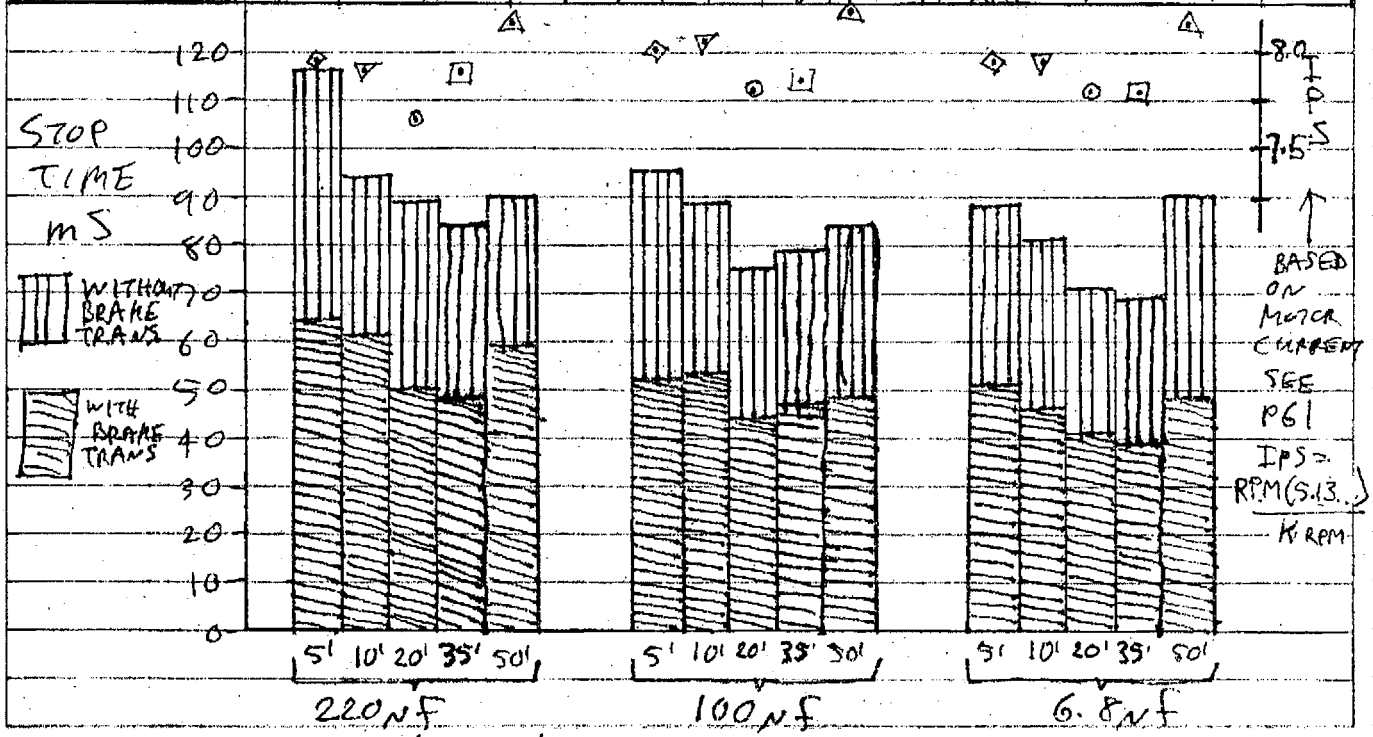


Option 3 —



THE PREVIOUS STOP DATA SUBMITTED TO C.B. HE SAYS THE TIME INFORMATION IS NOT VALID BECAUSE THE SPEED WAS DERIVED FROM TAPE LENGTH WHICH IS NOT ACCURATE FROM TAPE TO TAPE (20% ERROR) AND ALSO BECAUSE THE SPEED IS A DECAYING FUNCTION WITH TIME. C.B. SUGGESTS DETERMINE STOP TIME BY TRIGGERING A SCOPE ON EOT AND FEEDING DATA OUT TO A SECOND CHANNEL, DERIVE STOP TIME FROM TRIGGER TIME UNTIL DATA CEASES. ALSO IT IS DESIRED TO RECORD THE MOTOR CURRENTS FOR VARIOUS OTHER CORRELATIONS. - SAME CONDITIONS AS P101 - STOP TIMES —

WAFER	C = ~~220~~ 6.8nF			C = 100nF			C = ~~68nF~~ 220nF		
TYPE	BRAKE	NO BRAKE	Im	BRAKE	NO BRAKE	Im	BRAKE	NO BRAKE	Im
5' ⟩	51mS	88mS	43mA	52mS	95mS	42mA	64mS	116mS	43mA
10-103	46mS	81mS	43	53mS	89mS	41	61mS	94mS	44mA
20-122	41mS	71mS	46	44mS	75mS	46	50mS	89mS	49mA
35-105	39mS	69mS	46	47mS	79mS	45	48mS	84mS	44mA
50-118	48mS	90mS	39	48mS	84	38	59mS	90mS	39mA
AVG	45mS	80mS	43mA	49mS	84mS	42mA	56mS	95mS	44mA



WORK OF: [signature] DATE 6-24-82

I witness this document and understand its contents.

NAME _____ Date _____

I saw the tests made _____ (Initial if yes)

I witness this document and understand its contents.

NAME _____ Date _____

I saw the tests made _____ (Initial if yes)

WORK OF: [illegible] DATE: 6-24-82

STOP TIMES FOR 220 NF WAFER	WITH BRAKE	NO BRAKE
5'	48 MS	90 MS
10'	76 MS	82 MS
20'	50	76
35'	40	54
50'	47	79
AVG	52 MS	76 MS

STOP TIMES FOR G.E. 6.8 NF WAFER	BRAKE	NO BRAKE
5'	40 MS	75 MS
10'	41	61
20'	37	65
35'	35	55
50'	44	66
AVG	39 MS	64 MS

I witness this document and understand its contents.

NAME _____ Date _____

I saw the tests made. _____ (Initial if yes)

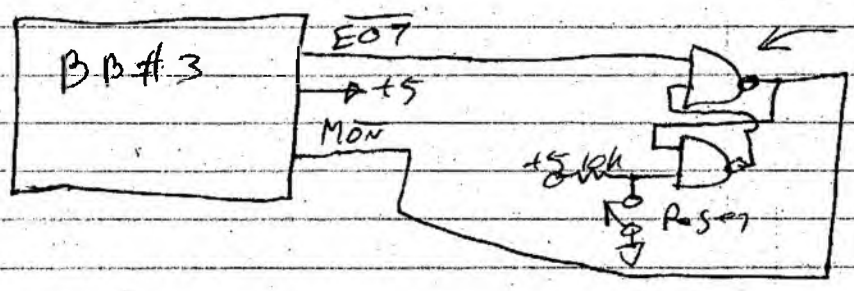
I witness this document and understand its contents.

NAME _____ Date _____

I saw the tests made. _____ (Initial if yes)

MOTOR STOPPING TIME - AS A FUNCTION OF THE MOTOR SUPPLY FILTER CAPACITOR AND USE OR NON-USE OF MOTOR BRAKING TRANSISTOR

PROCEDURE: SEE PAGE 83 FOR MOTOR POWER SUPPLY CIRCUIT (RS = 10k). EOT MARKER USED TO STOP THE MOTOR USING THE CIRCUIT BELOW



METHOD: TAPE INSERTED AND RESET SWITCHED TO START MOTOR. EOT MARKER CAUSES R-S FLIP-FLOP TO FLIP AND THE OUTPUT TURNS THE MOTOR ON SIGNAL OFF. TEST CONDITIONS: V_{BATT} = 5.00 VOLTS. V_{MOTOR} SET TO 4.00 VOLTS. STOP TIME OR DISTANCE MEASURED BY MEASURING THE DISTANCE THE EOT FOIL MOVES FROM THE CENTER OF THE EOT WINDOW. DISTANCE MEASURED FROM FRONT EDGE BACK TO EOT WINDOW CENTER. TAPE SPEED MEASURED BY COUNTING TIME FROM EOT TO EOT.

MOTOR VOLTAGE = 4.00 VOLTS - USING PLASTIC MILLED MECHANICS

WAFER TYPE	C = 220μF/16V		C = 100μF/10V		C = 6.8μF/6V		TIME EOT TO EOT	CALCULATED SPEED IPS
	BRAKE IN	BRAKE OUT	BRAKE IN	BRAKE OUT	BRAKE IN	BRAKE OUT		
5' X	320 mils	600 mils	300 mils	550 mils	270 mils	500 mils	9 sec	6.7 IPS
10' 10-103	540	580	330	550	290	430	17 sec	7.1
20' 20-122	310	470	270	~~700~~ 430	230	400	39 sec	6.2
35-105	260	350	230	380	230	360	65 sec	6.5
50-118	340	580	340	540	320	480	82 sec	7.3

THIS DATA WILL BE CHARTED ON THE NEXT PAGE. STOP DISTANCES ARE RECORDED. STOP TIMES CAN BE CALCULATED FROM THIS AND THE SPEED.

WORK OF: [signature] DATE: 6-23-82

I witness this document and understand its contents.
NAME ..... Date .....
I saw the tests made ..... (initial if yes)

I witness this document and understand its contents.
NAME ..... Date .....
I saw the tests made ..... (initial if yes)

-MSG M#= 86251 FR=JPER TO=ALCC SENT=06/25/82 12:56 AM
R#=081 ST=C DIV=039 CC=0160 BY=JPER AT=06/25/82 12:50 AM
TO - DANIEL CHEN - ALCC
CC - C.B. WILSON - ALCC
FM - YOKU NISHIMURA PMM/TKO - JPER
JPER 6-25-82 14.47
REF-YOK-06-106 URGENT ***
SUBJ - MICRO-TAPE / TOKYO MAGNETIC PRINTING (TMP)
DANIEL, THIS IS TO LET YOU KNOW THAT DR. NAMIKAWA OF TMP HAS JUST SIGNED NON-DISCLOSURE AGREEMENT NDA 1773 TODAY (6-25-82), AND THUS I HAVE RELEASED APPLICABLE COPIES OF DOCUMENTS PLUS ONE SAMPLE TO HIM FOR HIS STUDYING TMP'S PRELIMINARY QUOTE WORKS.
DR. NAMIKAWA WILL TRY TO ANSWER IF THEY ARE ABLE, OR NOT ABLE WITHIN 2 WEEKS.

SHOULD YOU BE HERE FOR THE PERIOD OF JUNE 28 THRU JULY 4TH AND IF YOU NEED TO HAVE AN INTERIM DISCUSSION WITH THEM, YOU CAN GO AHEAD TO CONTACT AND MEET.
DR. NAMIKAWA/ PHONE TOKYO 835-5771, IN CASE HE IS ABSENT, MR. OTSUKA AT THE SAME PHONE NUMBER WILL BE ANSWERING FOR YOU, AND SHOULD TWO OF THE ABOVE PERSONNEL IS OUT OF CONTACT, THEN YOU CAN CONTACT MR. TOCHIHARA, THE PLANT MANAGER AT PHONE 0427-59-2221.

AS I AM STILL OCCUPIED BY OTHER PRIORITIES, I CANNOT BE ACCOMPANYING TO YOU, HOWEVER, IF I CAN KNOW YOUR ITINERARY AND HOTEL, I WILL SUBMIT THE ORIGINAL NDA 1773 TO YOU.

NEW SUBJECT / RIKEI --- MR. OKUMURA
I VOLUNTARILY HAVE CONTACTED THEM WHATABOUT THEIR QUOTE POSITION, AND FOUND FROM MR. OKUMURA THAT HITACHI MAXELL HAS BECOME NEGATIVE BECAUSE OF A TECHNICAL PROBLEM, THEN, THEY WERE CONTACTING "OLYMPUS" (MANUFACTURER BOTH FOR OPTICAL PRODUCTS/CAMERAS, AND CASSETTE RECORDERS), AND MORE SURPRISING HE MENTIONED, HE ALSO CONTACTED SONY. I SUGGEST YOU SHOULD TELEX HIM AGAIN TO CONFIRM THEIR LATEST POSITION. PROBABLY, MR. OKUMURA MAY TELEX YOU SOMETHING IN A NARROW DAY.

RGDS.

YOKU NISHIMURA PMM/TKO YN - JPER

Jim –

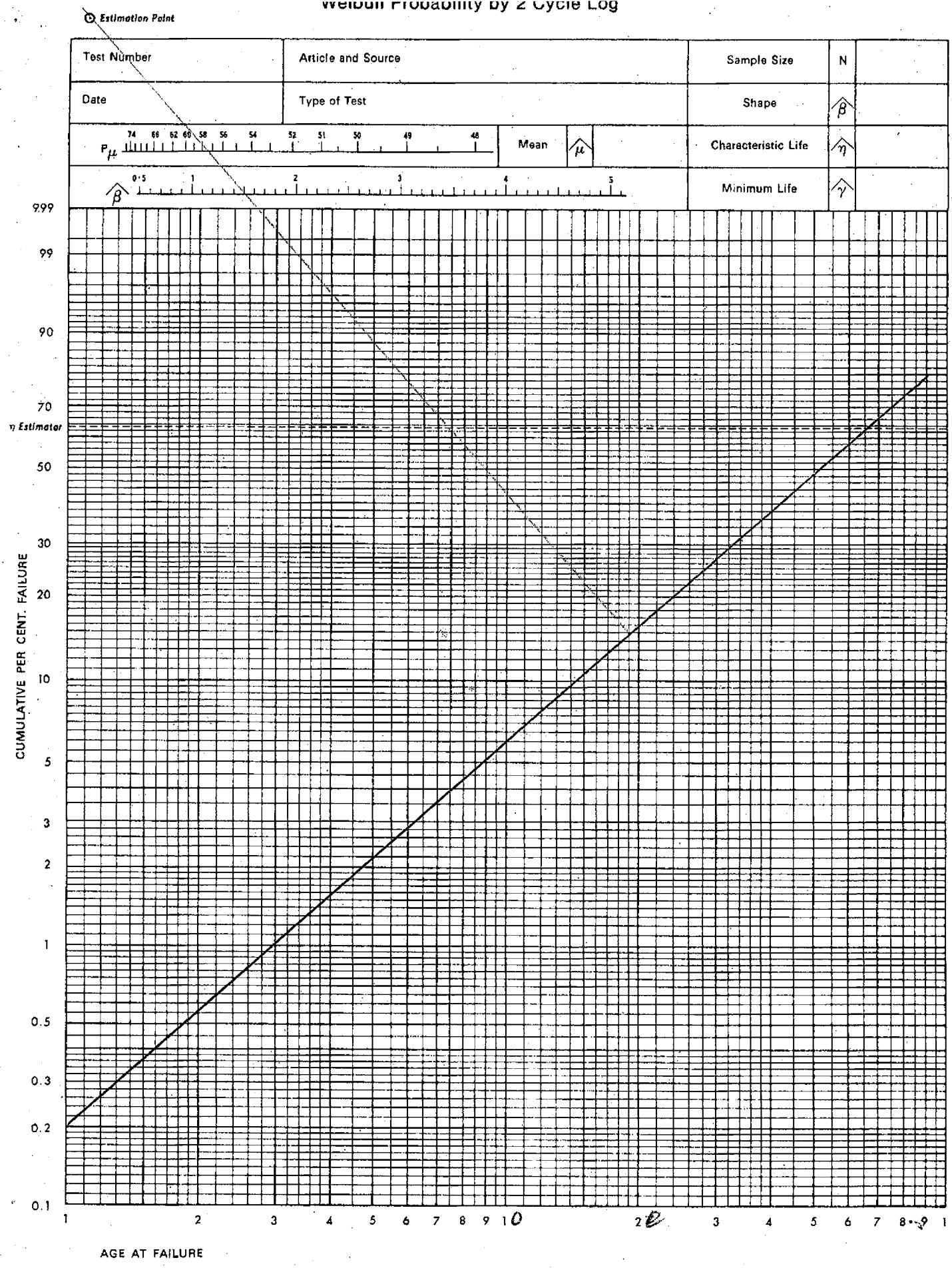
These are my assumptions on wafer life –

A. Several scenarios are shown on one of my work sheets. From this I judged that 1% failures at 90% conf. level after 3 hrs of operation and 5% failures at 9 hrs is a possible spec. Failure means catastrophic (breakage, optics fail, hard errors due to flaking oxide, high friction, etc) (we may need the spec to mention drive conditions, ie max current allowed in our drive) or also significant degredation of soft error rate § (perhaps $< 10^{-4}$).

B. I think the following two tests might be appropriate to verify the above.

1. Run 1000 wafers 3 hours. Use data recorded at beginning of test to be played back, (~~you get~~, if fail read first time, then must read each of 3 successive trys perhaps) The test will not be passed if more than 7 units fail.
2. Run 500 wafers 9 hours. Same criterion and the test will not be passed if more than 20 fail.

This can help make a curve of failures allowed vs bit time for this test


Weibull Probability by 2 Cycle Log
Estimation Point
Test Number
Article and Source
Sample Size
N
Date
Type of Test
Shape
Mean
Characteristic Life
Minimum Life
74 66 62 60 58 56 54 52 51 50 49 48
0·5 1 2 3 4 5
99.9
99
90
70
η Estimator
50
30
20
10
5
3
2
1
0.5
0.3
0.2
0.1
CUMULATIVE PER CENT. FAILURE
1 2 3 4 5 6 7 8 9 10 2 3 4 5 6 7 8 9 1
AGE AT FAILURE

1%

MEAN (56%)

WAFER LENGTH	HRS	PASSES	SCORE	HRS	PASSES
5'	3	1480	1.5		
SCENARIO:	5	2466			
LOAD/SAVE PGM (1 pass)	9	4438			
5 times/day	15	7397			
5 days/wk					
50 weeks/yr = 1250 passes.	26	12822			
10'	3	740			
Use PGM w/ DATA (2 pass)	5	1233			
10 times/day	9	2219			
1 days/wk	15	3698			
50 wks/yr = 1000 passes	26	6410			
25'	3	295			
Use data/pgm (2 pass)	5	492			
3 times/day	9	885			
3 day/wk	15	1475			
40 wk/yr = 720	26	2558			
50'	3	148			
Use data/pgm (2 pass)	5	246			
2 times/day	9	443			
3 days/wk	15	738			
50 wk/yr = 600	26	1278			

	8.2 IPS TIME	CAPACITY
5'	7.3	
10'	14.6	
25'	36.6	
50'	73.2	

(319)	(871)	(232)
10	20	50
13	22	114
34	68	
51	69	
70	69	
168	228	114
42	57	
50%	25%	50%

90% CONF

20 drives
3 hrs/wafer
4 lots/day → 80 wafers/day
400/week

4-6 weeks

4 weeks = 1600
6 weeks = 2400

Assume 1000 with 10 fail @ 90%

$.01 \pm \left(\frac{.01(.99)}{1000}\right)^{1/2} 1.28$

$\pm .004$

1.4% @ 90% CONF

7 FAIL @ 90%

$.007 \pm \left(\frac{.007(.993)}{1000}\right)^{1/2} 1.28$

$\pm .0034$

$.0036 - .0104$

.36% – 1.04%

Assume 1600 with 16 fail @ 90%

$.01 \pm \left(\frac{.01(.99)}{1600}\right) 1.28$

5% max at 9 hrs with 500 units

$.05 \pm \left(\frac{.05(.95)}{500}\right)^{1/2} 1.28$

$\pm .012$

$.04 \pm \left(\frac{.04(.96)}{500}\right)^{1/2} 1.28$

$\pm .011$

$.03 - .05$

20 FAIL @ 90%

$.04 \pm \left(\frac{.04(.96)}{100}\right)^{1/2} 1.28$

$\pm .026$

$.035 \pm \left(\frac{.035(.965)}{333}\right)^{1/2} 1.28$

$.035 \pm .013$

$.032 - .048$

500
.04
20.00

R.L. BENJAMIN ASSOCIATES
405 Ridgewood Drive
Richardson, Texas 75080
(214) 783-8319

Final & Composite Report
June 30, 1982
Texas Instruments, Lubbock
Microtape Peripheral

NOTE:

This report covers the recommendations made over the period of this contract and therefore contains recommendations that may have already been tested and incorporated into the design by Texas Instruments, Inc. There are some final recommendations contained in this report that may not have been tried by Texas Instruments at the time of this report.

Read/Write Circuit:

The first area investigated was the head chosen. The head gap is considered to be not optimum for the frequency spectrum desired of 4-12 Khz. The 100 microinch gap head being used has a peak output when operating at 10 ips at 50Khz. At 4Khz, the output is down 12 db and at 12 Khz it is theoretically down 3 db. The gap width, tape speed and frequency recorded are interrelated. The theoretical response for perfect playback head maximum output occurs when the gap length equals one-half the wavelength of the signal passing under it. Thus, for a 100 microinch head and a tape speed of 10 ips, the frequency for maximum output on a read is when the ratio of the magnetic gap length to the effective wavelength is equal to 0.5 or the effective wavelength is 200 microinches. The peak frequency is 10 ips/200ui = 50 Khz. Increasing the gap width will help

the playback amplitude, but will require higher write currents. Based on a previous design done by a member of our staff, the gap on the current head is a reasonable tradeoff for optimum reads and writes.

Write Circuit:

The IC used to supply the write current to the head does not appear to have sufficient drive capability. The 80C98 is spec'd at 4 ma output under a short circuit condition. Another device should be used such as the 74C240 which has 4-5 times the drive capability of the 80C98. The shaping network currently being considered has a peak current of 4.4 ma in the breadboard which is close to 150% of the current required to erase the tape (3 ma as reported to us by C.B.). However, adding up the worst case driver impedances and resistors, the worst case DC current is 1.7 ma at 5 volts. We recommend that the head impedance be lowered from 50 mh to 10 mh, the series resistors changed to 390 ohms, two 74C240 stages be paralleled on each side of the head and the parallel capacitors be removed. The time constant will then be 8 usecs or 12.8% of the total time between flux transitions.

Read Circuit:

The first stage gain is 11 and the second stage gain is 10. There is a concern over the apparent redundancy of the second stage amplifier and the comparator in that both are essentialy inverting saturating amplifiers. The second stage amplifier clips the output at 0.65v. If the diodes were removed, and the gain of the second stage were reduced, it may be possible to eliminate C16. Care must be taken to investigate the possible ranges on the input offset variations, but a preliminary calculation shows it is possible. The comparator on the output of the two stage op amp read circuit is not correct in our opinion. The hysterisis should be in the positive leg as Exatron has drawn. The minus input should be tied directly to the output of the second op amp and the positive input should be tied through a resistor to the bias supply. The bias supply should have a 4.7 uf and a 0.1 uf decoupling to keep it stable. Also the hysterisis resistor R11 should be larger than the output pull-up on the comparator to keep it from oscillating. R11 should be 22K and R43 should be 10 K.

BOT/WP Sensors:

There is a way to reduce the number of parts in the BOT/WP area which will require a software change as well. Either Q4 or Q3 can be eliminated if the LEDs in the sensors are wired in series and enabled by the same transistor. No additional current will be required when reading either sensor and the parts count can be reduced.

Step Down Regulator:

The step down regulator essentially is the circuit in Figure 1. The first step is to make an approximation of the operating frequency. Assume 1% ripple allowable on the motor (0.4v). The question is how long does it take at 25ma through the motor to discharge C4 by 0.4 volts (This also assumes the hysteresis is 0.4V)? If C = 220uf, then t = (EC)/I or 0.4x220x10E-3/25xE-3 or 352usec or an operating frequency of roughly 2.8Khz. This is an order of magnitude lower than the desired range of 25-50Khz where the size and cost of the inductor becomes reasonable. Therefore, the capacitor can be reduced an order of magnitude which also saves in the cost of parts. Then t would be 35 useconds.

There are three modes a step down regulator can operate in. One is where the transistor turns on before the catch diode (D11) finishes conducting. This causes excessive heating of the catch diode especially if the reverse recovery time of the diode is very long. The catch diode overheating is one of the common failures of switching regulators when they are operated in this mode. D11 should have a reverse recovery time of less than 1 usec to minimize the heating in the diode. The second case is where the transistor turns on just as the diode stops conducting and the third case is where the transistor turns on after D11 stops conducting. The recovery time of the transistor will not matter much if the circuit is operating in the third mode but it still should be on the order of 2-4 useconds.

The inductor needs five parameters specified, the inductance, the frequency of operation, the DC resistance, the Q (Quality Factor) and the DC current rating. The Q does not apply too well in this application of inductors, but needs to be set at some reasonable number to allow the selection of off the shelf vendor parts. Therefore, based on our experience, the Q should be a minimum of 40 at the operating frequency.

If the capacitor is allowed to supply current to the motor for approximately 35 useconds, then Q2 is turned on, allowing the current to ramp up replacing the charge, and then turned off, letting the catch diode, D11, to transfer the energy from the inductor to the capacitor, the circuit will be operating in the third mode mentioned above. To maintain a reasonable efficiency at normal battery voltages, let the inductor drop not exceed 0.2 volts. To replace the 25 ma, the circuit should be charging to a value 4 times the draw current or 100 ma. A charge time should be somewhat less than the discharge time, so set the charge time to about 25 useconds. To avoid approaching the saturation currents of the inductor, its current rating should be 2 times the peak current or 50 ma and the DC saturating current would be 200 ma. The voltage at the output of the inductor will be the battery voltage minus the series diode drops, the drop across Q2 and the inductor. To get an output of 4 volts, there will be, when operating on the battery, approximately 1v across the inductor. The inductance L equals E/(di/dt) or 1/(100ma/25 useconds) or 250uh (10% tolerance).

To avoid excessive losses in the inductor (loss of efficiency), the DC resistance needs to be very low. A drop of .2 volts at 50 ma is 4 ohms but we believe a value of 1 ohm is a better goal to maintain effeciency. Thus, the inductor L1 - should have the following specifications:

Inductor L1

Inductance = 250 uh (10% tolerance)
Frequency = 50 Khz minimum
Q = 40 minimum
DC Resistance = 1 ohm maximum
DC Current Rating = 50 ma

The hysteresis on the voltage comparator should be set to 0.04 volts which is the ratio of the feedback resistor and the AC equivalent of R11, R15 and R16. The latter is now 40.4K, therefore R14 should be 100K.

Step Up Regulator:

The Step up regulator operates in essentially two modes. The first is going from a low battery of 4 volts stepping up to 5 volts and still running the motor and the write head. The second is operating from a low battery of 2.5 volts stepping up to 5 volts to run just the CMOS circuitry. Again, the frequency of operation is chosen to be around 25 Khz. The external capacitor on the 4193 should be 93 pf (circuit board capacitance must be included). The millampere-seconds in the capacitor should = 0 in the step up case.

Consider first the step up from 4 to 5 volts with an estimated load of 10 ma. The cycle within the 40 usec is for the current to ramp up to Ipeak, ramp down based on 5 volts + diode drop = 5.3 volts and then some idle time. Ipeak = 2 x Iload x (1+(Vout-Vin)/Vin) = 2 x .01(1+ (5-4)/4) = 25 ma. If the current is to rise to 25 ma in 20 usec, L = Vin x t on/Ipeak = 4 x 20 x E-6/0.025 = 3.2 millihenrys.

Now consider the second case of stepping up from 2.5 volts to 5 volts at an estimated load of 5ma. Ipeak = 2 x 0.005 (1+ (5-2.5)/2.5)= 20 ma. Note that this is approximately the same as the first case. The DC current should be specified at twice the requirement or 50 ma and the Q again is chosen to be 40. The DC loss should be no more than .25 V. At 25 Khz, XL = 1000 ohms, therefore the DC resistance should be 10 ohms maximum.

Inductor L2

Inductance = 3.2 millihenrys (10% tolerance)
Frequency = 50 Khz
DC Current = 50 ma
Q = 40
DC Resistance = 10 ohms maximum.

C7, the filter capacitor, also can be 22 uf.

The above is a first pass and inductors of with the above specifications should be obtained. Actual peak currents should be then measured and then a final correction of the spcifications if needed can be made. This is not a detailed report as far as the derivations of the equations are concerned or for the experience factors used.

Firmware:

The software was in a state of change when we first looked at it. With the change of the operating frequency of the microprocessor from 2.5 Mhz to 3.58 Mhz, several avenues to make the code more efficient were open. At that time, the software was about 300 bytes over the ROM limit. Also, there were problems in the syncronization on read with the data from the head.

The reduction of code size and still retaining all of the features of the microtape is, in our opinion, achievable. Although the peripheral bus is 4 bits wide, all data transfers were bytes or in multiples of 2 nibbles. Since the microcode changes to the 7040 would allow byte reads and writes as well as nibble wide reads and writes, we determined that it is more code efficient to go to byte transfers and the timing with a 3.58 Mhz crystal is still within the windows required. It does mean a change in the data transfer philosophy. The original code contained a large amount of nearly identical code for specialized cases in the read/write process apparently deemed necessary by the slower clock rate being imposed then. However, we believe with some careful thought, these redundant routines can be eliminated by such methods as using the same register to transfer parameters to a subroutine instead of two nearly identical routines that use different registers and by using a register to hold the error code and deciding later what to do with the error rather than having two similar routines with different exit points due to different errors.

The code that follows is based on going to a byte oriented firmware package. It also contains a read routine that corrects for speed variations during a read record. The current philosophy is to use the leader before a record to provide the timing information for the entire read record operation. This is perhaps not bad if the records are not long or the speed varations along the entire tape are kept to within 5%. From our past experience with reel to reel type cassettes, (not the one reel, endless loop being used here), one cannot guarantee the tape will not bind and slow down the tape at certain points. Therefore, a PLL of some sort is usually required either in the hardware or the software. Since the records can be virtually any length and indeed your software personnel frequently use record lengths of 3000 or greater, a software PLL should reduce the error rate and thus is included in the READ BYTE FROM WAFER routine.

As far as the syncronization problems are concerned, there were several oversights in the timing on start and stop of the tape and the syncronization algorithm that were mutually discovered by the staff at Texas Instruments and our staff. We believe that a non-sync pattern should be written for the motor stop and start times instead of the sync pattern to avoid prematurely assuming the software is in syncronization with the data especially if the PLL idea is not used. That would set the sample point for the data polarity at less than the optimum point and increase the error rate.

```
'/T     N=NUMBER OF BYTES T=MAXIMUM EXECUTION TIME

        * ROUTINE TO WRITE A BYTE TO BUS
4/24    WRBYTE  BTJOP   %HSK,BSTAT,RHELP         ; BIF BUS NOT READY
2/10            MOVP    A,BDATA                 ; MOVE FIRST NIBBLE TO BUS
3/11            MOVP    %DROP,BCNTL
1/32            TRAP    TFLOAT                  ; TOGGLE HANDSHAKE
1/8             SWAP    A                       ; GET TO NEXT BYTE
2/10            MOV     A,BDATA
4/35    WRB1    BTJZP   %HSK,BSTAT,WRB2         ; BIF READY FOR 2ND NIBBLE
4/              BTJO    %FE,BITCON,WRB1         ; KEEP WAITING TIL OUT OF TIME
3/11    WRB2    MOVP    %DROP,BCTNTL
1/32            TRAP    TFLOAT                  ; TOGGLE HANDSHAKE
1/7             RETS
-------------------------------------------------------------------
26 BYTES / 180 CYCLES
        * READ A BYTE FROM BUS
3/73    RDBUS   CALL    @RCVNIB                 ; GET FIRST NIB
2/8             MOV     A,TEMP
3/73            CALL    @RCVNIB                 ; GET SECOND NIB
1/8             SWAP    A
2/8             OR      TEMP,A
1/7             RETS
        *
4/12    RCVNIB  BTJZP   %BAV,BSTAT,GONE         ; TEST FOR BAV ACTIVE
4/12            BTJZP   %IRQ,BSTAT,RCVNIB       ; TEST FOR BUS DATA READY
 /11            MOVP    %RELEAS,BCNTL           ; RESET IRQ
3/10            MOVP    BDATA,A                 ; GET DATA
1/32            TRAP    TFLOAT                  ; RELEASE BUS
2/7             AND     %LSN,A                  ; CLEAR MSN
1/7             RETS
(17/91 MIN)
-------------------------------------------------------------------
29 BYTES / 241 CYCLES MIN)
```

```
        * WRITE BYTE TO WAFER ( CALLED BY TRAP BIT10A)
4/22    TSTB10  BTJO    %>FF,BITCON,TSTB10      ; WAIT FOR END OF BYTE
3/9             MOV     %10,BITCON              ; RESET BIT COUNTER
2/10            MOV     A,B                     ; MOV DATA THROUGH QUEUE
3/10    ADACHK  ADD     A,CHKSUM                ; ADD DATA TO CHECK SUM
3/9             ADC     %0,CHKSUM-1
1/7             RETS
-------------------------------------------------------------------
16 BYTES / 67 CYCLES
        * READ BYTE FROM WAFER ( CALLED BY TRAP BIT8B)
4/22    TSTB8B  BTJO    %>FF,BITCON,TSTB8B      ; WAIT FOR END OF BYTE
2/7             MOV     B,TEMP                  ; SAVE READ DATA
2/10            MOVP    CAPTUR,A                ; GET LAST 1/3 BIT TIME
2/8             MOV     A,TEMP+1                ; SAVE IT
1/14            TRAP    ONE8TH                  ; TAKE 1/8 OF 2/3 BIT TIME
3/10            SUB     A,TWO3RD+1              ; & SUB FROM 2/3 BIT TIME
3/10            SBB     EIGTH,TWO3RD
2/7             RL      TEMP+1                  ; 1/2
 3/10            ADD     TEMP+1,TWO3RD+1         ; ADD IN 1/8 OF NEW TIME
3/9             ADC     %0,TWO3RD
1/14            TRAP    ONE8TH                  ; JUSTIFY TWO3RD TO RIGHT
2/10            MOV     A,TIME                  ; SET NEW BIT TIME
2/8             MOV     TEMP,A                  ; RETRIEVE DATA
3/10            ADD     A,CHECKSUM              ; UPDATE CHECKSUM
3/9             ADC     %0,CHECKSUM-1
1/7             RETS
-------------------------------------------------------------------
37/305
        *
        * PUT 1/8 OF TWO3RD INTO EIGHT
        *
3/10  (ONE8TH)  MOV     TWO3RD,EIGTH
2/8             MOV     TWO3RD+1,A
2/7             RR      EIGTH
1/5             RRC     A
2/7             RR      EIGTH
1/5             RRC     A
2/7             RR      EIGTH
1/5             RRC     A
3/9             AND     %>1F,EIGTH
1/7             RETS
---------------------------------------
18/70
        * RECEIVE & STORE DATA FROM BUS
3/255   RCVPAB  CALL    @RDBUS
2/10            STA     *DATAP
2/7             DEC     DATAP
2/7             DEC     COUNT
2/5             JC      RCVPAB
-------------------------------------------------------------------
```

11 BYTES / 284 CYCLES

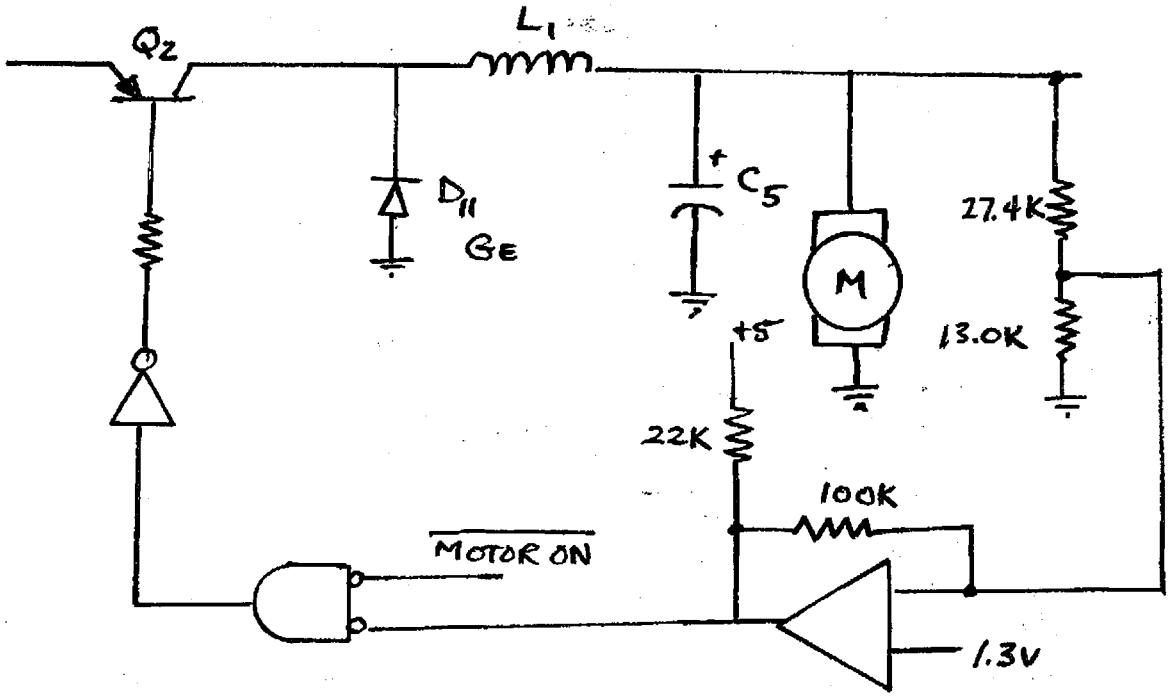


FIGURE 1 STEP DOWN REGULATOR

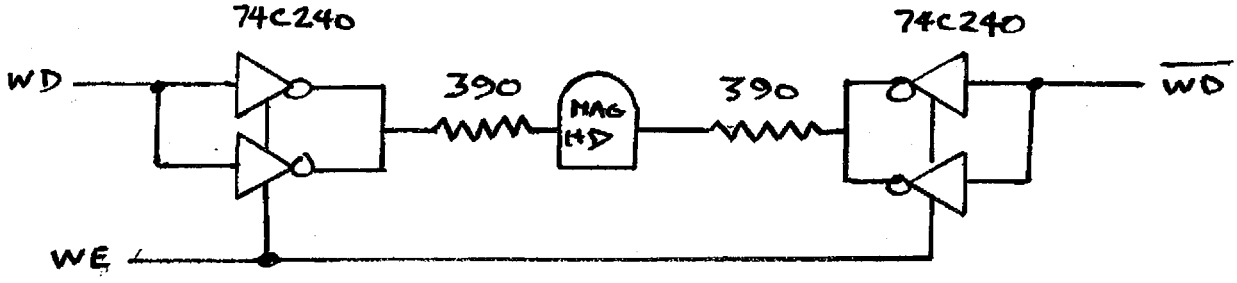


FIGURE 2 WRITE CIRCUIT

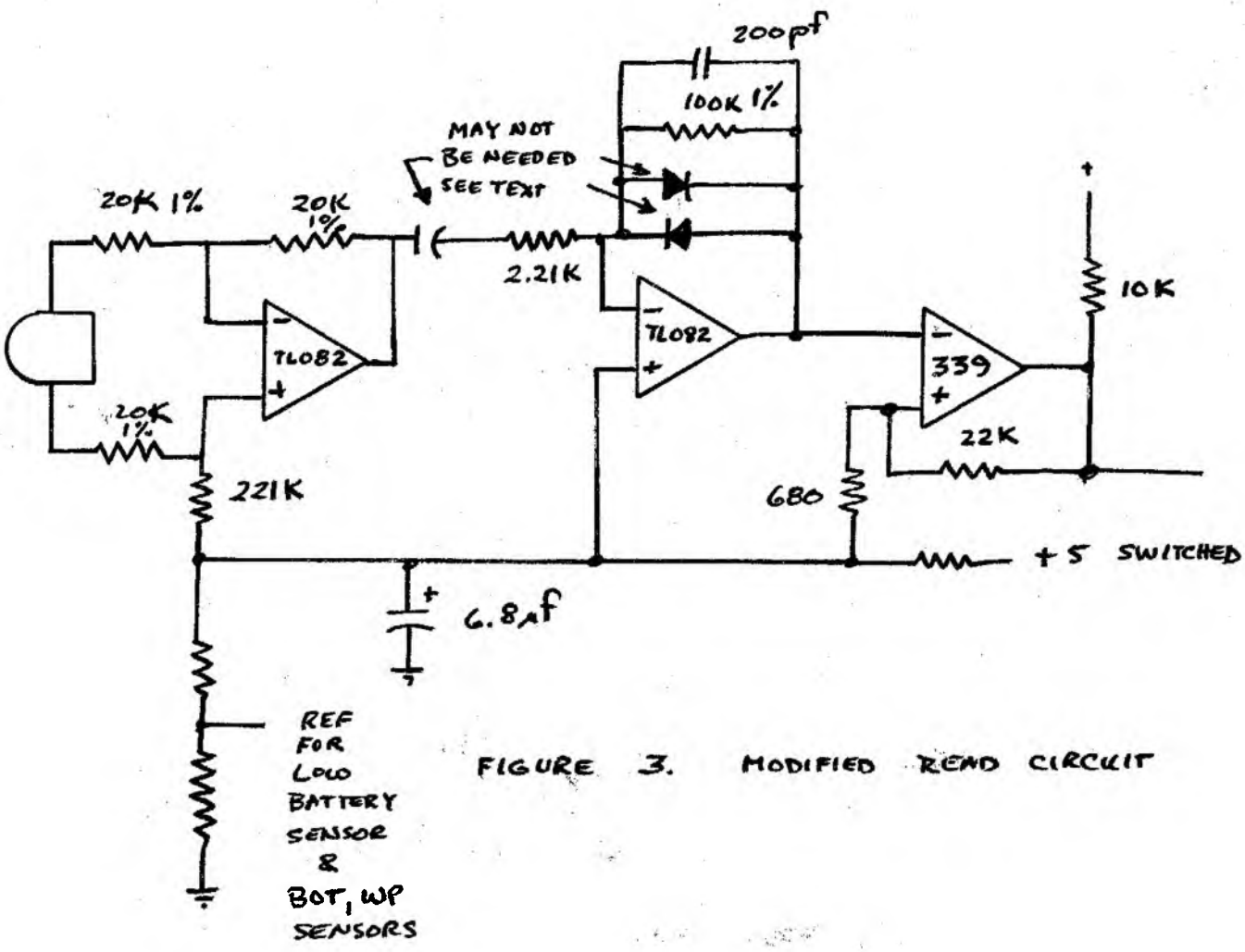


FIGURE 3. MODIFIED READ CIRCUIT

M E M O R A N D U M

August 18, 1982

TO: Leonard P. Lachmann
Dan Swindler

CC: Joe C. Fox
C.B. Wilson
Ryan Provenzano
Gerald Sledd
Edwin Wong

FROM: Kedar Morarka

SUBJECT: PROTOTYPE BUILD OF MICROTAPE WAFERS AT EXATRON:

Jim Aronld and I visited Exatron Corp. in Sunnyvale, on August 11th and 12th for building microtape wafers using plastic parts molded from TI tooling.

We built about 400 wafers of different tape lengths. We did not encounter any major problems in assembling these units. The yield data is as given below:

	CERTIFIED	MECH. REJECT	CERTIFICATION REJECT
O 5 feet	116	2	8
O 10 feet	61	6	7
O 25 feet	60	N.A.	N.A.
O 35 feet	71	5	-----
O 50 feet	63	4	-----

We left 50 wafers at Exatron for their testing. The remaning assemblies will be tested for electrical, mechanical and environmental characteristic at TI to identify any required modification before hard tooling is started. Some of the possible improvements identified for assembling the wafers are-

O Incorporate posative stops in ultrosonic welders for better control of dimensions.

O Device fixture to wind the tape consistently on the spool.

We also visited flurocarben who makes pinch roller for Exatron. The pinch roller tool is in good condition and we can rely on this tool for our initial requirements. We also talked to GBS Incorporated as a potential source for assembling wafers. They are currently manufacting floppy disketts for various companies. GBS has also assembled wafers for Exatron. In my opinion GBS has the capability and expertise to assemble the wafers and they should be given an opportunity for quoting this assembly.

Regards,

K. M. Morarka

Kedar Morarka

1% FAILURE RATE AT

CONFIDENCE LEVEL	Z
60%	.26
70%	.53
80%	.84
85%	1.00
90%	1.28

$$.01 = .009 \pm \left(\frac{.009(.991)}{n}\right)^{1/2} z$$

$z = 1$

$\left(\frac{(.009)(.991)}{n}\right)^{1/2} z = .001$

$\frac{.008919}{n} z^2 = 10^{-6}$

$n = 8919$

$\left(\frac{.008(.992)}{n}\right)^{1/2} z = .002$

$\frac{.007936}{n} = .000004$

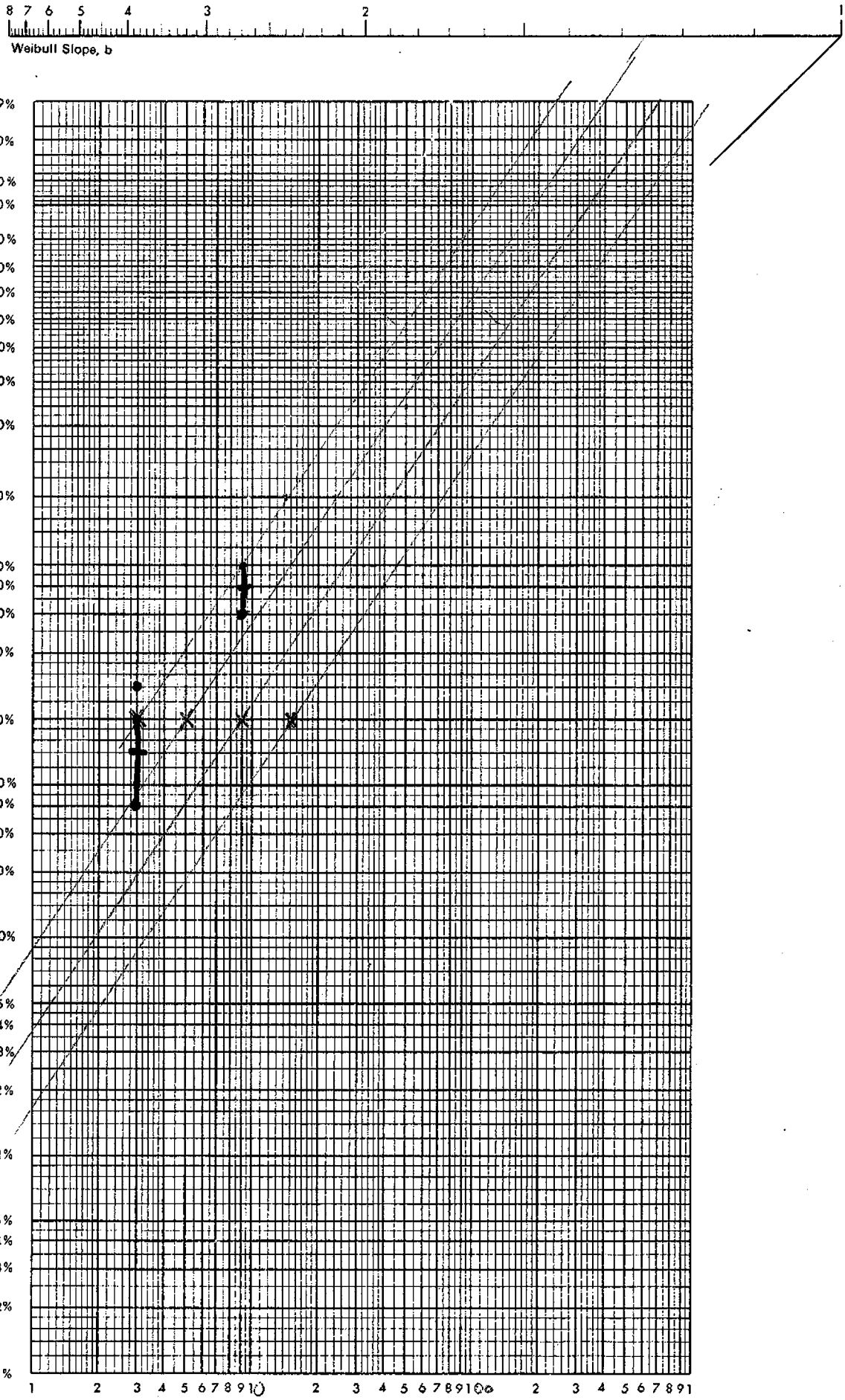
$n = 1984$

$\left(\frac{.007(.993)}{n}\right)^{1/2} z = .003$

H_0: $\pi \leq .01$

H_A: $\pi > .01$

Extended Weibull Probability by 3 Cycle Log



E102 5/12/82 900

WAFER	CUM HRS	OVER 2	OVER 4	OVER 8	OVER 20
10100	51.7	51.7	51.7	51.7	51.7
10116	50.7	50.7	50.7	50.7	50.7
F10121	22	22	22	22	22
F10123	34	34	34	34	34
20100	51.1	51.1	51.1	51.1	51.1
F20101	22	22	22	22	22
20103	51.8	51.8	51.8	51.8	51.8
20106	51.1	51.1	51.1	51.1	51.1
20112	51.1	51.1	51.1	51.1	51.1
20116	42.3	42.3	42.3	42.3	42.3
20118	51.5	51.5	51.5	51.5	51.5
20119	51.1	51.1	51.1	51.1	51.1
20124	51.1	51.1	51.1	51.1	51.1
50106	29	29	29	29	29
50110	50.5	50.5	50.5	50.5	50.5
50111	.62	0	0	0	0
50114	.7 -2.6	0	0	0	0
50118	2.62	2.62	0	0	0
50113	.62	0	0	0	0
50115	4.15 -14.4	4.15	4.15	0	0
50108	4.09 -19.3	4.09	4.09	0	0
50116	.85	0	0	0	0
50112	.88	0	0	0	0
50109	2.05 -4.21	2.05	0	0	0
50107	2.12 -4.28	2.12	0	0	0
50100	4.2 -19.3	4.2	4.2	0	0
10124	1	0	0	0	0
10107	3.09 -5.25	3.09	0	0	0
10104	3.05 -5.21	3.05	0	0	0
10126	1.17	0	0	0	0
35103	10.96	10.96	10.96	10.96	0
35102	10.96 -19.44	10.96	10.96	10.96	0
35101	4.23	4.23	4.23	0	0
35104	3.08 -5.24	3.08	0	0	0
35100	1.96 -5.24	0	0	0	0
20120	.96	0	0	0	0
20123	1.12	0	0	0	0
20125	1.12	0	0	0	0
20109	1.12	0	0	0	0
20121	1.12	0	0	0	0
20102	2.24 -4.40	2.24	0	0	0
20115	4.39 -14.11	4.39	4.39	0	0
20110	2.24 -4.40	2.24	0	0	0
20114	2.24 -4.40	2.24	0	0	0
35107	4.39 -19.60	4.39	4.39	0	0
35108	4.46 -19.67	4.46	4.46	0	0
35106	2.24 -4.40	2.24	0	0	0
10125	4.39 -17.22	4.39	4.39	0	0
35109	4.39 -19.60	4.39	4.39	0	0
35105	11.12	11.12	11.12	11.12	0
20122	1.12	0	0	0	0
50102	1.25	0	0	0	0
50119	1.25	0	0	0	0
50103	2.42	2.42	0	0	0
50104	1.83	0	0	0	0
50105	2.3	2.3	0	0	0
50177	2.25	2.25	0	0	0
10105	2.28	2.28	0	0	0
5110	~~4.6~~ 15.16	4.6	4.6	0	0
5111	4.55 -15.05	4.55	4.55	0	0

70/102 FAIL

50

N = 58

750 hrs / 15 Soks.

10102	2.28	2.28	0	0	0
10109	4.55 - 14.89	4.55	4.55	0	0
10113	2.4 - 4.56	2.4	0	0	0
5105	2.4 - 4.56	2.4	0	0	0
5106	1.28	0	0	0	0
5107	1.28	0	0	0	0
5108	1.28	0	0	0	0
5109	2.4 - 4.64	2.4	0	0	0
20117	1.28	0	0	0	0
10128	1.98	0	0	0	0
10122	1.1	0	0	0	0
10120	1.1	0	0	0	0
10118	1.1	0	0	0	0
10112	4.37 - 6.24	4.37	4.37	0	0
10111	1.1	0	0	0	0
10119	4.37 - 17.20	4.37	4.37	0	0
10117	1.1	0	0	0	0
10103	2.1	2.1	0	0	0
35110	3.08	3.08	0	0	0
20113	1.1	0	0	0	0
10108	1.1	0	0	0	0
10114	1.1	0	0	0	0
20105	1.1	0	0	0	0
10110	1.1	0	0	0	0
10115	1.1	0	0	0	0
20126	1.6	0	0	0	0
20108	1.6	0	0	0	0
5104	2.72 - 4.88	2.72	0	0	0
20114	1.6	0	0	0	0
20107	1.6	0	0	0	0
		0	0	0	0
		0	0	0	0
		0	0	0	0
		0	0	0	0
		0	0	0	0
		0	0	0	0
TOTAL	855.62	811.33	755.17	694.04	661
COUNT	92				

Weibull Probability by 2 Cycle Log

⊙ *Estimation Point*

Test Number	Article and Source	Sample Size	N	
Date	Type of Test	Shape	$\hat{\beta}$	
P_μ 74 66 62 60 58 56 54 52 51 50 49 48	Mean	$\hat{\mu}$	Characteristic Life	$\hat{\eta}$	
$\hat{\beta}$ 0·5 1 2 3 4 5		Minimum Life	$\hat{\gamma}$	

N
80 40 20

CUMULATIVE PER CENT. FAILURE

99.9 99 90 70 50 30 20 10 5 3 2 1 0.5 0.3 0.2 0.1

η Estimator

24 12 6
16 8 4
8 4 2
4 2 1
24 12 6
16 8 4
8 4 2

1 2 3 4 5 6 7 8 9 10 2 3 4 5 6 7 8 9 100

AGE AT FAILURE

E102 5/12/82 900

WAFER	CUM HRS	OVER 2	OVER 4
10100	51.7	51.7	51.7
10116	50.7	50.7	50.7
F10121	22	22	22
F10123	34	34	34
20100	51.1	51.1	51.1
F20101	22	22	22
20103	51.8	51.8	51.8
20106	51.1	51.1	51.1
20112	51.1	51.1	51.1
20116	42.3	42.3	42.3
20118	51.5	51.5	51.5
20119	51.1	51.1	51.1
20124	51.1	51.1	51.1
50106	29	29	29
50110	50.5	50.5	50.5
50111	.62	0	0
50114	.7	0	0
50118	2.62	2.62	0
50113	.62	0	0
50115	4.15	4.15	4.15
50108	4.09	4.09	4.09
50116	.85	0	0
50112	.88	0	0
50109	2.05	2.05	0
50107	2.12	2.12	0
50100	4.2	4.2	4.2
10124	1	0	0
10107	3.09	3.09	0
10104	3.05	3.05	0
10126	1.17	0	0
35103	10.96	10.96	10.96
35102	10.96	10.96	10.96
35101	4.23	4.23	4.23
35104	3.08	3.08	0
35100	1.96	0	0
20120	.96	0	0
20123	1.12	0	0
20125	1.12	0	0
20109	1.12	0	0
20121	1.12	0	0
20102	2.24	2.24	0
20115	4.39	4.39	4.39
20110	2.24	2.24	0
20114	2.24	2.24	0
35107	4.39	4.39	4.39
35108	4.46	4.46	4.46
35106	2.24	2.24	0
10125	4.39	4.39	4.39
35109	4.39	4.39	4.39
35105	11.12	11.12	11.12
20122	1.12	0	0
50102	1.25	0	0
50119	1.25	0	0
50103	2.42	2.42	0
50104	1.83	0	0
50105	2.3	2.3	0
50177	2.25	2.25	0
10105	2.28	2.28	0
5110	4.6	4.6	4.6
5111	4.55	4.55	4.55

10106	2.28	2.28	0
10102	2.28	2.28	0
10109	4.55	4.55	4.55
10113	2.4	2.4	0
5105	2.4	2.4	0
5106	1.28	0	0
5107	1.28	0	0
5108	1.28	0	0
5109	2.4	2.4	0
20117	1.28	0	0
10128	1.98	0	0
10122	1.1	0	0
10120	1.1	0	0
10118	1.1	0	0
10112	4.37	4.37	4.37
10111	1.1	0	0
10119	4.37	4.37	4.37
10117	1.1	0	0
10103	2.1	2.1	0
35110	3.08	3.08	0
20113	1.1	0	0
10108	1.1	0	0
10114	1.1	0	0
20105	1.1	0	0
10110	1.1	0	0
10115	1.1	0	0
20126	1.6	0	0
20108	1.6	0	0
5104	2.72	2.72	0
20114	1.6	0	0
20107	1.6	0	0
		0	0
		0	0
		0	0
		0	0
		0	0
		0	0
		0	0
TOTAL	855.62	811.33	755.17
COUNT	92		

9.2hrs

.03

5/12 0900 10-12 hrs additional not loggcs. -12-

E102 5/10/82 ~~1100~~

WAFER	CUM HRS		OVER 2	OVER 4	OVER 8	OVER 20
10100	13.6	51.7	13.6	13.6	13.6	
10116	12.71	50.7	12.71	12.71	12.71	
10121	12.69	—	12.69	12.69	12.69	FAILED @ ~~12:30~~ 22+34
10123	12.7	—	12.7	12.7	12.7	FAILED @ 34
20100	13.04	51.1	13.04	13.04	13.04	
20101	13.05	51.8	13.05	13.05	13.05	FAILED @ ~~12:30~~ 22+34
20103	13.81	51.1	13.81	13.81	13.81	
20106	13.05	51.1	13.05	13.05	13.05	
20112	13.12	51.1	13.12	13.12	13.12	
20116	7.1	42.3	7.1	7.1	0	
20118	13.06	51.5	13.06	13.06	13.06	
20119	13.06	51.1	13.06	13.06	13.06	
20124	13.05	51.1	13.05	13.05	19.05	
50106	7.74	29.0	7.74	7.74	0	
50110	12.63	50.5	12.63	12.63	12.63	
50111	.62		0	0	0	
50114	.62	.70	0	0	0	
50118	2.62		2.62	0	0	
50113	.62		0	0	0	
50115	.88	4.15	0	0	0	
50108	.82	4.09	0	0	0	
50116	.85		0	0	0	
50112	.88		0	0	0	
50109	.93	2.05	0	0	0	
50107	1	2.12	0	0	0	
50100	.93	4.20	0	0	0	
10124	1		0	0	0	
10107	.97	3.09	0	0	0	
10104	.93	3.05	0	0	0	
10126	1.17		0	0	0	
35103	10.96		10.96	10.96	10.96	
35102	10.96		10.96	10.96	10.96	
35101	.96	4.23	0	0	0	
35104	1.96	3.08	0	0	0	
35100	1.96		0	0	0	
20120	.96		0	0	0	
20123	1.12		0	0	0	
20125	1.12		0	0	0	
20109	1.12		0	0	0	
20121	1.12		0	0	0	
20102	1.12	2.24	0	0	0	
20115	1.12	4.39	0	0	0	
20110	1.12	2.24	0	0	0	
20114	1.12	2.24	0	0	0	
35107	1.12	4.39	0	0	0	
35108	1.12	4.46	0	0	0	
35106	1.12	2.24	0	0	0	
10125	1.12	4.39	0	0	0	
35109	1.12	4.39	0	0	0	
35105	11.12		11.12	11.12	11.12	
20122	1.12		0	0	0	
50102	1.25		0	0	0	
50119	1.25		0	0	0	
50103	2.42		2.42	0	0	
50104	1.83		0	0	0	
50105	2.3		2.3	0	0	
50177	2.25		2.25	0	0	
10105	2.28		2.28	0	0	
5110	1.28	4.06	0	0	0	
5111	1.28	4.55	0	0	0	

10101	2.28	2.28	0	0	
10106	2.28	2.28	0	0	
10102	2.28	2.28	0	0	
10109	1.28 4.55	0	0	0	
10113	1.28 2.40	0	0	0	
5105	1.28 2.40	0	0	0	
5106	1.28	0	0	0	
5107	1.28	0	0	0	
5108	1.28	0	0	0	
5109	1.28 2.40	0	0	0	
20117	1.28	0	0	0	
10128	1.98	0	0	0	
10122	1.1	0	0	0	
10120	1.1	0	0	0	
10118	1.1	0	0	0	
10112	1.1 4.37	0	0	0	
10111	1.1	0	0	0	
10119	1.1 4.37	0	0	0	
10117	1.1	0	0	0	
10103	2.1	2.1	0	0	
35110	1.1 3.08	0	0	0	
20113	1.1	0	0	0	
10108	1.1	0	0	0	
10114	1.1	0	0	0	
20105	1.1	0	0	0	
10110	1.1	0	0	0	
10115	1.1	0	0	0	
20126	1.6	0	0	0	
20108	1.6	0	0	0	
5104	1.6 2.72	0	0	0	
20114	1.6	0	0	0	
20107	1.6	0	0	0	
		0	0	0	
		0	0	0	
		0	0	0	
		0	0	0	
		0	0	0	
		0	0	0	
		0			
TOTAL	314.51	238.26	217.45	202.61 +130	
COUNT	92	27	18	16 16	

12.6 hrs 20 hrs

2 FAIL

C102 5/6/82 1700

WAFER	CUM HRS	OVER 2
10100	4.31	4.31
10116	3.35	3.35
10121	3.4	3.4
10123	3.41	3.41
20100	3.75	3.75
20101	3.76	3.76
20103	4.52	4.52
20106	3.76	3.76
20112	3.83	3.83
20116	3.77	3.77
20118	3.77	3.77
20119	3.77	3.77
20124	3.76	3.76
50106	3.41	3.41
50110	3.34	3.34
50111	.62	0
50114	.62	0
50118	2.62	2.62
50113	.62	0
50115	.88	0
50108	.82	0
50116	.85	0
50112	.88	0
50109	.93	0
50107	1	0
50100	.93	0
10124	1	0
10107	.97	0
10104	.93	0
10126	1.17	0
35103	10.96	10.96
35102	10.96	10.96
35101	.96	0
35104	1.96	0
35100	1.96	0
20120	.96	0
20123	1.12	0
20125	1.12	0
20109	1.12	0
20121	1.12	0
20102	1.12	0
20115	1.12	0
20110	1.12	0
20114	1.12	0
35107	1.12	0
35108	1.12	0
35106	1.12	0
10125	1.12	0
35109	1.12	0
35105	11.12	11.12
20122	1.12	0
50102	1.25	0
50119	1.25	0
50103	2.42	2.42
50104	1.83	0
50105	2.3	2.3
50177	2.25	2.25
10105	2.28	2.28
5110	1.28	0
5111	1.28	0

10101	2.28	2.28
10106	2.28	2.28
10102	2.28	2.28
10109	1.28	0
10113	1.28	0
5105	1.28	0
5106	1.28	0
5107	1.28	0
5108	1.28	0
5109	1.28	0
20117	1.28	0
10128	1.98	0
10122	1.1	0
10120	1.1	0
10118	1.1	0
10112	1.1	0
10111	1.1	0
10119	1.1	0
10117	1.1	0
10103	2.1	2.1
35110	1.1	0
20113	1.1	0
10108	1.1	0
10114	1.1	0
20105	1.1	0
10110	1.1	0
10115	1.1	0
20126	1.6	0
20108	1.6	0
5104	1.6	0
20114	1.6	0
20107	1.6	0
		0
		0
		0
		0
		0
		0
		0
TOTAL	186.01	109.76
COUNT	92	

92 @ 2hrs | 27 @ 4hrs

3½ hrs

12 hrs

AGE	BALL RATE
1	.01
2	.04
4	.16
8	.48
16	1.6
32	3.2

1. TI tests so far. MTBF ≥ 1 day. 1440 passes × 3 (20' tape)
= 4320 passes

2. Assume 3 passes/day for 200 days/yr with 20' wafer.
600 passes × 1/3 minute = 200 minutes = 2hr 20 min

3. Exatron 1000pass magazine ad.

4 3 hrs operating with 200 hour MTBF.
$r = 1 - e^{-\lambda t} = 1 - e^{-3/200} = .0149 = 1.5\%$ return rate.

5.

	TAPE LENGTH	LOOP TIME	TIME FOR 40 K PASSES	PASSES AT 200 HOURS	250 Hou
**	5	4KBYTES 6	66.7	120K	150K
	10	8K 12	133.3	60K	75K
	15	18	200.0	40K	50K
*	20	16K 24	266.7	30K	37.5K
	35	42	466.7	17.1K	21.4K
	50	48K 60	666.7	12K	15K

2K

□ 2 2 2 8

□ 0 2 8 8

2 4 6 12 18 32K

50K

-MSG M#= 88692 FR=JAXS TO=ALCC SENT=10/01/82 09:50 AM
R#=403 ST=C DIV=039 CC=0814 BY=JAXS AT=10/01/82 09:50 AM

MEMORANDUM
OCTOBER 1, 1982

TO:	HERB SHANZER	NMS
	JIM NIEMEYER	JCF3
	LEONARD P. LACHMANN	JCF3
	C. B. WILSON	ALCC
	JIM ARNOLD	ALCC
	GARY FUTRELL	CPR
	GUN BHAKTA	JCF3
COPY:	KEDAR MORANKA	JCF3
FROM:	DINO TRINH	JCF3

SUBJECT: EXATRON TRIP REPORT ON SEPTEMBER 21 AND 22

ON 9/21, KEDAR AND I MET CLARENCE JONES, PROCESS MANAGER, BOB FONTANA, PRODUCTION MANAGER, BOTH FROM NCR, BOB HOWELL, CHAIRMAN, STEVE NAPOLI, PRODUCTION MANAGER, AND RYE SMITH, CONSULTANT ENGINEER FROM EXATRON. WE DISCUSSED THE WAFER MANUFACTURING PROCESS AND TOOLING REQUIREMENTS WITH NCR AND EXATRON. WE ALSO SHOWED SLIDE COVER SAMPLES AND FINALIZED ALL MOLD ADJUSTMENTS THAT WILL BE MADE TO EXATRON'S AND TI'S DRIVE MECHANISM.

KEDAR BROUGHT TI MOLDED WAFER PARTS AND HAD REQUESTED EXATRON TO ASSEMBLE THEM. THESE WAFERS WERE 50, 35, 25, AND 10 FEET LONG, WITH 50 OF EACH. THESE SAMPLES LATER WERE ULTRASONIC WELDED HERE AT TI.

THE NEXT DAY I ASSISTED BOB FONTANA AS HE RECORDED THE NECESSARY TIME REQUIRED TO PERFORM EACH OPERATION; I ALSO HELPED BOB AS HE PRACTICED EACH OPERATION. SINCE THIS WAS MY FIRST TIME AT EXATRON, I TOURED THE PLANT AND STUDIED THEIR PRODUCTION METHOD.

IF YOU HAVE ANY QUESTIONS, PLEASE FEEL FREE TO CONTACT ME AT 2164 OR KEDAR AT 2263.

REGARDS,
DINO TRINH/LL

M E M O R A N D U M
October 28, 1982

TO: Leonard P. Lachmann

COPY: Jim Arnold
C. B. Wilson 5884
Gary Futrell
Gerald Sledd

FROM: Kedar Morarka

SUBJECT: TRIP REPORT/VISIT TO NCR FOR DISCUSSION ON THE MICROTAPE WAFER

I visited with the NCR Corporation on October 21st and the 22nd in Dayton, Ohio, to discuss various mechanical design issues on the microtape wafers. I met with the following personnel:

0	Clarence L. Jones	Process Engineer
0	James Seybold	Manufacturing Engineer
0	David Blakely	Buyer for Magnetic Media
0	James Eggleston	Buyer for Tooling
0	Vern Ingram	Director of Purchasing
0	Bob Birch	Product Manager
0	John Reintjes	Manager of OEM Sales

The summary of our discussion is given below:

0 We will send NCR a written approval to use the parts we supplied. These parts have a few dimensions which are out of specification. None of these dimensions will affect the functionality of the wafer.

0 We need to approve the use of other parts (pinch roller, spring and pad) which NCR will be purchasing from Exatran's vendors for initial 50K production.

0 NCR plans to start building 1000 piece qualification units in early December in Dayton. We need a decision on what this qualification will consist of and when we can notify NCR of the results of our tests.

0 TI will supply pinch roller hub and slide cover (1000 each) to NCR for their qualification build by November 15, 1982.

0 TI will furnish a prototype certifier to NCR by mid November.

0 We will provide assembly drawings of: spring and pad, flange and hub.

0 NCR is extremely concerned about the source of back coated magnetic tape. The current supplier is very unreliable and they want us to work towards the development of other sources.

- NCR wants the shipping schedule on the initial 50K production.

- NCR is very hesitant in purchasing our tools. They prefer complete independence on the tooling issue.

- I have given my name to NCR as an engineer responsible for any mechanical changes in the wafer. All correspondence on drawing changes, however, will be through purchasing.

Regards,

K. M. Morarka

Kedar Morarka/LL

-MSG M#= 47914 FR=PRT TO=ALCC SENT=11/11/82 04:21 PM
R#=216 ST=C DIV=039 CC=0160 BY=PRT AT=11/11/82 04:21 PM
TO: JIM ARNOLD ALCC
KEDAR MARARKA JCF3
CR WILSON ALCC
RE: XYLOID PLASTICS
FR: GARY FUTRELL CPR

THE FOLLOWING QUOTATIONS WERE RECEIVED 11-10-82. PLEASE REVIEW AND IF ACCEPTABLE, WE WILL ARRANGE TRANSFER OF TOOLINGS.

PART NUMBER	DESC	QUOTE (EA)	
1048969	TOP CASE	10K	.16
		20K	.155
		30K	.15
		40K	.145
		60K	.14
		80K	.135
		100K	.13
		MAT'L FROM XYLOID/MAT'L FROM TI	
1048970	BTM CASE	10K	.18 .15
		20K	.17 .14
		30K	.165 .135
		40K	.16 .13
		60K	.155 .125
		80K	.15 .12
		100K	.145 .115
1048971/	HUB &	WITH NEW CORE ($1050.00)	
1048970	FLANGE	10K	.12
		20K	.11
		30K	.105
		40K	.104
		60K	.102
		80K	.101
		100K	.10
		TOOL "AS IS"	
		10K	.19
		20K	.185
		30K	.18
		40K	.178
		60K	.176
		80K	.174
		100K	.172
1048973	ROLLER HUB	10K	.034
		20K	.026
		30K	.024
		40K	.023
		60K	.022
		80K	.021
		100K	.020

PLEASE ADVISE OF YOUR DECISION ASAP.
REGARDS,
GARY FUTRELL, BUYER
PURCHASING-CPG TEXAS INSTRUMENTS INC D7ID32

M E M O R A N D U M
January 14, 1983

TO: Jim Niemeyer
Leonard P. Lachmann

COPY: Jim Arnold
C. B. Wilson
Gary Futrell

FROM: Kedar Morarka

SUBJECT: TRIP REPORT/VISIT TO ROCKFORD AUTOMATION

I visited Rockford Automation in Toronto on January 12, 1982; Gary Futrell, Purchasing, and Mike Mohit, VQE, were visiting there at the same time. I met with Bill Steinhagen, President; Walter Strilee, General Manager; and John Mackie, Plant Manager.

My objective was to make an evaluation of this vendor's technical capability in building wafer cartridges for us and to explain to them the critical assembly requirements of our product.

Rockford Automation designs and builds automatic assembly systems. They also manufacture audio cassettes for various companies, including AMPAX and CBS. At their Toronto plant, they have an integrated molding-assembly system for the high speed manufacturing of audio cassettes; they also assemble 8 - track cartridges on a low volume basis.

During our discussions, Bill Steinhogen admitted they will not be able to completely automate the wafer assembly. Winding, splicing and the threading of tape in the lower plastic case will have to be done manually; however, they will automate most of the remaining operations.

Rockford is capable of assembling wafers for us. They have a good in-house molding facitlity, which could be integrated with the assembly system--eliminating several handling operations; they have experience in building 8 - track cartridges which are very similar to our product. Rockford has the resources on technical expertise to do a satisfactory job for us.

Rockford Automation will submitt a written quote in the first week of February.

Regards,

Kedar Morarka

Kedar Morarka

KM/11

-MSG M#= 148383 FR=WVP TO=ALCC SENT=02/05/83 12:53 PM
R#=346 ST=C DIV=039 CC=0160 BY=WVP AT=02/05/83 12:53 PM
TO: JIM ARNOLD ALCC
CC: JIM BRYCE CPR
CB WILSON ALCC
FR: GARY FUTRELL CPR
RE: WAFERTAPE TAPE SOURCING

JIM, PER MY DISCUSSION WITH EXATRON ON 2-1-83, YOU SHOULD BE RECEIVING WAFERTAPE SAMPLES USING THE AUDIO MAGNETICS TAPE, WITHIN TWO WEEKS.

AUDIO MAGNETICS ALSO HAS EXPRESSED INTEREST IN SLITTING THE PRODUCT.

REGARDS,
GARY FUTRELL CPR

MEMORANDUM

09 February 1983

TO:	Jim Arnold	Jerry Robinson
	Randy Ahlfinger	Keith Danforth
	Wes Cox	Shaike Maoz
	Ilya Shimon	Mark Jackson
COPY:	Milton Kuser	C.B. Wilson
	Martin Cooper	
FROM:	Darrell Whitten	
SUBJECT:	WAFERTAPE MULTIFUNCTION IC SPEC	

Please review the attachments and plan to attend a meeting Monday at 1:00 - 2:00PM in Ryan Provenzano's conference room on the lower floor.

The purpose of the meeting will be to answer questions about the attached preleminary spec and system schematic for the Wafertape Cost Reduction. These have been reviewed with Exar, who are now engaged in the implementation of the approach. If you see any deficiencies or have any comments or questions, I would appreciate your help in identifying these now to avoid problems later.

If you cannot attend the meeting I still need your feedback in the form of written comments on the attachments. I will check with each of you for these prior to the meeting.

Thank you,

Darrell

TEXAS INSTRUMENTS INC.
CONSUMER PRODUCTS GROUP
PRELIMINARY SPECIFICATION
WAFERTAPE MULTIFUNCTION IC

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings
over Operating Free Air Range
(all voltages relative to ground)

Supply Voltages	MIN	MAX	UNITS
VCC	-.4	10.0	Volts
V analog	-.4	10.0	Volts
All Input Voltages (except LBI)	-0.4	Vcc+ 0.4	Volts
LBI Input Voltage - steady state	-0.4	Vcc+ 0.4	Volts
-10mS transient	-	Vcc+ 7.0	Volts
All Output Voltages	0	Vcc	Volts
Storage Temperature Range	-55	+150	°C
Electrostatic Discharge Immunity (Rs=4.7 K ohm; Cs=90pf)	2.5		KV

2. Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Operating Temperature Range	-10	25	+70	°C
Supply Voltages, Vcc	4.0	5.0	7.0	Volts
V analog (High)	3.8	4.8	6.8	Volts
(Low)	0		0.4	Volts
VIH, High Level Input (except LBI, $\overline{WP}$ SENSE, $\overline{BOT/EOT}$ SENSE)	1.5		VCC-2.5	Volts
VIL, Low Level Input (except LBI, $\overline{WP}$ SENSE, $\overline{BOT/EOT}$ SENSE)	-0.4		0.6	Volts
VOH-High Level Output	Vcc-0.5		Vcc	Volts
VOL-Low Level Output	0		0.3	Volts
Low Battery Indicator				
VSET	4.0		4.1	Volts
Hysteresis	0.2		0.3	Volts
Rin-input resistance	400		-	K ohm
IOH	100		-	uAmp
IOL	-100		-	uAmp
Power-up Reset				
Rin-input resistance	100	200	400	K ohm
Hysteresis	100		200	mVolt
IOH	100		-	uAmp
IOL	-100		-	uAmp

ELECTRICAL SPECIFICATIONS - Cont'd.

2. RECOMMENDED OPERATING CONDITIONS - Cont'd.

	MIN	NOM	MAX	UNIT
Write-Protect Sense				
Rin-input resistance	4.5			K ohm
IIH	25		100	uAmp
IOH	100		-	uAmp
IOL	-100		-	uAmp
Beginning Of Tape/End Of Tape Sense				
IIH	0.1		0.5	uAmp
IOH	100		-	uAmp
IOL	100		-	uAmp
Motor Drive Switch				
PSIC input				
IIL	-25		-100	uAmp
IIH	-15		-	uAmp
TMS 70C20 input				
IIL	-		-50	uAmp
IIH	-15		50	uAmp
MDS output				
IOH (Leakage; direct Connection to +5V)			.1	uAmp
VOH	(V Batt-0.2)			Volt
IOL (Sink current; direct connection to +5V)	2.5		5.0	mA
Slew-rate Control and Analog Supply Switch				
IIH	-15		-	uA
IIL	15		50	uA
IOH (Leakage;direct connection to +5V)			.1 -	uA
VOH	(Vcc-.2)			Volts
IOL (sink current; direct connection to +5V)	2.5		5.0	mA
TOL (Transition time of output current relative to input low)	-		5	uS

ELECTRICAL SPECIFICATIONS - Cont'd.

2. RECOMMENDED OPERATING CONDITIONS - Cont'd.

	MIN	NOM	MAX	UNIT
Write Circuitry				
Write Enable Input				
IIH	-15			uAmp
IIL	50		140	uAmp
Data Input				
IIH	-15			uAmp
IIL	50		140	uAmp
Data Out, $\overline{\text{Data Out}}$				
IOH, VOH GTOE* Vcc-0.2V	15			mA
IOL, VOL LTOE* 0.2V	15			mA
TOH (Transition to high)			.05	uS
TOL (Transition to low)			.05	uS
Read Circuitry				
Data In, $\overline{\text{Data In}}$ (differential input)	.5			mVpp
CMRR	70			dB
Raw Data Out				
IOH	-100		-	uAmp
IOL	100		-	uAmp
IIH	-15			uAmp
Clock Input				
IIH			100	uAmp
IIL			100	uAmp
Frequency	0.5	3.58	6.0	MHZ
Edge Detect Out				
IOH	-100			uAmp
IIH	-15			uAmp
IOL	100			uAmp
Baud Rate	4K	8K	12K	
Icc - (targets to be defined with breadboard)			8.0	mA
- STAND BY MODE				
- WRITE MODE				
- READ MODE				

* GTOE: Greater than or equal
LTOE: Less than or equal

M E M O R A N D U M
February 15, 1983

TO: Leonard P. Lachmann
Jim Niemeyer

COPY: Jim Arnold
C. B. Wilson

FROM: Kedar Morarka

SUBJECT: TRIP REPORT FOR VISIT TO EXATRON

Jim and I visited Exatron Corporation and Xyloid Plastics on February 7 and 8, 1983. Our objective was to discuss the quality of plastic parts with Xyloid and assembly process with Exatron, as they relate to the wafer compatibility problem.

Xyloid and Exatron has agreed to immediately take the following actions:

- Institute a quality control program to periodically check plastic parts as they are molded (at present they have no such checking).
- Maintain flatness of flange within drawing specification. (We are building a set of gauges to measure the plastic parts and will ship these to Exatron.)
- Polish bearing area in the B/C to eliminate rough spots.
- Eliminate gate extensions on the flange. These extensions are causing the flange to drag in the B/C.
- Repair B/C mold so that a proper welding spot is obtained on the bearing post.
- Adjust wafer case sonic welding fixture to eliminate excessive pressure on the flange bearing post.

Exatron is currently using tapes recorded at 90 degrees in a standard lab for adjusting the azimuth on the magnetic head. We will use these tapes to check our adjusting set up. We obtained several tapes which showed 100% cross compatibility on our drives.

We are continuing the tests to determine the effect of various variables on the compatibility.

Regards,
Kedar Morarka

KM/ll

-MSG M#= 30717 FR=ALC1 TO=ALCC SENT=04/04/83 11:49 AM
R#=028 ST=C DIV=039 CC=0815 BY=ALC1 AT=04/04/83 11:49 AM
TO: DARRELL WHITTEN.....ALCC

CC: MILTON KUSER.....MMK
GARY FUTRELL.....CPR
YUICHI MURANO.....ALCC VISITING
HERB SHANZER.....HMS
JIM ARNOLD.....ALCC

FM: C.B. WILSON.....ALCC

RE: POSSIBLE SOURCES FOR WAFER PRODUCTION IN JAPAN

MURANO-SAN HAS IDENTIFIED TWO POSSIBLE VENDORS FOR WAFER PRODUCTION IN JAPAN. IF YOU ARE READY FOR INITIAL QUOTATIONS, HE WILL BE GLAD TO HELP.

1. THIS SOURCE IS CONSIDERING THE BASIC BUSINESS DECISION AND WE SHOULD WAIT FOR THAT BEFORE REQUESTING A FORMAL QUOTATION.

HITACHI MAXCELL
3-3-1 GINZA, CHUOH KU, TOKYO
03-576-6221
MR. UNO, MR. KUNO

2. THIS SOURCE IS READY TO ACCEPT A REQUEST FOR QUOTATION.

TAIYO YUDEN K.K.
1-2-12 UENO, TAITOH KU, TOKYO
03-833-5441 03-835-4754 (FAX)
MR. YOSHIDA, MR. IIDA

BEST REGARDS,
C.B. WILSON.....ALCC/ALC1, M/S 5884, 806-796-3328

MEMORANDUM
05 April 1983

TO: Jim Bryce
Vic Szepe
Darrell Whitten

COPY: C.B. Wilson
Jim Arnold
Kedar Moraka
Chuck McKnight
Alan Daniels
Dan Gust
Darrel Watson
Ralph Balthrop
Gary Ragle
Chris Woolam

FROM: Gary Futrell/Mike Mohit

SUBJECT: ENTREPO (FORMERLY EXATRON) CC-40 WAFERTAPE REVIEW (3-29-83 AND 3-30-83

A meeting was held with Bob McDonald, President; Steve Napoli, Director of Manufacturing; Anthony Perez, Vice President of Operations and David Osborne, Vice President of Marketing and Sales to review the quality program necessary for Entrepo to become a fully qualified vendor, delivery of product and the possibility of a contractural relationship. The last qualification trip was made in July 1982. At that time Exatron did not appear to be able to meet our quality requirements and was not qualified. (July trip report attached).

To update everyone on the current status of Entrepo below is listed some general data:

1) Entrepo is now an independent operating entity producing drives and wafertapes as an OEM. Robert Howell of Exatron continues to hold a major portion of the company (30%), but does not have any management responsibility.
2) Exatron continues to operate as a mail order business under Robert Howell's direction.

3) The split of the company was to a large degree brought about in an attempt to remove the company from the showdown of the numerous lawsuits brought against Exatron and to attempt to build a better credit rating (a Dun and Bradstreet is attached for Exatron only. Entrepo was not listed by Dunn & Bradstreet).
4) Entrepo indicated that two investment companies will be making large capital investments in exchange for stock.
5) Entrepo has submitted a patent application for the sliding cover developed at TI. We may wish to insure we have a portion of the patent.
6) Anthony Perez and David Osborne have joined the company after the split was made. Perez and Osborne have their backgrounds in computer and communication industry.
7) Entrepo indicated they would like to license Rockford Automation as a second source for manufacturing and marketing the wafertape.
8) Entrepo is in process of hiring someone to take charge of engineering reporting to the president. David Osborne is currently acting in that capacity.

We worked with Entrepo's management for several hours to put together a quality program to meet TI's requirements.

Currently Entrepo is doing an incoming inspection on the plastic parts to a .65 AQL, unfortunately due to the tooling problems almost every lot is rejected. After the lots are rejected Entrepo generally will review each lot and go ahead and build product with all but the worst lots of products. After assembly, the parts are mechanically run-in (100%) for eight hours then tested for jitter and tape tension (100%) where some 50% of the product is lost.

They are in process of establishing a histogram for soft data error. So far they have been unable to establish a consistent data base. They are also building a computer controlled certification system with 1000 drives. They estimated completion by the end of May 1983.

Entrepo agreed that these procedures must be improved and agreed to the following program:

ACTION	DATE
1) Hire a director of quality	5-1-83
2) Prepare a QA manual	7-1-83
3) Review the proposed procedures with Texas Instruments personnel	7-15-83
4) Execute quality procedures to include:	starting 7-1-83 completion 1-1-84
A) Vendor selection guidelines	
B) Manufacturing process controls and documentation	
C) Reliability testing	
D) Source inspections when required	
E) Qualification procedures	

In view of the agreement to develop a quality program that will be acceptable to TI we recommend that Entrepo be given a temporary and conditional qualification with frequently quality inspections from TI, until 7/1/83. At that time new procedures and QRA lab test must be acceptable to TI to award full qualification status.

Next we spent some time reviewing Entrepo's production plans (see attachment). As you can see, Entrepo has plans in place to be able to supply 300K wafertapes per month by December of 1983.

Assuming that Entrepo can execute their program given their current cash flow problems then they should have sufficient capacity when combined with Rockford Automation to meet demand on the new product if TI's product becomes a huge success. Entrepo is preparing a schedule that will be available next week showing the short term support for our current orders. This plan requires TI to finish the label artwork, release the final specification, and resolve the cover issue. Entrepo will supply plastics and tape to Rockford in order to allow Rockford to build some product in advance of their tooling.

One issue resolved is TI's responsibility for the tape procured by NCR. Entrepo, unknown to anyone at TI, has used most of this tape for their product and has made arrangements with NCR to pay for the material.

The 500 tapes requested by Engineering will ship w/o 4-3-83 although the 50' tapes are in jeopardy due to a jitter problem that continues to plague Entrepo on the longer lengths.

Based on the fact we were meeting spec on tapes shorter than 50' & didn't have a way to test tapes - we might have been longer than we thought CB

We briefly reviewed a contractural relationship. Entrepo was satisfied with TI's standard contract with the following exceptions and/or modifications:

1) TI will not have to forecast an annual quantity to Entrepo.
2) Entrepo cannot meet Rockfords pricing for a few months but will reduce the current prices (see attached quote) and agrees to renegotiate prices on September 1, 1983.
3) Due to Entrepo cash flow problems they cannot agree to a 90 day unscheduled provision, but will agree to a 60 day provision.
4) They can supply a certification of compliance but will be unable to provide individual lot test data this year.
5) They would like to have payment terms of 2/10 for 50% of the product and net 60 for the balance.

Based upon this review and considering the financial problems Entrepo has we strongly recommend that TI purchase as many wafers as necessary to cover our needs through September 1983 and bring these into stock as soon as Entrepo can provide them. This will insure product until Rockford is on board in the event that Entrepo does not survive.

Regards,

Gary Futrell/Mike Mohit

attachments:

1) Exatron D&B
2) Assembly and Tooling forecast
3) Latest price quotation
4) Exatron July qualification trip report

-MSG M#= 114706 FR=ALCC TO=ALCC SENT=10/14/83 06:55 PM
R#=043 ST=C DIV=039 CC=0815 BY=JMPE AT=10/06/83 09:09 PM
TO: C B WILSON - ECJ
TO: JIM ARNORD - ALCC
CC: I KOIKE - AKRI
CC: Y.UCHIDA / S SATO - FEJP

RE: L11001 REPLY FOR YOUR TELEPHONE CALL

((DEVICE STATUS))
GATE CODE NEME OF C20A (PREVIOUSLLY CALLING L11001) IS L71000S.
2 LOTS OF L71000S PARTS ARE RUNNING AT OUR FRONT-END,AND SHIPPING
COMMITMENT ARE AS FOLLOWS.

SLICE OUT	10/26
F.G OUT	11/1
SHIPPING	11/2

PROBABLY SAME AS C71003 SHIPPING WHICH PARTS WERE PREVIOUSLLY CALLING
THE GATE CODE C11006.

((FUNCTION DIFFERENCE BETWEEN C20A AND C20))

	C20	C20A
- PRIORITY OF INT CLR AND EN	X	O
- ILLEGAL RELEASE OF IDLE STATE	X	O

X ------ NOT CORRECT
O ------ CORRECT

= DETAILS OF PRIORITY OF INT CLR AND EN =
I/O CONTROL REGISTOR SET "1 1" (CLR/EN AT THE SAME TIME),IN THIS CASE,
IF INT INPUT IS ALREADY LATCHED AND INT FLG IS ACTIVE,IT IS ORDINARY
MANNER TO CLEAR INT FLG PRIOR TO ACCEPT INTERRUPT WITH EN FLG="1"
AND DISABLE INTERRUPT ACTION.
HOWEVER C20 WILL OCCASIONALLY PRIORITIZE EN BIT AND ACTIVE INTERRUPT
DUE TO TIMING SKEW.
= DETAILS OF ILLEGAL RELEASE OF IDLE STATE =
WHEN CPU EXECUTES IDLE INSTRUCTION,CPU ENTERS INTO POWER SAVE MODE BY
CLOCKHALT.THE RELEASE OF THIS STATE WILL BE DONE BY INT INPUT.
IF THE INT INPUT NOT INFLUENCED BY INT BIT AT STATUS REGISTOR OR INT EN
BIT IS USED,IT WILL CREATE THE PROBLEM.
FOR EXAMPLE,AT THE STATE THAT INT3 IS DISABLE BY EN BIT OF I/O CONTROL
REGISTOR,INT3 INPUT BECOMES ACTIVE FOR IDLE RELEASE,CPU NEVER ENTERS
TO INT3 ROUTINE WHILE CLOCK KEEPS RUNNING.WHEN INT IS DISABLED BY INT
BIT OF STATUS REGISTOR,THE SAME THING MAY HAPPEN.

BEST REGARDS.
RYOJI YONEMOTO FEJP

MSG 39 815 ECJ FEJP CJP ALCC
TO: RYOJI YONEMOTO.....FEJP

CC: YUICHI MURANO.....ECJ
CHUCK BRANSON.....ALCC
DARRELL WHITTEN.....HEXB

FM: C.B. WILSON.....ALC1

RE: 70C20A

WE ARE STILL CONTINUING TO TRY TO FIND OUT WHAT THE REAL PROBLEM IS WITH THE SOFTWARE WE HAVE IN THE 70C20 FOR THE WAFERTAPE (GATE CODE L11001). AS I MENTIONED TO YOU WHEN I WAS IN JAPAN, WE GET A FAILURE USING THE ACTUAL PART THAT WE DON'T SEEM TO GET WHEN USING THE AMPL. SINCE THAT TIME WE HAVE FOUND A SERIOUS PROBLEM WITH OUR MACHINE LEVEL CODE, BUT THAT ERROR DOES NOT EXPLAIN WHY THE AMPL WORKS AND WE BELIEVE A SEPARATE PROBLEM IS RESPONSIBLE FOR THE ACTUAL FAILURE.

IN SEARCHING FOR THIS SECOND FAILURE, WE HAVE BEEN TESTING SOME CODE (WHICH DOES NOT USE THE MICROCODED INSTRUCTIONS OF THE L11001) ON THE 70C20A. WE ARE APPARENTLY SEEING A SUPRIZING FAILURE ON THESE 70C20A PARTS. THE FAILURE APPEARS TO BE THAT THE PART IS NOT ABLE TO BE INTERRUPTED OUT OF AN IDLE STATE WITH AN INTERRUPT 2 FROM THE TIMER. SPECIFICALLY, WE HAVE THE FOLLOWING CODE:

```
        MOVP    %START,TIMER      START = >A0, TIMER  = >03
        MOVP    %I2CS,IOCNTL      I2CS  = >4C, IOCNTL = >00
        EINT
        CLR B
        IDLE
        BTJO %SETBIT,B,RSYNC8
```

THE FAILURE WE BELIEVE WE ARE SEEING IS THAT THE PART DOES NOT EVER COME OUT OF THE IDLE INSTRUCTION WHEN THIS IS EXECUTED. I AM NOT ABSOLUTELY SURE OF THIS BECAUSE WE HAVE ONLY A COUPLE OF 70C20A PARTS OVER HERE AND THIS WAS NOTICED LATE FRIDAY FOR THE FIRST TIME. WE HAVE SOME OTHER 70C20A PARTS OVER IN THE QUAL LAB WHICH I WILL GET BACK MONDAY AND WE WILL VERIFY AGAIN WITH MORE PARTS AND MAKE ABSOLUTELY SURE WE ARE NOT SEEING SOMETHING ELSE. IT IS DIFFICULT FOR ME TO IMAGINE THAT THE PART ACTUALLY HAS THIS TYPE OF FAILURE, BUT I WANTED TO ADVISE YOU OF OUR INFORMATION AND GET YOUR COMMENT.

I AM STILL INTERESTED VERY MUCH IN THE PROGRESS OF THE LOTS OF WAFERTAPE CODE ON THE 70C20A (GATE CODE L71000S). DO YOU HAVE ANY CHANGE TO THE 11/2 SHIPPING DATE FOR THESE PARTS?

BEST REGARDS,
C.B. WILSON.....ALCC/ALC1

```
     F504  02
1067 F505  92          MOVP   B,TIME                  2/3 bit timer
     F506  02
1068 F507  D5          CLR    CHKSUM                  set chksum to 0
     F508  31
1069 F509  D5          CLR    CHKSUM-1
     F50A  30
1070               *     COPY   ALC.JCF.STRINGY.SRC.OLDRINT   old microcode i
1071 F50B  72          MOV    %RBITDT/256,INT2V-1
     F50C  F7
     F50D  33
1072 F50E  72          MOV    %RBITDT-(256*(RBITDT/256)),INT2V
     F50F  8A
     F510  34
1073               *     MOV    %RDBIT1,INT2            set up INT2 opcode
1074               *     MOV    %RDBIT2,INT2+1          set up INT2 parameter
1075               *     CLR    INT2+2                  set up INT2 parameter
1076 F511  A2          MOVP   %START,TIMER            start 2/3 bit timer
     F512  A0
     F513  03
1077 F514  A2          MOVP   %I2CS,IOCNTL            select & clear INT2
     F515  4C
     F516  00
1078 F517  05          EINT                           reinterruptidity
1079 F518  C5          CLR    B                       TEST
1080 F519  01          IDLE                           TEST
1081 F51A  56          BTJO   %SETBIT,B,RSYNC8        test for 1
     F51B  08
     F51C  05
1082 F51D  C5  RSYNC7  CLR    B                       TEST
1083 F51E  01          IDLE                           TEST
1084 F51F  57          BTJZ   %SETBIT,B,RSYNC9        test for 0
     F520  08
     F521  07
1085 F522  C5  RSYNC8  CLR    B                       TEST
1086 F523  01          IDLE                           TEST
1087 F524  57          BTJZ   %SETBIT,B,RSYNC7        test for 0
     F525  08
     F526  F6
1088 F527  E0  RESINK  JMP    RESYNC                  if two 1's in a row
     F528  89
1089               * test for 2 more Os
1090 F529  C5  RSYNC9  CLR    B                       TEST
1091 F52A  01          IDLE                           TEST
1092 F52B  56          BTJO   %SETBIT,B,RESINK        test for 1
     F52C  08
     F52D  F9
1093 F52E  C5          CLR    B                       TEST
1094 F52F  01          IDLE                           TEST
1095 F530  56          BTJO   %SETBIT,B,RESINK        test for 1
     F531  08
     F532  F4
1096 F533  72          MOV    %4,BITCON               bitcon will have been 1
     F534  04
     F535  02
1097 F536  EE          TRAP   BITBBA                  wait end of nibble (spac
1098               * register A will have been swapped (spacer only)
```

```
0204                    *---------------------------------------------------------
0205                    * wafer drive control constant equates
0206    00FF    INITDR  EQU     >FF                     initialize drive
0207    0001    INITWF  EQU     >01                     initialize wafer ddr
0208    00F3    MT      EQU     >F3                     turn on motor & sensor
0209    0008    MTBAR   EQU     >08                     turn off motor
0210    00F1    MTWE    EQU     >F1                     turn on motor, WE & sens
0211    0000    RENITW  EQU     >00                     tri-state DO
0212    00FB    SN      EQU     >FB                     turn on EOT/BOT sensor
0213    00FB    STOP    EQU     >FB                     turn off drive except se
0214    00F9    WE      EQU     >F9                     turn on WE & sensor
0215                    * wafer test contant equates
0216    0040    BATTRY  EQU     >40                     bit-test for battery-lev
0217    0002    EOTTST  EQU     >02                     bit-test for EOT
0218    0080    INPUT   EQU     >80                     bit-test for input data
0219    0004    WP      EQU     >04                     bit-test for WP
0220                    * wafer data consatnt equates
0221    0001    INVBIT  EQU     >01                     wafer-write invert
0222    0008    SETBIT  EQU     >08                     store a "1" bit
0223                    *---------------------------------------------------------
0224                    * bus control constant equates
0225    0001    DROP    EQU     >01                     drop HSK bit
0226    0000    HSKSET  EQU     >00                     let HSK float
0227    0004    INHIB   EQU     >04                     inhibit IBC
0228    0001    RELEAS  EQU     >01                     release-HSK bit
0229                    * bus test constant equates
0230    0001    HSK     EQU     >01                     bus ready bit-test
0231    0008    IRQ     EQU     >08                     bus data ready bit-test
0232    0002    BAV     EQU     >02                     BAV active test
0233                    *---------------------------------------------------------
0234                            COPY    ALC.JCF.STRINGY.SRC.MHZ358
B0001                   * timer constant equates
B0002   000D    BITIME  EQU     >0D     3.58MHz,8KBaud  data half-bit time
B0003   0020    HALT    EQU     >20                     stop timer
B0004   00C0    HRANGE  EQU     >C0     3.58MHz         high time/low freq cutof
B0005   0038    LRANGE  EQU     >38     3.58MHz         low time/high freq cutof
B0006   00BF    MAX     EQU     >BF                     max timer, no sleep
B0007   0006    ORANGE  EQU     >06     3.58MHz         bit to bit compare
B0008   0000    SLEEP   EQU     >00                     sleep mode
B0009   00A0    START   EQU     >A0                     timer-start bit
B0010                   * software loop constants
B0011   0067    BOSTIM  EQU     >67     3.58MHz         wait valid sync (150 ms)
B0012   00B6    BOTIME  EQU     >B6     3.58MHz         BOT past head (300 ms)
0235                    *       COPY    ALC.JCF.STRINGY.SRC.MHZ5
0236                    *---------------------------------------------------------
0237                    *       COPY    ALC.JCF.STRINGY.SRC.FE
0238                            COPY    ALC.JCF.STRINGY.SRC.PE
C0001                   * interrupt select & clear constant equates
C0002   0043    I1CS    EQU     >43                     clear and select INT1
C0003   006A    I123C   EQU     >6A                     clear INT1,2&3 flags
C0004   0048    I2C     EQU     >48                     clear INT2 flag
C0005   004C    I2CS    EQU     >4C                     clear and select INT2
C0006   0004    I2S     EQU     >04                     test INT2 select bit
C0007   0068    I23C    EQU     >68                     clear INT2&3 flags
C0008   007C    I23CS   EQU     >7C                     clear and select INT2&3
C0009   0060    I3C     EQU     >60                     clear INT3 flag
C0010   0070    I3CS    EQU     >70                     clear and select INT3
```

101 DESIGN VERIFICATION TEST (DVT) RESULTS

entrepo

1/84

PODUCTION:

The 101 DVT had three major areas namely ambient functional te ting, environmental testing and reliability. At the time of writing the ambient functional is complete, the environmental 90% complete and the reliability test is ongoing. This note summarizes the results to date. A comprehensive report with full reduced data will be generated at the completion of the reliability portion of the test.

SUMMARY

AMBIENT FUNCTIONAL:

The five drive/five wafer interchange tests in laboratory ambient were run beginning 1/28/84, 2/24/84 and 3/3/84. The first test demonstrated an average error rate of less than 1 error per 10 exp.9 bits transferred. The second test had a wafer that miss-tracked badly. After removing this wafer from the data the result was an error rate 3 errors per 10 exp. 8 bits transferred. The final test also had a rogue wafer that miss-tracked. After removal of this wafer from the test the error rate was less than 1 error in 10 exp.9 bits transferred. The conclusion is the an interchange error rate of better than 1 in 10 exp.8 bits transferred has been demonstrated. The wafer tracking problem was traced to a lack of tension in the wafers due to tolerance problems in assembly of the drag pad and also missaligned head loading pads. The wafer design is being reviewed to improve the manufacturability of both pads. A regression test of the ambient functional test will be run when wafers from the final process are available.

A change to 12 ips was made to reduce the recording density to improve the azimuth tolerance of the head adjustment and drift during life. A two drive, two wafer interchange test was carried out using one Audio K tape and one PD Magnetics tape. The test was continued to over 20,000 passes of each tape. The average error rate of both tapes, over four times rated life was 1.5 errors per 10 exp.9 bits transferred.

SIGNAL LOSS RESULTS:

Signal amplitudes were logged throughout all tests and the reduction over time noted. The amplitude of the signal was found to reduce over the first 1000 passes after which time it reaches a steady state. The reduction in the signal is less for tapes using thin media. The tests used two tape types namely a 180 μ" media and a 120 μ" media. The 2F reduction for 180 μ" media averaged 30% and for the 120 μ" the average reduction was 16%. During this test, two drives reached 300 power on hours without failure.

WORST CASE AZIMUTH BUDGETS:

A test was run to determine the worst case azimuth alignment that would allow a soft error rate of better than 1 in 10 exp.8 bits transferred. Two wafers were selected with excellent tracking to remove this variable from the experiment. Two drives were adjusted to 0 azimuth using a signal peaking procedure. The two tapes were formatted and interchanged between drives. An error handling of 10 exp.7 bits was carried out and the azimuth adjusted away from nominal in 3 minute increments. This was repeated until the error rate became catostrophic (> 100 errors in 10 exp.7 bits). The azimuth at which this occurred was determined to be 21 minutes total. By comparison with earlier tests the total missalignment for an error rate of 1 in 10 exp.8 is approximately 6 minutes worse than for an error rate of 1 in 10 exp.7. Thus the total azimuth budget was determined to be 18' or +/- 9' from nominal. The budget is shared by four factors namely:

1. Wafer insertion repeatability.
2. Tape tracking within the wafer.
3. Initial head azimuth alignment.
4. Azimuth drift over life.

The partitioning of these budgets is as follows:

1. +/- 1`
2. +/- 2`
3. +/- 2`
4. +/- 4'

TAPE LIFE:

Mechanical life tests of the wafers has determined that catastrophic mechanical failure occurrs at > 30,000 passes typically. A test was run in which two wafers were run continuously performing data handling and the error rate noted. One wafer (20 ft.) ran for 27,000 passes before the error rate reduced to worse than 1 in 10 exp.8 and the other (35 ft.) was removed from the test at 20,000 passes before its error rate had reduced below spec. Further tape life tests are now underway with the life at these lengths. A tentitive conclusion is that the expected life of 20 and 35 ft. tapes greatly exceeds the 5000 passes specified. The average error rate measured throughout this test (which transferred a total of 17,000 megabits) was 3 errors in 10 exp.9 bits.

WRITE OVER:

The remnant 1F signal after overwriting a 2F pattern was measured for all tapes used in the test. Two tape types were used namely a media thickness of 180 u" and a media thickness of 120 u". As expected the thick media demonstrated worse writeover than the thin media. Average results are:

180 u" media writeover	24 dB
120 u" media writeover	30 dB

The conclusion is that while both are adequate the 120 u" media should yield lower error rates. Entrepo has chosen to standardize on the 120 u" media.

ENVIRONMENTAL TESTING DISCUSSION:

The environmental tests run so far have consisted of recording at various temperatures and running error handling tests at different temperatures over the specified range. A full interchange test has not yet been run. The specification calls for operation over a 10 degree C to 45 degree C range. Environmental testing has been carried out between 5 degrees C and 50 degrees C to gain additional confidence at the extremes of the specification.

Initial tests showed that the wafer tracking problems become more severe as the temperature was varied. This was attributed to friction changes within the wafer. The first tooled wafers were found to have little or no angle on the guide conics with the result that the tape could switch between running against the upper guides to the bottom of the conics in a random fashion as the friction changed. The problem was corrected by 3/1/84 and the environmental test restarted.

No electronic failures have occurred in either high or low temperature testing with in excess of 200 hours completed at 50 degrees C and in excess of 200 hours at 5 degrees C.

ERROR HANDLING OVER TEMPERATURE:

A wafer was formatted at 25 degrees C and a 10 exp.7 bit test run to verify data integrity. No errors occurred. The temperature was lowered to 5 degrees C and a two 10 exp.9 bits tests completed without error. The drive was raised to 50 degrees C while a 10 exp.9 bit test was being run. One error occurred during the transition to 50 degrees C. A further 10 exp.9 bit test was run at 50 degrees C during which time 3 errors occurred. The average error rate during the test is 1.2 errors in 10 exp.9 bits. The test will continue to the life of the wafer.

DRIVE AZIMUTH VARIATION WITH TEMPERATURE:

To evaluate azimuth variations with temperature, three drives were aligned to a master tape at room temperature and cycled to 0 degrees C, back up to 50 degrees C and back to room temperature. At each temperature extreme the azimuth was measured by measurements of the signal loss from the master tape. A worst case total of 7' was recorded, while the total variation is within the allowed budget it should be noted that the adjustment screws did not have locking compound applied. The test will be re-run when the first production batch of drives is available.

MOTOR CURRENT OVER TEMPERATURE:

An experiment was run to determine the variation of motor current with temperature. 12 wafers were used and the temperature was varied between 5 degrees C and 45 degrees C.

The conclusions reached are:

1. Tire and motor friction account for 60-70% of total motor current.
2. Tape drag accounts for 30-40% of total motor current.
3. Motor current decreases 5-10% when the temperature increases from 25 degrees C to 45 degrees C.
4. Motor current increases 20-30% when the temperature drops from 25 degrees C to 5 degrees C.

MOTOR SPEED VARIATIONS WITH TIME (101 OPEN LOOP):

The motor speed was monitored when driving 20 ft. and 50 ft. wafers at both 5 degrees C and 45 degrees C. Two variations were measured:

1. Short Term - Variations within 1 second.
2. Long Term - Variations within 2 minutes.

Results obtained across a sample of 12 wafers are:

45 degrees C	Short Term	= +/- .7%
	Long Term	= +/- 2.0%
5 degrees C	Short Term	= +/- 1.2%
	Long Term	= +/- 3%

The conclusion is that the motor speed remains with the specified +/- 4% over temperature, with differing wafer lengths and within the time to make at least one tape pass.

MULTIPLE INSERTION TESTS:

A test was run to determine the wear, if any, on the wafer hold-in buttons. A simple robot was built (by Astec Hong Kong) to carry out the test. The hold-in force was measured and 50,000 insections were made. The hold-in force was checked periodically. At the conclusion of the test the hold-in force remained in excess of 200 grams. An inspection of the buttons determined that the button wear was minimal and that they remained dimensionally within spec. A subjective observation was made that the "feel" of the insertion improved as the buttons became polished by multiple insertions.

INDEX LIFE TESTS:

Initial tape index sense strips were fabricated using a conductive aluminized mylar strip. In the experiments performed to date index failures occurred at < 2000 passes using this material. A new material using a combination of silver and chrome is in test at this time with the following results:

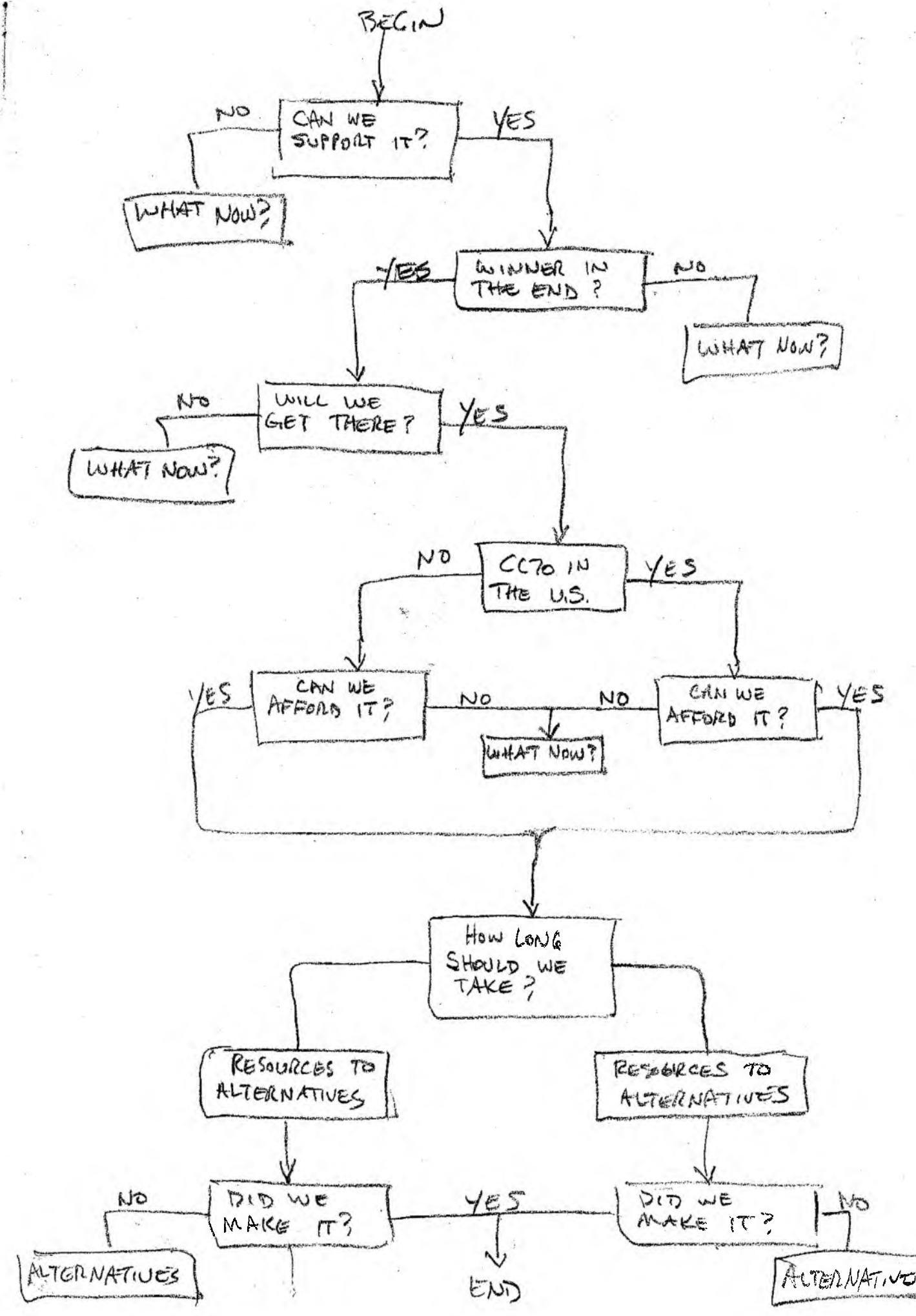
TAPE 1	20 ft.	19500 PASSES	NO FAILURES
TAPE 2	20 ft.	12000 PASSES	NO FAILURES
TAPE 3	20 ft.	4260 PASSES	MECHANICAL FAILURE
TAPE 4	20 ft.	7600 PASSES	NO FAILURES
TAPE 5	20 ft.	7700 PASSES	NO FAILURES
TAPE 6	20 ft.	16600 PASSES	NO FAILURES

The test is continuing.

CONCLUSIONS:

1. The M101 transport has demonstrated interchange capability better than specified.
2. The M101 electronics performs to specifications over the temperature range.
3. Azimuth drift is marginally within specification limits and will be tested further.
4. Motor speed variations are within specified limits.
5. The transport and wafer are capable of operating over the temperature range but conclusive testing of interchange has not yet been completed.
6. Tape life has been demonstrated on 20 ft. and 30 ft. wafers of in excess of 20,000 passes.
7. Drive testing has reached 300 power on hours without failure.
8. Multiple insertions of a wafer have demonstrated 50,000 insertions without losing wafer retention.
9. Index wear life of in excess of 19,000 passes has been demonstrated.

Agfa-Philips


BEGIN
CAN WE SUPPORT IT?
NO
YES
WHAT NOW?
WINNER IN THE END?
YES
NO
WHAT NOW?
WILL WE GET THERE?
NO
YES
WHAT NOW?
CCTO IN THE U.S.
NO
YES
CAN WE AFFORD IT?
YES
NO
WHAT NOW?
CAN WE AFFORD IT?
NO
YES
How LONG SHOULD WE TAKE?
RESOURCES TO ALTERNATIVES
RESOURCES TO ALTERNATIVES
DID WE MAKE IT?
NO
YES
ALTERNATIVES
END
DID WE MAKE IT?
NO
ALTERNATIVES

WAFERTAPE REVIEW

ISSUES

1. Future cost:

   a. In lost sales and customer attitude with non shipment.

   b. In OST dollars.

   c. In written off material we can't recover.

   d. In critical resources.

   e. In resources we don't have.

   f. By not being able to meet our business plan with software sales and applications.

10/28/83, CBW, 39-289

1. What should we do if we stop the wafertape?

   a. Role of audio cassette probably limited to retail channel and the low price buyer (students, etc)

   b. Accelerate a disk program? What are the needs for battery disk versus the existing mini floppy disk?

   c. What do we have the people do who are working on the wafertape now?

   d. If we do the CC70 offshore, we do have some resources that can reasonably be freed up to work on wafertape or new products.

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1. How close are we?

   a. The software errors were definitely significant and directly correlated to the compatability failures.

   b. All the known software errors are corrected now and we can begin testing revised software next week as well as start new processors at any time.

   c. The mechanical configuration we have now seems very likely to be good enough, given the software changes. The Pioneer improvements seem feasible to give us significantly more margin in the future.

   d. The wafer problems (on the manufacturing side) are really not new problems at all, just problems that haven't had sufficient attention.

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1. Will we be perceived as a winner with this technology if we are the only ones to use it?

2. Will we be able to afford the continuing support for this mass storage system? (duplication, wafer production, distribution of media, etc)

10/28/83, CBW, 39-289

C.B.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 10508 • LUBBOCK, TEXAS 79408
U.S. Consumer Products Group

2 December 1983

Mr. Takayuki Hashimoto
Pioneer Ansaphone
70-1, Hayashi 2-Chome
Tokyo, Japan

Dear Mr. Hashimoto:

On behalf of Texas Instruments, I want to thank you and your company for your work on our wafertape peripheral program. Due to our withdrawal from the Home Computer market and factors associated with the technology and supply of wafertape cartridges, we have discontinued development of this peripheral. This unfortunate action had to be taken at a time, as you know, when your company had begun to demonstrate some very favorable improvements to the drive mechanism. We feel that you gave us very outstanding support for this program and we appreciate your efforts.

We apologize for any inconvenience caused by this, but would like to maintain the good relationship we have established and hope for your cooperation with us in the future.

Sincerely,

C.B. WILSON
Engineering Manager
Compact Computer Programs
Consumer Products Group

Fifty Years of Innovation