Geneve II V1.0

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Abstract

This document details the internals of the Geneve II design with the aim to allow access its full potential.

Introduction

The Geneve II is an evolution of the TI-99/4A and Myarc Geneve home computer. It is based on the 9995 16 bit CPU and retains the features of the TI-99/4A and Geneve. In doing so it will be almost 100% software compatable.

The driving force behind the Geneve II was the challenge. If it can be done then why not do it. It was intended to complete this back in 2008 but with work and family it was not to be. Presently about 2500 hours have been put into this project since it concept. Hopefully it will be complete in the next year or two.

The Geneve II will have the ability to be situated in the PEB but also it can be attached inside a PC case and operated from the disk drive power supply.

The design has been targeted for the Cyclone III FPGA and will take two of these devices – partially due to the VHDL design size and partially due to the number of pins required.

Architecture

The maintain compatability there are no significant architectural changes from the top level. However, in the detail there are some extra registers and the 9995 has a 16 bit interface to allow quicker operation.

On the PCB there are two FPGAs.

The one on the left contains the PLL to multiply up the xtal frequency to allow quicker operation, TMS9995 with full 16 bit connection, FPU100 to allow full floating point at hardware speed in parallel to the TMS9995, bespoke Dram controller for the external memory, memory mapper which deals with the memory pages along with the mode register and floating point registers and incorporates a Gramulator for TI-99/4A software. The memory mapper also has the EEPROM and scratch pad ram incorporated. The memory mapper also deals with decoding of RTC, keyboard etc. It deals with wait state control and it also performs the PEB interface no matter what clock speed or wait states have been requested. The final job of this FPGA is to interface with two SD cards to allow data to be read and stored.

The FPGA on the right deals with the 9938 and gives it a VGA output, PS2 mouse interface, PS2 keyboard interface, VRAM interface, IDE connector interface, it talks to the ethernet chip at the top of the PCB and it will contain the 9901 to allow joysticks.

The PCB has all the voltags level shifting required for direct interface to the PEB.

Memory Map 99/4A

When 99/4A mode is selected then the system has the following memory mapping :

99/4A MODE	
0000 1FFF	Operating System
2000 3FFF	8K Expansion RAM
4000 5FFF	I/O Operating System
6000 7FFF	8/16K Cartridge ROM
8000 8007	8 Memory Page Mapping Regs
8008 800F	Keyboard
8010 801F	Clock
8020 83FF	PAD RAM
8400 85CF	Sound
85D0 85DF	FPU100
85E0 85EF	VDP Waits CPU Waits
85F0 85FF	8 Memory Book Mapping Regs
8600 87FF	External Bus
8800 8FFF	VDP
9000 97FF	Speech
9800 9FFF	GROM
A000 FFFF	24K Expansion RAM

An explaination of the extra registers, not in the Geneve, will be given later.

Memory Map 9640

When 9640 mode is selected then the system has the following memory mapping :

9640 MODE	
0000 03FF	1K Operating System
0400 EFFF	Memory Expansion
F000 F0FF	PAD RAM
F100 F107	Keyboard
F108 F10F	VDP
F110 F11F	16 Memory Page/Book Regs
F120 F123	Sound
F124 F12D	FPU100
F12E F12F	VDP Waits CPU Waits
F130 F13F	Clock
F140 FFF9	Memory Expansion
FFFA FFFF	RAM

An explaination of the extra registers, not in the Geneve, will be given later.

Extra Registers

ExReg89, ExRegAB, ExRegCD and ExRegEF are book registers which provide the extra address decoding for registers Reg01, Reg23, Reg45 and Reg67. The latter four registers are the page registers that exist on the Geneve and the ExReg registers select which book of pages are to be used.

Each ExReg has 5 bits set aside. This allows 32 times the memory capacity of the Geneve. These registers are in the book mapping locations.

FPU_AMSW and FPU_ALSW are the most and least significant words making up a 32 bit number for the floating point unit. FPU_BMSW and FPU_BLSW are the most and least significant words making up the other 32 bit number for the floating point unit. FPU_CTRL selects the mode and initiates the sequence. The FPU runs conpletely in parallel to the TMS9995 so the can be performing simultanious calculations. These registers are in the FPU100 locations.

VDPwaits and CPUwaits are registers which allow the number of wait states for the 9938 and number of wait states for the TMS9995. These can be set to 0 for maximum speed even when using the external memory in 16 bit mode. However, it should be noted then when the gramulator is operating then the CPU will default to at least 1 wait state to allow extra time for the Gramulator operation.

Instruction Set

	OC	OC	OC	B	TD	TD	D	D	D	D	TS	TS	S	S	S	S
A	1	0	1	0												
AB	1	0	1	1												
C	1	0	0	0												
CB	1	0	0	1									Format			
S	0	1	1	0									I			
SB	0	1	1	1												
SOC	1	1	1	0												
SOCB	1	1	1	1												
SZC	0	1	0	0												
SZCB	0	1	0	1												
MOV	1	1	0	0												
MOVB	1	1	0	1												

	OC	OC	OC	OC	OC	OC	D	D	D	D	TS	TS	S	S	S	S
COC	0	0	1	0	0	0										
CZC	0	0	1	0	0	1							Format			
XOR	0	0	1	0	1	0							III			
MPY	0	0	1	1	1	0										
DIV	0	0	1	1	1	1										

	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	TS	TS	S	S	S	S
MPYS	0	0	0	0	0	0	0	1	1	1			Format			
DIVS	0	0	0	0	0	0	0	1	1	0			IX			

	OC	OC	OC	OC	OC	OC	D	D	D	D	TS	TS	S	S	S	S
XOP	0	0	1	0	1	1							IX			

	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	TS	TS	S	S	S	S
B	0	0	0	0	0	1	0	0	0	1						
BL	0	0	0	0	0	1	1	0	1	0						
BLWP	0	0	0	0	0	1	0	0	0	0						
CLR	0	0	0	0	0	1	0	0	1	1						
SETO	0	0	0	0	0	1	1	1	0	0						
INV	0	0	0	0	0	1	0	1	0	1			Format			
NEG	0	0	0	0	0	1	0	1	0	0			VI			
ABS	0	0	0	0	0	1	1	1	0	1						
SWPB	0	0	0	0	0	1	1	0	1	1						
INC	0	0	0	0	0	1	0	1	1	0						
INCT	0	0	0	0	0	1	0	1	1	1						
DEC	0	0	0	0	0	1	1	0	0	0						
DECT	0	0	0	0	0	1	1	0	0	1						
X**	0	0	0	0	0	1	0	0	1	0						

	OC	OC	OC	OC	OC	OC	C	C	C	C	TS	TS	S	S	S	S
LDCR	0	0	1	1	0	0							Format			
STCR	0	0	1	1	0	1							IV			

	OC	OC	OC	OC	OC	OC	OC	OC	SD	SD	SD	SD	SD	SD	SD	SD
SBO	0	0	0	1	1	1	0	1								
SBZ	0	0	0	1	1	1	1	0								
TB	0	0	0	1	1	1	1	1								
JEQ	0	0	0	1	0	0	1	1								
JGT	0	0	0	1	0	1	0	1								
JH	0	0	0	1	1	0	1	1								
JHE	0	0	0	1	0	1	0	0								
JL	0	0	0	1	1	0	1	0								
JLE	0	0	0	1	0	0	1	0								
JLT	0	0	0	1	0	0	0	1								
JMP	0	0	0	1	0	0	0	0								
JNC	0	0	0	1	0	1	1	1								
JNE	0	0	0	1	0	1	1	0								
JNO	0	0	0	1	1	0	0	1								
JOC	0	0	0	1	1	0	0	0								
JOP	0	0	0	1	1	1	0	0								

	OC	OC	OC	OC	OC	OC	OC	OC	C	C	C	C	W	W	W	W
SLA	0	0	0	0	1	0	1	0								
SRA	0	0	0	0	1	0	0	0								
SRC	0	0	0	0	1	0	1	1								
SRL	0	0	0	0	1	0	0	1								

	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	O	W	W	W	W
AI	0	0	0	0	0	0	1	0	0	0	1					
ANDI	0	0	0	0	0	0	1	0	0	1	0					
CI	0	0	0	0	0	0	1	0	1	0	0					
LI	0	0	0	0	0	0	1	0	0	0	0					
ORI	0	0	0	0	0	0	1	0	0	1	1					

	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	NC	NC	NC	NC	NC
LWPI	0	0	0	0	0	0	0	1	0	1	1	1					
LIMI	0	0	0	0	0	0	1	1	0	0	0						

	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	W	W	W	W
STST	0	0	0	0	0	0	1	0	1	1	0	0	VIII				
LST	0	0	0	0	0	0	0	0	1	0	0	0					
STWP	0	0	0	0	0	0	1	0	1	0	1	0					
LWP	0	0	0	0	0	0	0	0	1	0	0	1					

	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC
RTWP	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	OC	NC	NC	NC	NC	NC
IDLE	0	0	0	0	0	0	1	1	0	1	0						
RSET	0	0	0	0	0	0	1	1	0	1	1		Format				
CKOF	0	0	0	0	0	0	1	1	1	1	0		VII				
CKON	0	0	0	0	0	0	1	1	1	0	1						
LREX	0	0	0	0	0	0	1	1	1	1	1						

	0	0	0	0	0	0	0	1	0	0	W	W	W	W
LST														
LWP	0	0	0	0	0	0	0	1	0	0	1	W	W	W	W
DIVS	0	0	0	0	0	0	1	1	0	TS	TS	S	S	S	S
MPYS	0	0	0	0	0	0	1	1	1	TS	TS	S	S	S	S
LI	0	0	0	0	0	1	0	0	0	0	0	W	W	W	W
AI	0	0	0	0	0	1	0	0	0	1	0	W	W	W	W
ANDI	0	0	0	0	0	1	0	0	1	0	0	W	W	W	W
ORI	0	0	0	0	0	1	0	0	1	1	0	W	W	W	W
CI	0	0	0	0	0	1	0	1	0	0	0	W	W	W	W
STWP	0	0	0	0	0	1	0	1	0	1	0	W	W	W	W
STST	0	0	0	0	0	1	0	1	1	0	0	W	W	W	W
LWPI	0	0	0	0	0	1	0	1	1	1	NC	NC	NC	NC	NC
LIMI	0	0	0	0	0	1	1	0	0	0	NC	NC	NC	NC	NC

	0	0	0	0	0	1	1	0	1	0	NC	NC	NC	NC	NC
IDLE															
RSET	0	0	0	0	0	1	1	0	1	1	NC	NC	NC	NC	NC
RTWP	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0
CKON	0	0	0	0	0	1	1	1	0	1	NC	NC	NC	NC	NC
CKOF	0	0	0	0	0	1	1	1	1	0	NC	NC	NC	NC	NC
LREX	0	0	0	0	0	1	1	1	1	1	NC	NC	NC	NC	NC
BLWP	0	0	0	0	0	1	0	0	0	0	TS	TS	S	S	S	S
B	0	0	0	0	0	1	0	0	0	1	TS	TS	S	S	S	S
X**	0	0	0	0	0	1	0	0	1	0	TS	TS	S	S	S	S
CLR	0	0	0	0	0	1	0	0	1	1	TS	TS	S	S	S	S
NEG	0	0	0	0	0	1	0	1	0	0	TS	TS	S	S	S	S
INV	0	0	0	0	0	1	0	1	0	1	TS	TS	S	S	S	S
INC	0	0	0	0	0	1	0	1	1	0	TS	TS	S	S	S	S
INCT	0	0	0	0	0	1	0	1	1	1	TS	TS	S	S	S	S
DEC	0	0	0	0	0	1	1	0	0	0	TS	TS	S	S	S	S
DECT	0	0	0	0	0	1	1	0	0	1	TS	TS	S	S	S	S
BL	0	0	0	0	0	1	1	0	1	0	TS	TS	S	S	S	S
SWPB	0	0	0	0	0	1	1	0	1	1	TS	TS	S	S	S	S
SETO	0	0	0	0	0	1	1	1	0	0	TS	TS	S	S	S	S
ABS	0	0	0	0	0	1	1	1	0	1	TS	TS	S	S	S	S
SRA	0	0	0	0	1	0	0	0	C	C	C	C	W	W	W	W
SRL	0	0	0	0	1	0	0	1	C	C	C	C	W	W	W	W
SLA	0	0	0	0	1	0	1	0	C	C	C	C	W	W	W	W
SRC	0	0	0	0	1	0	1	1	C	C	C	C	W	W	W	W
JMP	0	0	0	1	0	0	0	0	SD	SD	SD	SD	SD	SD	SD	SD
JLT	0	0	0	1	0	0	0	1	SD	SD	SD	SD	SD	SD	SD	SD
JLE	0	0	0	1	0	0	1	0	SD	SD	SD	SD	SD	SD	SD	SD
JEQ	0	0	0	1	0	0	1	1	SD	SD	SD	SD	SD	SD	SD	SD
JHE	0	0	0	1	0	1	0	0	SD	SD	SD	SD	SD	SD	SD	SD
JGT	0	0	0	1	0	1	0	1	SD	SD	SD	SD	SD	SD	SD	SD
JNE	0	0	0	1	0	1	1	0	SD	SD	SD	SD	SD	SD	SD	SD
JNC	0	0	0	1	0	1	1	1	SD	SD	SD	SD	SD	SD	SD	SD
JOC	0	0	0	1	1	0	0	0	SD	SD	SD	SD	SD	SD	SD	SD
JNO	0	0	0	1	1	0	0	1	SD	SD	SD	SD	SD	SD	SD	SD
JL	0	0	0	1	1	0	1	0	SD	SD	SD	SD	SD	SD	SD	SD
JH	0	0	0	1	1	0	1	1	SD	SD	SD	SD	SD	SD	SD	SD
JOP	0	0	0	1	1	1	0	0	SD	SD	SD	SD	SD	SD	SD	SD
SBO	0	0	0	1	1	1	0	1	SD	SD	SD	SD	SD	SD	SD	SD
SBZ	0	0	0	1	1	1	1	0	SD	SD	SD	SD	SD	SD	SD	SD
TB	0	0	0	1	1	1	1	1	SD	SD	SD	SD	SD	SD	SD	SD
COC	0	0	1	0	0	0	D	D	D	D	TS	TS	S	S	S	S
CZC	0	0	1	0	0	1	D	D	D	D	TS	TS	S	S	S	S
XOR	0	0	1	0	1	0	D	D	D	D	TS	TS	S	S	S	S
XOP	0	0	1	0	1	1	D	D	D	D	TS	TS	S	S	S	S
LDCR	0	0	1	1	0	0	C	C	C	C	TS	TS	S	S	S	S
STCR	0	0	1	1	0	1	C	C	C	C	TS	TS	S	S	S	S
MPY	0	0	1	1	1	0	D	D	D	D	TS	TS	S	S	S	S
DIV	0	0	1	1	1	1	D	D	D	D	TS	TS	S	S	S	S
SZC	0	1	0	0	TD	TD	D	D	D	D	TS	TS	S	S	S	S
SZCB	0	1	0	1	TD	TD	D	D	D	D	TS	TS	S	S	S	S
S	0	1	1	0	TD	TD	D	D	D	D	TS	TS	S	S	S	S
SB	0	1	1	1	TD	TD	D	D	D	D	TS	TS	S	S	S	S
C	1	0	0	0	TD	TD	D	D	D	D	TS	TS	S	S	S	S
CB	1	0	0	1	TD	TD	D	D	D	D	TS	TS	S	S	S	S
A	1	0	1	0	TD	TD	D	D	D	D	TS	TS	S	S	S	S
AB	1	0	1	1	TD	TD	D	D	D	D	TS	TS	S	S	S	S
MOV	1	1	0	0	TD	TD	D	D	D	D	TS	TS	S	S	S	S
MOVB	1	1	0	1	TD	TD	D	D	D	D	TS	TS	S	S	S	S
SOC	1	1	1	0	TD	TD	D	D	D	D	TS	TS	S	S	S	S
SOCB	1	1	1	1	TD	TD	D	D	D	D	TS	TS	S	S	S	S