APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		A	ECN 935953 G. McCLUSKEY 9-17-79 (1) EXTENSIVE REVISION	9-19-79	

SHEET																								
REV STATUS	REV	A														A	A							
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ±1°
3 PLACE DECIMAL ± .010
2 PLACE DECIMAL ± .02

DESCRIPTIVE NUMBERS
SHOWN IN PARENTHESES
FOR REFERENCE ONLY

TEXAS INSTRUMENTS
INCORPORATED
LUBBOCK, TEXAS

I/O BUS SPECIFICATION
HOME COMPUTER, 99/4

SIZE	DRAWING NO
A	1037185

SCALE

SHEET 1 OF 23

TI 919614

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1.0 SCOPE

This specification describes the I/O bus concept for the Texas Instruments Home Computer 99/4. It also defines the functional, electrical, and mechanical requirements for the I/O interface and discusses the quality assurance provisions which have been taken and are planned.

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2.0 APPLICABLE DOCUMENTS

2.1 Writing subroutine links, device service routines and interrupt service routines for the Home Computer.

2.2 Home Computer system memory, CRU, and interrupt mapping specification.

2.3 9900 family systems design and data book.

2.4 I/O bus evaluation.

3.0 GENERAL DESCRIPTION

The concept for the Texas Instruments Home Computer 99/4 I/O bus is to provide maximum flexibility and good performance within a constraint of low cost for both mainframe and computer system. This concept is achieved by providing both memory and CRU I/O buses to the 99/4 peripherals. The memory bus (16 bit data bus converted to eight bits wide) is used for instruction fetch from control ROM in the peripherals and for data transfer to/from memory mapped peripherals. The CRU bus is used for peripheral enable/disable and for device control and data transfer to/from CRU mapped peripherals.

A block diagram of the TI 99/4 electronics is shown in Figure 3.0. The TMS 9900 microprocessor accesses each peripheral to obtain instructions from the device service routine (DSR) read only memory. Since each peripheral contains its own DSR, the 99/4 does not have to be designed to anticipate future peripheral requirements. The dual I/O bus capability, along with interrupt handling and external DSRs provide flexibility at low cost.

Details on the DSR content and format are contained in the document referred to in Paragraph 2.1.

99/4 SYSTEM DIAGRAM

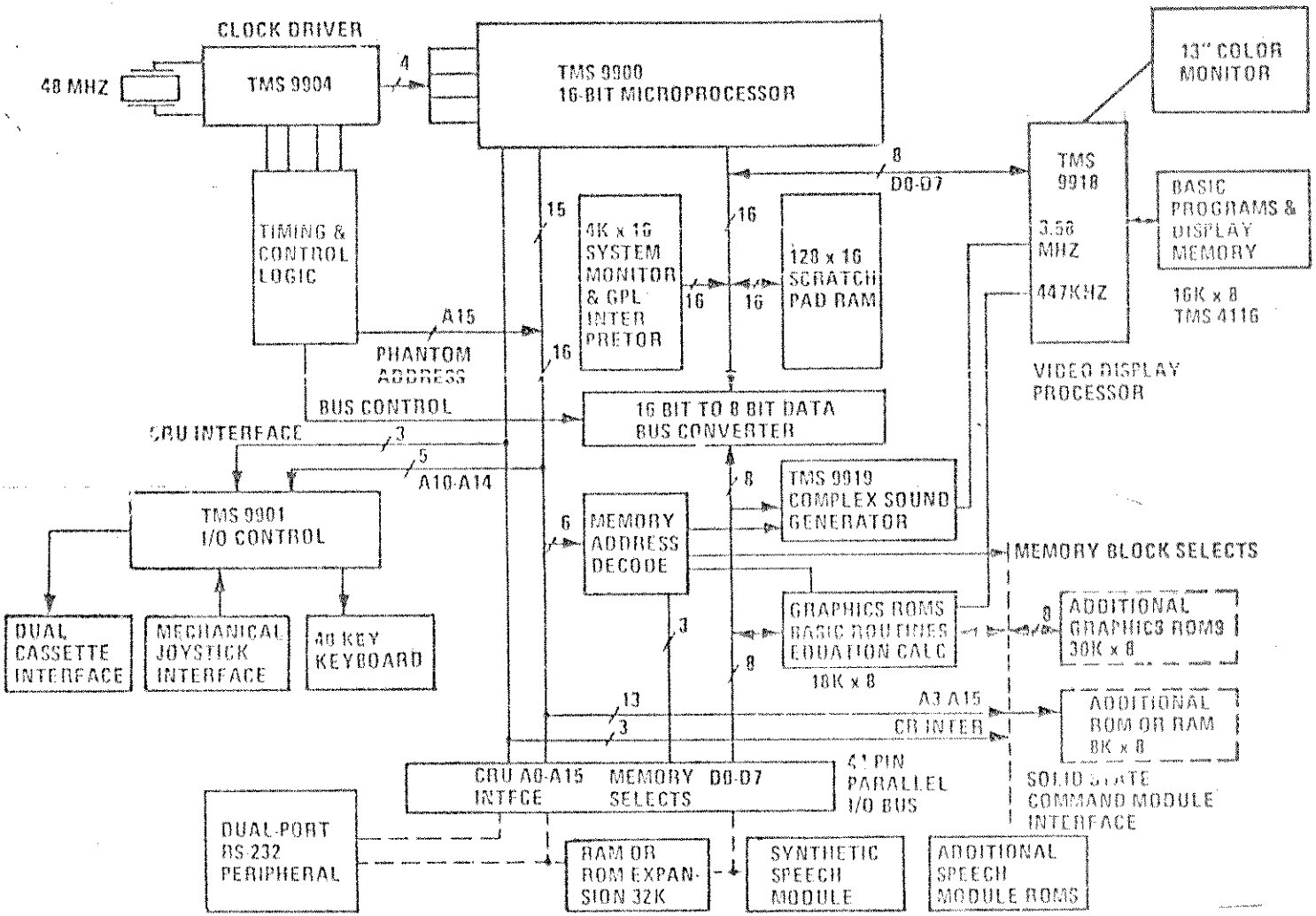

FIGURE 3.0

4.1 FUNCTIONAL REQUIREMENTS

4.1.1 I/O PIN DESCRIPTION

The table below defines the Home computer I/O pin assignments and describes the functions of each pin.

SIGNATURE	PIN	I/O	DESCRIPTION
A0	31	Out	
A1	30	Out	ADDRESS BUS
A2	20	Out	
A3	10	Out	A0 through A15 comprise the address bus.
A4	7	Out	This bus provides the 16 bit memory address vector to the external memory system
A5	5	Out	when MEMEN is active. Address bit 15 is
A6	29	Out	also used for CRU DATA OUT on CRU output
A7	17	Out	instructions.
A8	14	Out	
A9	18	Out	
A10	6	Out	
A11	8	Out	
A12	11	Out	
A13	15	Out	
A14	16	Out	
A15/CRUOUT	19	Out	
D0	37	I/O	DATA BUS
D1	40	I/O	
D2	39	I/O	D0 through D7 comprise the bidirectional
D3	42	I/O	data bus. This bus transfers memory data
D4	35	I/O	to (when writing) and from (when reading)
D5	38	I/O	the external memory system when MEMEN is
D6	36	I/O	active.
D7	34	I/O	
			BUS CONTROL
$\overline{\text{MEMEN}}$	32	Out	MEMory ENable. $\overline{\text{MEMEN}}$ indicates a memory access.
DBIN	9	Out	Data Bus In. When active (high) the data buffers and 9900 are in the input mode.
$\overline{\text{WE}}$	26	Out	Write Enable. $\overline{\text{WE}}$ indicates a memory write.
$\overline{\text{MBE}}$	28	Out	Memory Block Enable. $\overline{\text{MBE}}$ indicates a memory access in memory block >4000-5FFF.
$\overline{\text{CRUCLK}}$	22	Out	CRU Clock. Indicates data is available on the CRU OUT line.
CRUIN	33	In	CRU data IN. Input data line to the Home Computer.

4.1.1 I/O PIN DESCRIPTION (CONTINUED)

SIGNATURE	PIN	I/O	DESCRIPTION
			MEMORY CONTROL
READY/$\overline{\text{HOLD}}$	12	In	READY (when $\overline{\text{MEMEN}}$ is active) indicates external memory is ready for a memory access. $\overline{\text{HOLD}}$ (when $\overline{\text{MEMEN}}$ is inactive) indicates a request to use the data bus.
HOLDA/IAQ	41	Out	HOLD Acknowledge goes true when $\overline{\text{MEMEN}}$ is inactive and indicates that the 9900 is in a HOLD state. Instruction AcQuisition indicates (when $\overline{\text{MEMEN}}$ is active) the CPU is acquiring an instruction during a memory cycle.
			TIMING AND CONTROL
$\overline{\text{LOAD}}$	13	In	When active, $\overline{\text{LOAD}}$ causes the CPU to execute a nonmaskable interrupt with memory address FFFC containing the trap vector.
$\overline{\text{RESET}}$	3	Out	When active, $\overline{\text{RESET}}$ causes the Home Computer and the peripherals to be reset. Will be held active for a minimum of 5 clock cycles.
$\overline{\text{EXT INT}}$	4	In	EXTernal INTerrupt. When active, $\overline{\text{EXT INT}}$ causes the CPU to execute an interrupt.
$\overline{\text{Ø3}}$	24	Out	CPU Clock. Phase 3 of the CPU clock.
			POWER
GND	21,23 25,27		Ground reference.
			SPEECH MODULE SIGNALS
SBE	2	Out	Speech Block Enable. SBE indicates a memory access in the speech memory.
AUDIO IN	44	In	Input for the audio from the speech module.
+5	1		Supply voltage (+5V Nom)for speech module
-5	43		Supply voltage (-5V Nom)for speech module

4.1.2 MEMORY ALLOCATION

As specified in the Home Computer Mapping specification, the memory address space is broken into 8 blocks of 8K bytes of memory. The third block (addresses 400^-5FFF) is predecoded and made available at the I/O port for the peripherals. The sixth, seventh and eighth block (addresses A000-FFFF) are available for future expansion. For the speech module, (addresses>9000-97FF), a predecoded line is available at the I/O port.

4.1.3 CRU ALLOCATION

Of the available 4K of CRU bits, the first 1K (addresses 0000-07FE) are used internally in the Home Computer. The second 1K (addresses 0800-0FFE) are reserved for future use. The last 2K (addresses 1000-1FFE) are reserved for the peripherals to be plugged in the I/O port. A block of 128 CRU bits is assigned to each peripheral as listed below.

CRU ADDRESS	PERIPHERAL
1000	Disk
1100	Reserved
1200	Home Security
1300	RS-232
1400	Modem
1500	Reserved
1600	Digital Cassette
1700	Student Typing
1800	Thermal Printer
1900	Not Assigned Yet
1A00	Not Assigned Yet
1B00	Not Assigned Yet
1C00	Not Assigned Yet
1D00	Not Assigned Yet
1E00	Not Assigned Yet
1F00	Not Assigned Yet

4.1.4 INTERRUPT HANDLING

The interrupt available on the I/O port is one of the maskable interrupts of the TMS 9901 Programmable Systems Interface. Refer to the TMS 9900family data book and the Home Computer Mapping specification for Interrupts assignments.

4.2 ELECTRICAL REQUIREMENTS

4.2.1 LOADING

THE LOADING OF EACH I/O SIGNAL IN THE WORST CASE SITUATION (I.E., WITH THREE PERIPHERALS INCLUDING THE SPEECH MODULE) IS SHOWN IN TABLE 4.2.1. FIRST COLUMN SHOWS THE TOTAL LOAD, (DUE TO CONSOLE AND PERIPHERALS) AND THE SECOND COLUMN SHOWS THE LOAD EXTERNAL TO THE CONSOLE.

4.2.2 BUFFERING

EACH PERIPHERAL WILL BUFFER THE DATA BUS WITH A 74LS245 TYPE DRIVER (EXCEPT THE RS-232 WHICH USES A 74LS367 IN ORDER TO SAVE A PACKAGE). ALL I/O SIGNALS OTHER THAN THE DATA BUS, FROM THE 99/4 WILL DRIVE TWO LS-TYPE LEADS (VIH = 2.0V, VIL = 0.6V, IIH = 20μA, AND IIL = -0.2mA) PER PERIPHERAL. SEE TABLES 4.2.2, 4.2.3, AND 4.2.4 FOR I/O ELECTRICAL CHARACTERISTICS. IN ADDITION, PERIPHERALS GENERATING CRUIN, READY/$\overline{\text{HOLD}}$, $\overline{\text{LOAD}}$, AND $\overline{\text{EXTINT}}$ SHALL BUFFER THESE SIGNALS BEFORE THEY ARE PUT ON THE I/O BUS.

4.2.3 I/O READ

A CPU READ CYCLE FOR THE EXTERNAL DEVICE CONSISTS OF TWO 8-BIT READ CYCLES (FIG. 4.2.3). THE 2 BYTES READ ARE ASSEMBLED AS A 16 BIT WORD BEFORE THEY ARE PRESENTED TO THE 9900. SHOWN IN FITURE 4.2.3 ARE TWO 8 BIT READ CYCLES WITH ONE WAIT STATE INSERTED IN EACH TO WORK WITH SLOW MEMORIES. $\overline{\text{MEMEN}}$ GOES LOW TRUE AT THE BEGINNING OF CLOCK CYCLE 1. AT THE SAME TIME DBIN GOES HIGH TRUE. WE STAYS HIGH FALSE DURING THE ENTIRE CYCLE. AT THE SAME TIME THAT $\overline{\text{MEMEN}}$ GOES TRUE, THE ADDRESS BUS GOES ACTIVE. IN ORDER FOR THE NOISE AND THE GLITCHES (ASSOCIATED WITH CROSSTALK AND SIMULTANEOUS SWITCHING) TO GO AWAY WE ALLOW A MINIMUM OF 100 nS FOR THE ADDRESS LINES TO SETTLE. $\overline{\text{MBE}}$ (PRECODED FROM A0, A1 AND A2) GOES TRUE DURING THE LEADING EDGE OF Ø2 OF CLOCK CYCLE 1. DATA READ FROM THE PERIPHERALS WILL BE VALID 750 nS AFTER THE START OF CLOCK CYCLE 1. THE CPU WILL LOOK AT THE FULL 16 BIT DATA BUS DURING THE LEADING EDGE OF Ø1, OF CLOCK CYCLE 2. UNDER WORSE-CASE CONDITIONS, DATA MUST BE VALID 100 nS BEFORE THAT TIME.

4.2.4 I/O WRITE

Figure 4.2.4 shows a 16 bit I/O write cycle. As described earlier it is composed of two 8-bit writes. A write cycle will always be preceeded by a ALU cycle. $\overline{\text{MEMEN}}$ and DBIN go true at the start of the cycle. A settling time of 100 nS (min) is allowed for the address lines to settle down. $\overline{\text{WE}}$ goes true (low) on the leading edge of Ø2, during the wait states, and stays true for 660 nS (TYP). Both during a Read or a Write the odd byte is accessed first, followed by an even byte (this is to maintain compatibility with the 9985). A15/CRU OUT changes its state 990 nS (TYP) after the cycle is initiated. The second 8-bit write cycle is identical to the first 8-bit write. $\overline{\text{MBE}}$ stays true (low) during the entire (1.3 us) cycle.

4.2.5 SPEECH INTERFACE

The I/O port has 4 lines dedicated for use by the speech module: +5, -5, Speech Block Enable, and Audio In. See tables 4.2.3 and 4.2.4 for their electrical parameters.

SBE is decoded by the 99/4 for addresses >9000 and >9400 (write and read). For the write cycle, SBE goes active after the address and data lines are valid; see figure 4.2.7 for the Sound Write Timing.

The Audio In pin is an input from the speech module to the Audio In pin on the sound chip (9919). See table 4.2.4 for acceptable input levels.

4.2.6 GROM INTERFACE ON I/O PORT

No special timing is provided by the 99/4 to the I/O port when a GROM is used. However, table 4.2.5 (GROM electrical requirements) is included because the GROMS in the Command Module space share a common data interface with I/O and because it may be desired to implement a GROM on I/O later.

4.2.7 CRU TIMING

CRU interface timing is shown in Figure 4.2.5. The CRUOUT cycle is composed of 2 clock cycles. The CRU bit address when placed on the address bus A0 through A14 is allowed to settle for 100 nS (min). CRUCLK is a 80 nS (min) low true signal which occurs on the trailing edge of Ø1 of clock cycle 2. CRUOUT data is valid at the start of clock cycle 1, and is latched by the CRUCLK in the respective peripheral.

CRUIN also consists of 2 clock cycles 660 nS (TYP). Again we allow 100 nS for the add bus to settle down. CPU samples the CRUIN line on the leading edge of Ø1 of clock cycle 2. Data must be valid 40 nS (min) before that.

TABLE 4.2.1 I/O BUS LOADING

SIGNAL	TOTAL SWITCHING LOAD(pF)	MAXIMUM PERIPHERAL LOAD (pF)
D0-D7	210	90
A0-A2	100	90
A3-A14	100	90
CRUOUT/A15	110	100
$\overline{03}$	110	100
$\overline{RESET}$	100	90
READY/HOLD	80	70
CRUIN	125	90
CRUCLK	100	90
$\overline{MBE}$	100	90
$\overline{WE}$	100	90
SBE	35	25
DBIN	100	90
$\overline{MEMEN}$	100	90
HOLDA/IAQ	80	70

TABLE 4.2.2 DRIVE CAPABILITY OF I/O SIGNALS

SIGNAL NAME	DRIVER
$\overline{03}$	74LS244
CRUCLK	74LS244
$\overline{WE}$	74LS244
A0	74LS244
A1	74LS244
A2	74LS244
DBIN	74LS241
$\overline{MBE}$	74LS138
$\overline{MEMEN}$	74LS32
A3-A14	74LS367
D0-D7	74LS245
A15/CRUOUT	74LS244
SBE	74LS03
HOLDA	74LS32
$\overline{RESET}$	74LS04

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ELECTRICAL CHARACTERISTICS (WORST CASE CONDITIONS)

OUTPUTS (from 99/4)	VoH min/max (V)	VOL min/max (V)	IOH min/max (mA)	IOL min/max (mA)
driven by LS367: A0-A14	2.4/	/0.4	/-2.6	/24
driven by LS244: A15, $\overline{Q3}$, $\overline{MBE}$, $\overline{WE}$, $\overline{CRUCLK}$	2.4/	/0.5	/-15	/24
driven by LS04: $\overline{DBIN}$, $\overline{RESET}$	2.7/	/0.5	/-400µA	/8
driven by LS03: SBE	/5.5	/0.4	/50µA	/8
$\overline{MEMEN}$	2.4/	/0.4	/-630µA	/12
D0-D7, DRIVEN BY LS245/ LS244	(VCC-0.5V)/	/0.5	/-15	/24
D0-D7 DRIVEN BY 0430 GROMS	2.4/	/0.6	/-1	/2

TABLE 4.2.3 ELECTRICAL CHARACTERISTICS OF I/O CONNECTOR

SIZE		DRAWING NO
A		1037185
SCALE	REV A	SHEET 12

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ELECTRICAL CHARACTERISTICS (WORST CASE CONDITIONS)

INPUTS (to 99/4)	VIH min/max (V)	VIL min/max (V)	IIH min/max (mA)	IIL min/max (mA)
DØ-D7	2/	/0.8	/.95	/-0.71
TO 9900 LOAD, CRUIN	2.2/5.25	-1/0.8	/1	-1/
TO 9901 EXT INT	2.0/5.25	-.3/0.8	/100	/-100
TO 9919 AUDIO IN *	2.0/	/0.8	/70	--

* AC COUPLED

TABLE 4.2.4 ELECTRICAL CHARACTERISTICS OF I/O TABLE

SIZE		DRAWING NO.
A		1037185
SCALE	REV A1	SHEET 16

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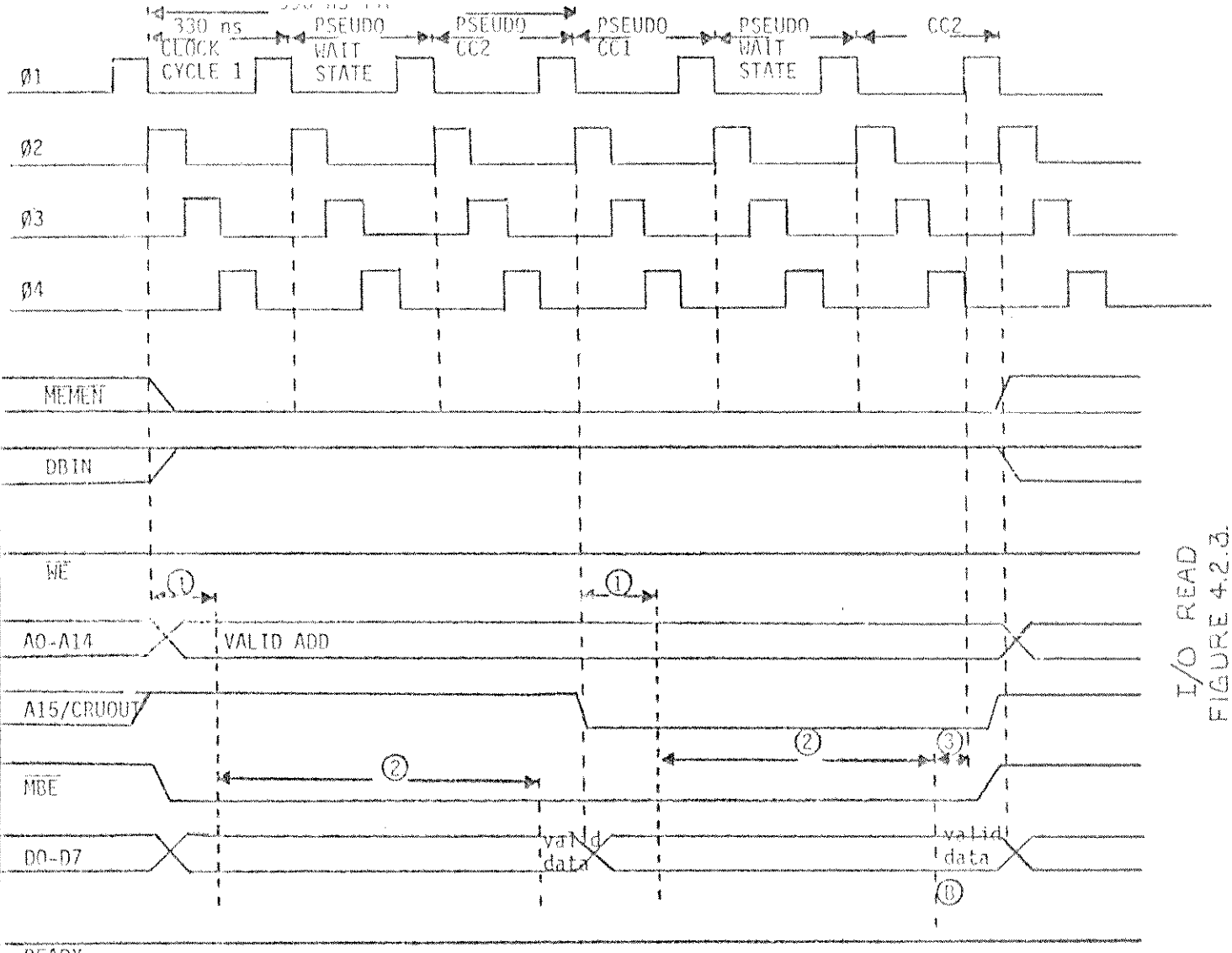
GROM INPUT/OUTPUT REQUIREMENTS

PARAMETER	MIN	NOM	MAX	UNITS
VIH	4.6		5.05	V
VIL			0.6	V
VOH	2.4			V
VOL (1)			0.6	V
IOH				mA
IOL (1)			2.0	mA

(1) WORST CASE TEST CONDITIONS: Vcc=+5.25, Vss=-0.6V, Vbb=-4.75V. UNDER THESE CONDITIONS, OUTPUT BUFFER WILL PULL A 270pF LOAD TO -0.6V IN 1.5µSECS WHILE SINKING A CURRENT OF 20 mA.

TABLE 4.2.5 GROM ELECTRICAL CHARACTERISTICS



I/O READ
FIGURE 4.2.3.

1 SETTLING TIME 100 nS(MIN)

2 ACCESS TIME FOR DSR ROM + DATA Ts + DATA BUFF DELAY(PERIPHERAL + MAINFRAME) = 650 nS(MAX)

3 SET UP TIME FOR 9900 = 60 nS(MIN)

SIZE	DRAWING NO	REV
A	1037185	

SCALE

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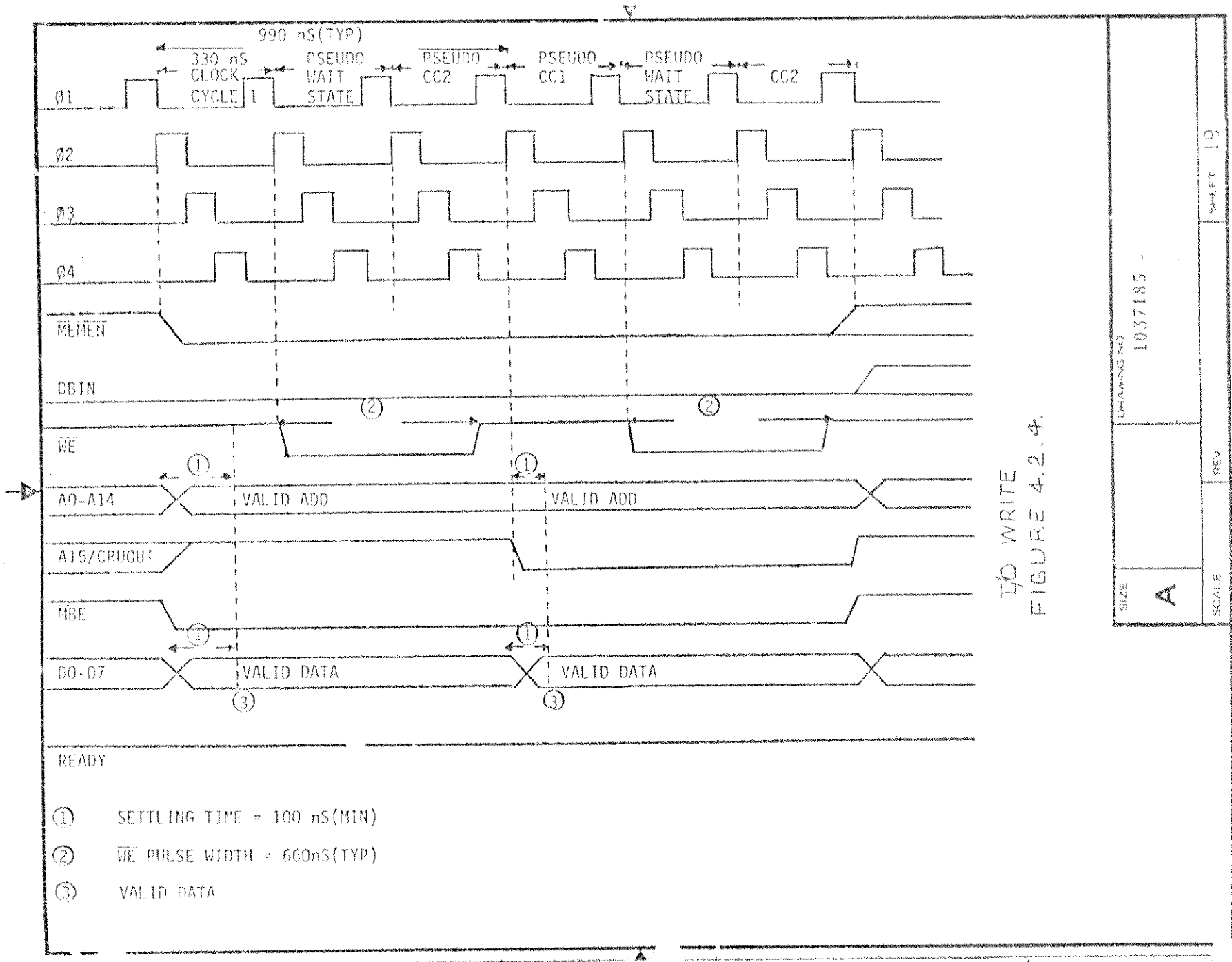
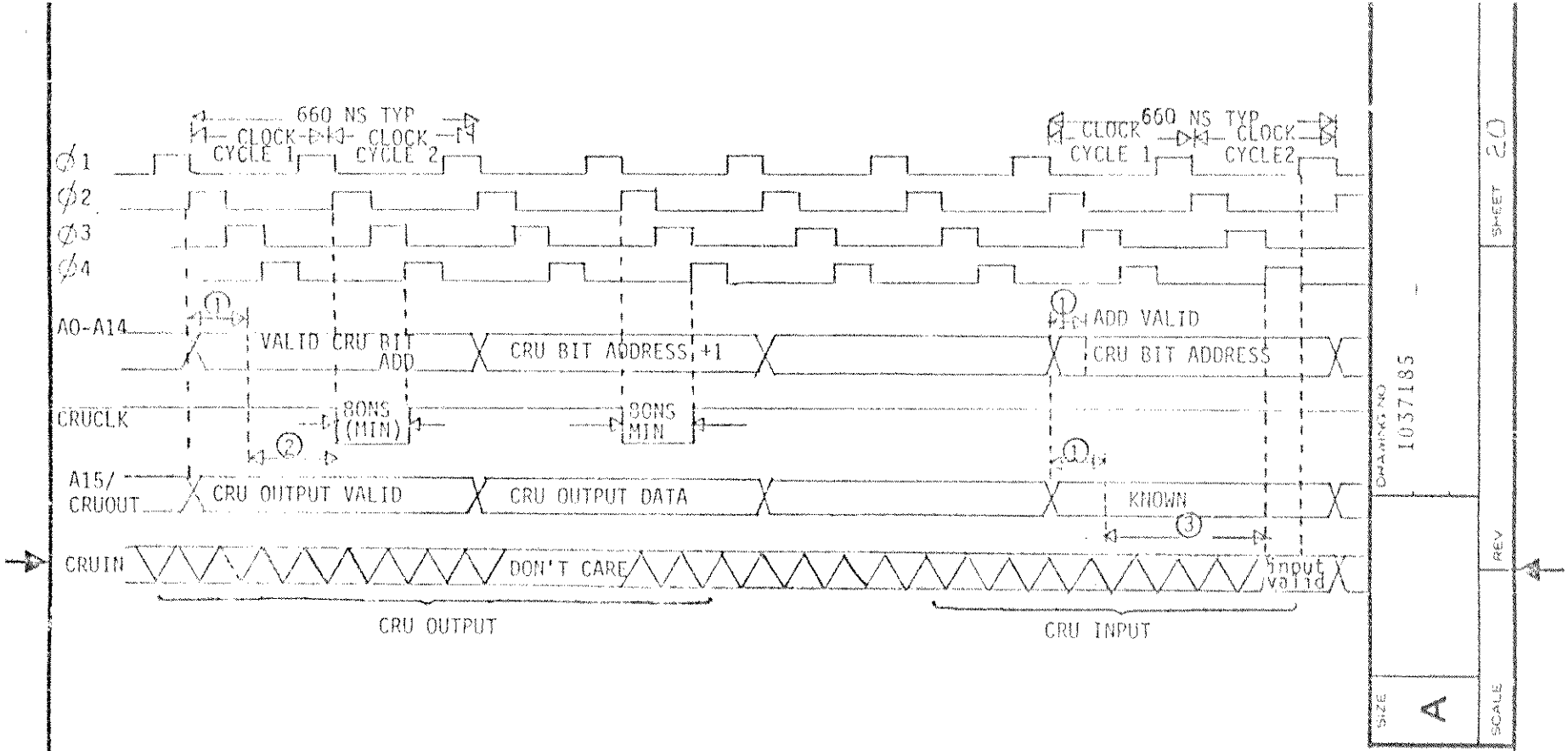


I/O WRITE
FIGURE 4.2.4.

DRAWING NO
1037185 -

SIZE A
SCALE
REV
SHEET 19

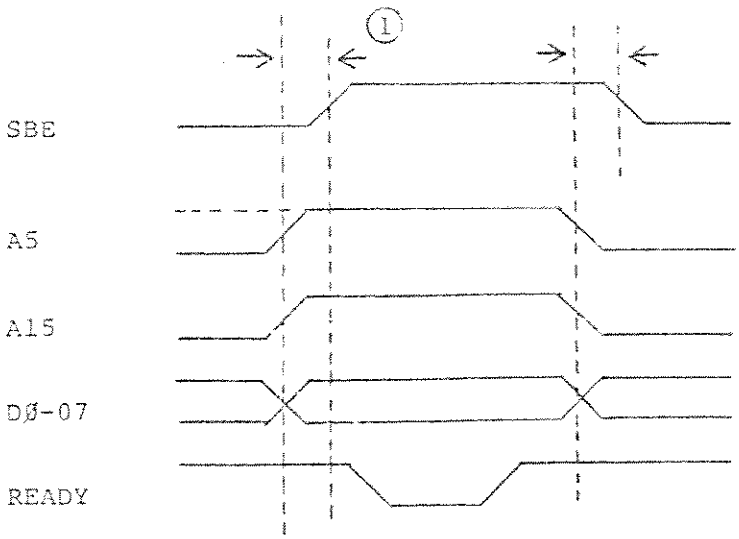


① ⟶ SETTLING TIME 100NS (MIN)

② ⟶ ADD VALID TO $\overline{\text{CRUCLK}}$ = 220NS (TYP)

③ ⟶ ADD VALID TO VALID CRUIN = 400NS (MAX)

FIGURE 4.2.5.



WRITE TO SPEECH TIMING.

DELAY, ADDRESS VALID TO SBE VALID, NSEC..

		MIN	MAX
1	SBE LOW TO HI	16	46
2	SBE HI TO LOW	24	44

FIGURE 4.2.7 TYPICAL SBE TIMING

SIZE		DRAWING NO
A		1037135
SCALE	REV	SHEET 21

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4.3 MECHANICAL REQUIREMENTS

The I/O bus of the 99/4 is accessible by opening a plastic door on the right side of the console as defined by mechanical drawings 1015934 and 1017936. The PCB edge card connector is a 44 pin double sided connector with 22 connection pairs located 100 mils apart. The mating connector specified for the peripherals is TI P/N 1034736-22. In addition there is a mating shield requirement due to the RFI specification to level 20730. The mating shield is Beryllium Copper and is designed to produce less than 10 milliohms resistance with a minimum clamping force of 5 pounds.

5.0 QUALITY ASSURANCE PROVISIONS

5.1 DESIGN VERIFICATION

Numerous analysis, breadboard and test exercises have been made to verify the I/O bus design concept and implementation. This process is ongoing as peripheral designs evolve. A summary of much of the work to date is contained in the I/O Bus Evaluation report.

5.2 PRODUCT TESTING

Part of the 99/4 final assembly test process will be the atachment of a special peripheral unit with worst ;e electrical loading and mechanical fit which will fully exercise all I/O lines at maximum speed. This "test" peripheral is yet to be defined in detail.