

MAIN LOGIC BOARD #1  
SHEET 1

**PRELIMINARY**  
FOR INFORMATION ONLY  
DATE 11/7/78

-2	-1	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	REMARKS

UNLESS OTHERWISE SPECIFIED  
 • DIMENSIONS ARE IN INCHES  
 • TOLERANCES  
 ANGLES ±  
 3 PLACE DECIMALS ±  
 2 PLACE DECIMALS ±  
 • DIMENSIONING IN ACCORDANCE  
 WITH ANSI Y14.5

MATERIAL:

DWN S. ALLEN 10-17-78  
 DATE  
 CHK  
 DESIGNER  
 QA  
 APVD  
 PRODUCT ENG  
 DESIGN ACTIVITY RELEASE

TEXAS INSTRUMENTS  
 INCORPORATED  
 CALCULATOR PRODUCTS DIVISION

MAIN LOGIC BOARD

SUP DWG SIZE DRAWING NO  
 D NA

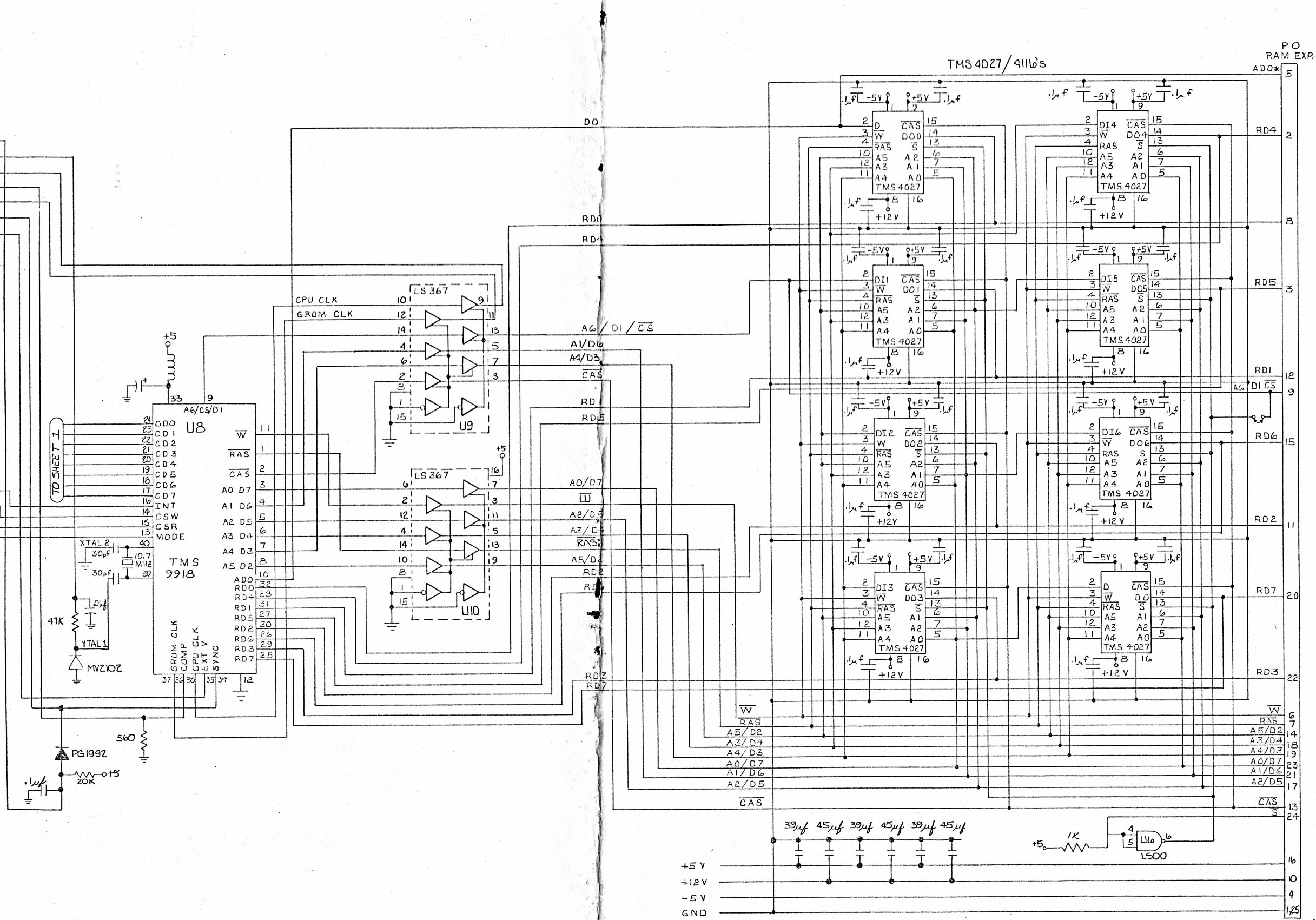
SCALE NONE REV LTR: SHEET 1/4

CLASS CODE:

(J2 CONT. FROM SHT. 3)

RESET 24  
 DC CONT. 22  
 CPU CLK 20  
 COMP VIDE 2  
 GROM CLK 15  
 SAMP/RESET 21  
 EXT VDD 23

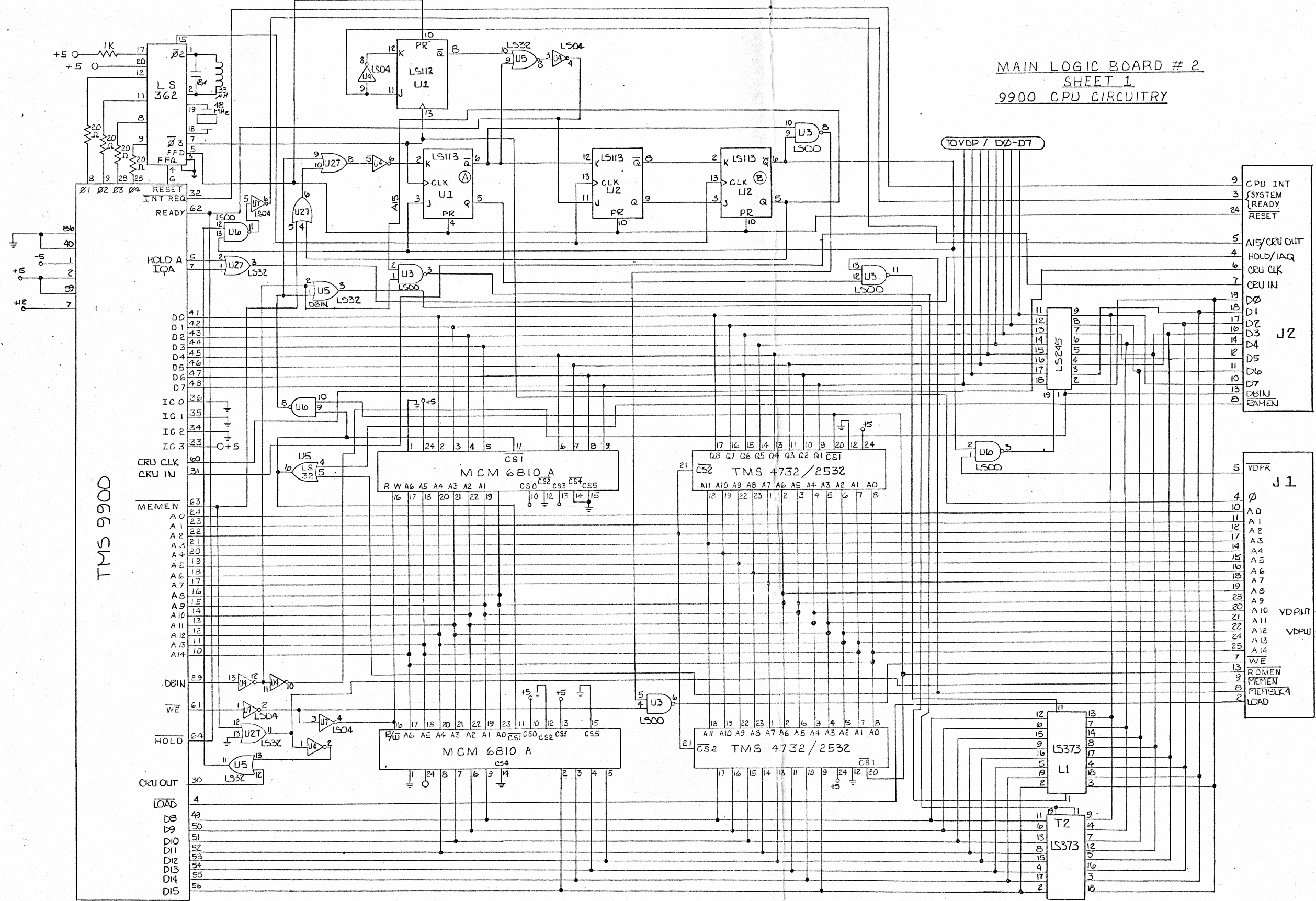
VPIN1 3  
 VDPW 6  
 YDPR 5  
 A14 25  
 P/O MLB COMUJ1



MAIN LOGIC BOARD  
 SHT. 2

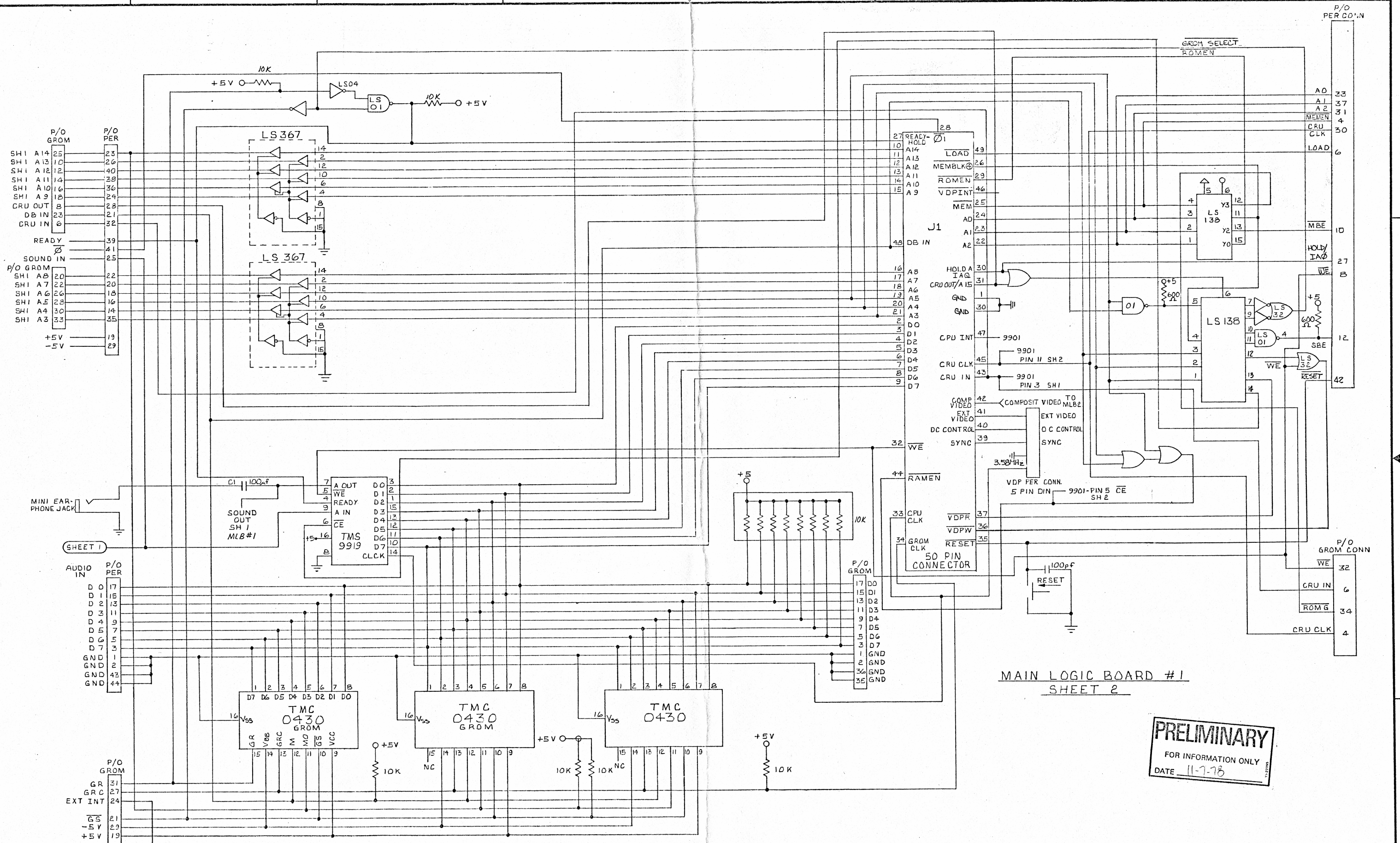
**PRELIMINARY**  
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MAIN LOGIC BOARD # 2  
SHEET 1  
9900 CPU CIRCUITRY



- 9 CPU INT
- 3 SYSTEM
- 24 READY
- 5 RESET
- 5 A15/CRU OUT
- 4 HOLD/IAQ
- 6 CRU CLK
- 7 CRU IN
- 19 D0
- 18 D1
- 17 D2
- 16 D3
- 14 D4
- 15 D5
- 11 D6
- 13 D7
- 8 DBIN
- 8 DBOUT
- 5 VDPR
- 4 A0
- 10 A1
- 11 A2
- 12 A3
- 17 A4
- 14 A5
- 15 A6
- 16 A7
- 18 A8
- 19 A9
- 23 A10
- 20 A11
- 21 A12
- 22 A13
- 24 A14
- 7 WE
- 13 ROMEN
- 9 MEMEN
- 8 MEMELK4
- 2 LOAD

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MAIN LOGIC BOARD #1  
SHEET 2

**PRELIMINARY**  
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