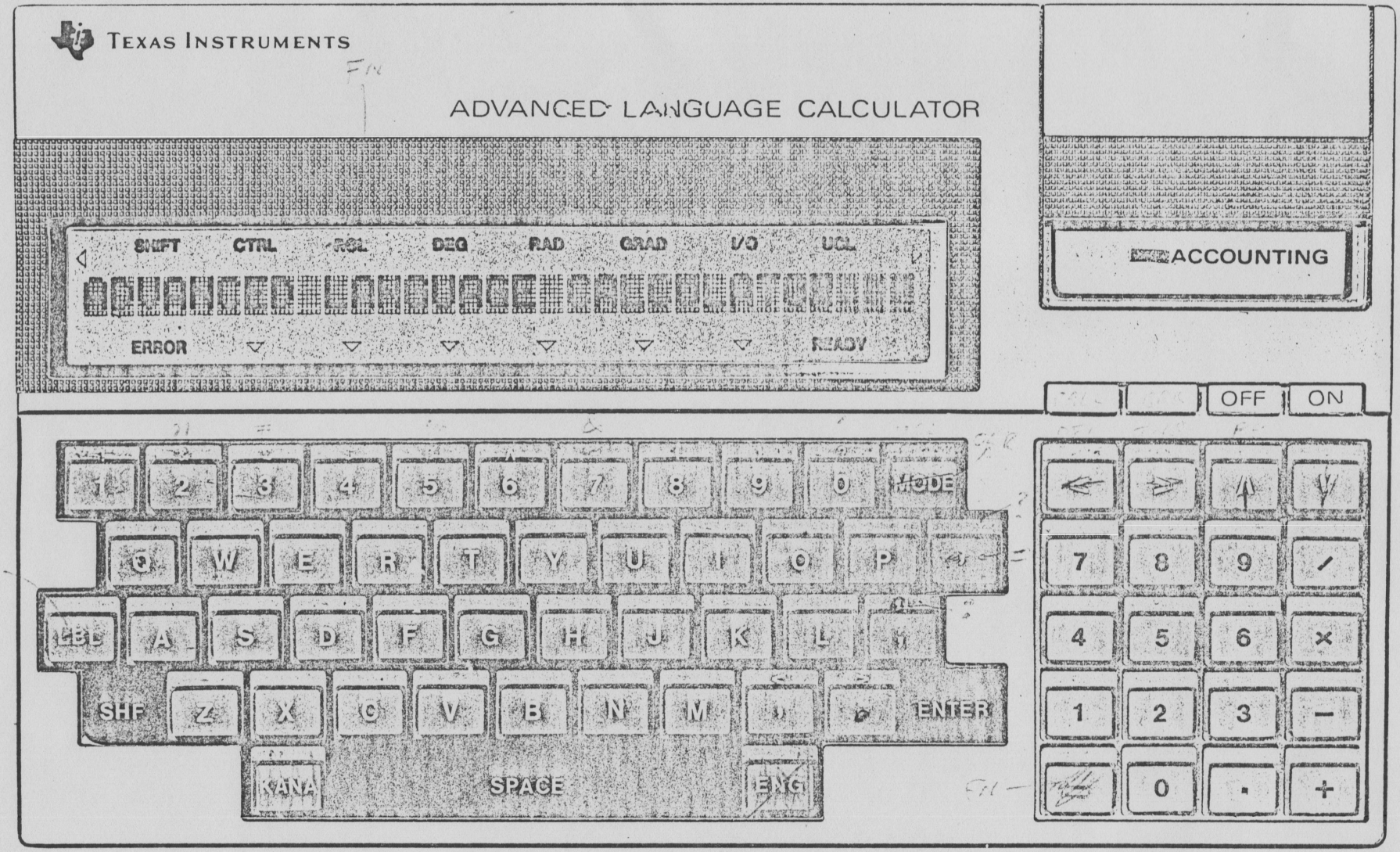
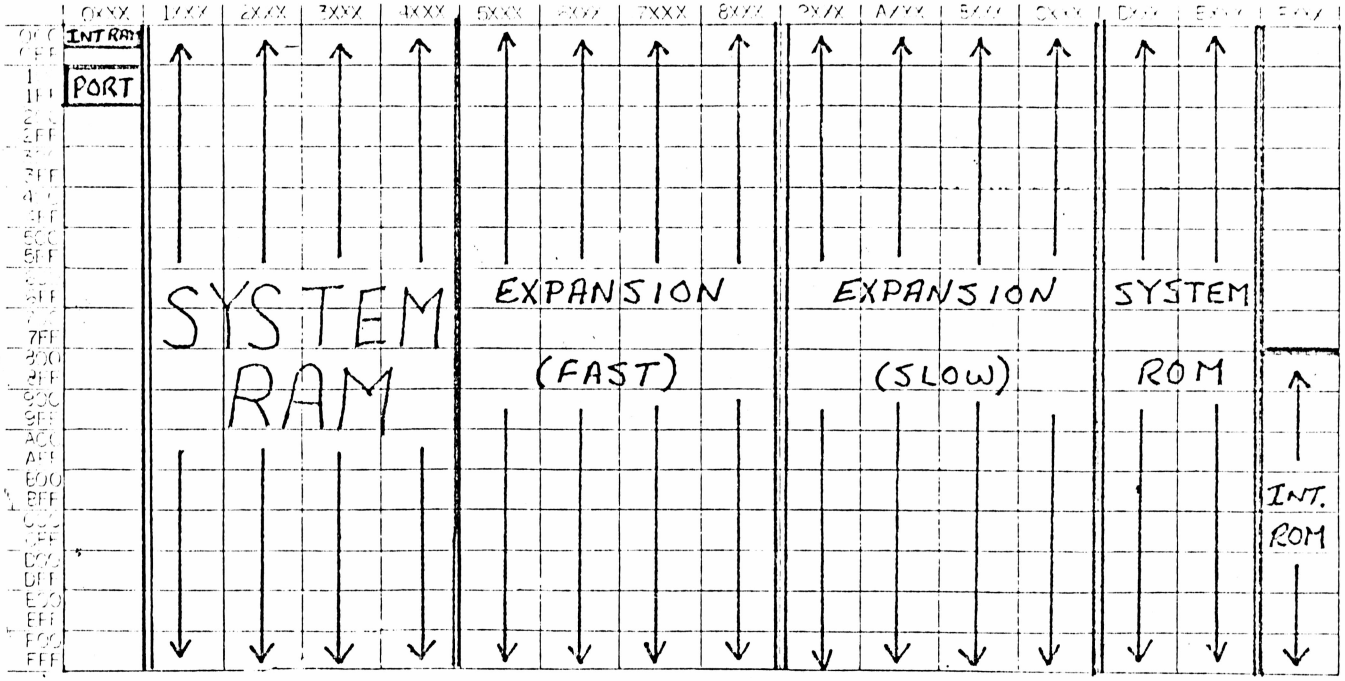

TEXAS INSTRUMENTS
ADVANCED LANGUAGE CALCULATOR
SHIFT
CTRL
RSL
DEG
RAD
GRAD
I/O
UCL
ERROR
READY
ACCOUNTING
OFF
ON
MODE
SHF
ENTER
KANA
SPACE
ENG

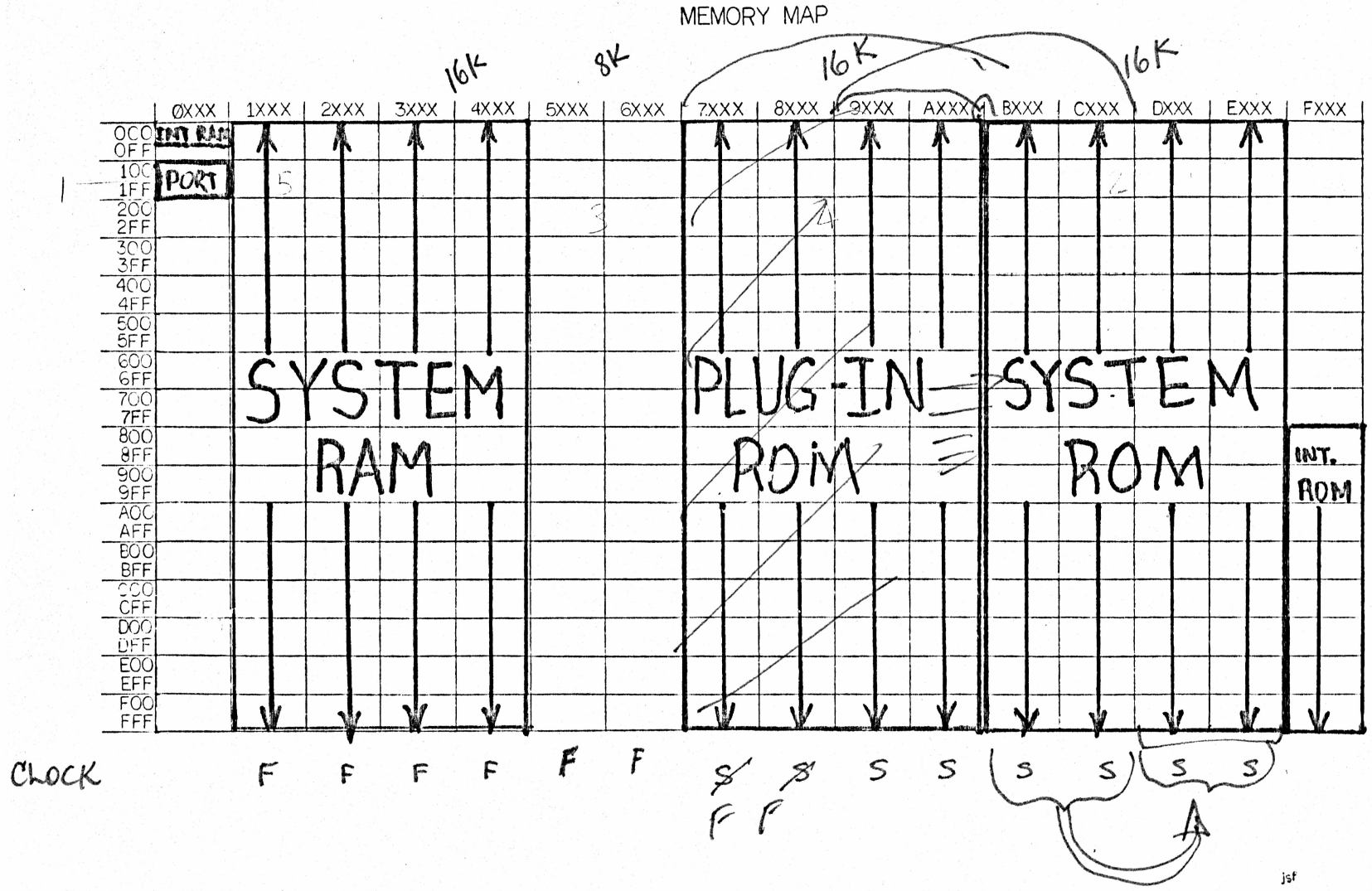
4-8K PAGES

MEMORY MAP



CMB 8/4/81

- SIMPLE CHANGE TO ~~ACHIEVE~~ MEMORY MAP CHANGE
- WRITE TO MAP REGISTER TO CHANGE SPEED
- ONE BIT TO SPEED UP PLUG-IN ROM SPACE



.ALC.DOC.PRODUCT.HWFUN

~~INTRO~~
ISSUES
LANGUAGE
OVERVIEW

LONESTAR HARDWARE FUNCTIONAL SPEC

SECTION 1 INTRODUCTION

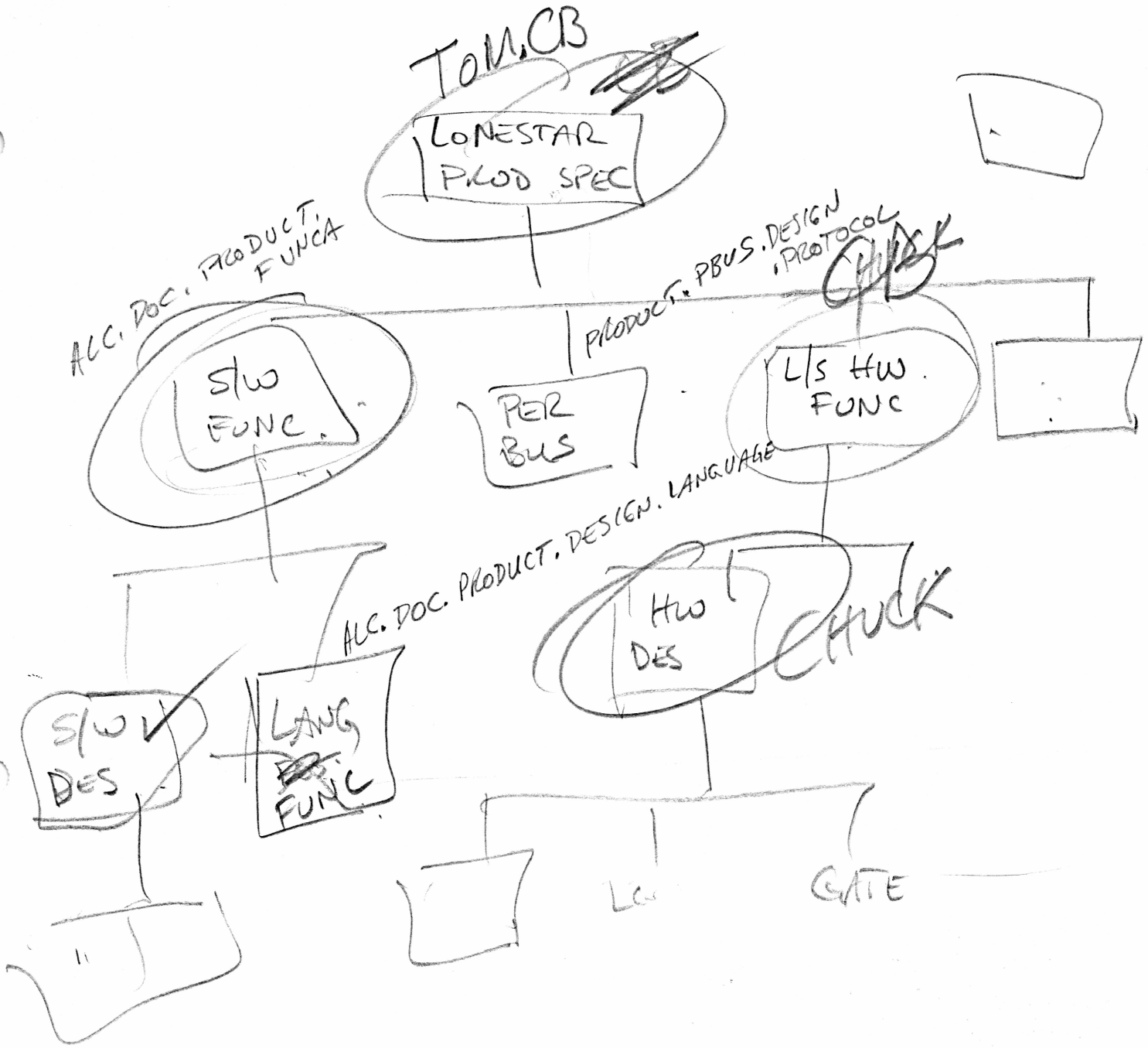
1.1 Purpose
1.2 Scope
1.3 Terminology
1.4 Related documents Gate Array.

SECTION 2 FUNCTIONAL DESCRIPTION. ~~OVERVIEW~~

2.1 SIZE AND STYLING - TILT
2.2 DISPLAY - overlays
2.3 KEYBOARD - OVERLAYS
2.4 POWER SYSTEM - POWER DOWN · LOW BATT · ADAPTER
2.5 ON/OFF & BREAK
2.6 PIEZO
2.7 MEMORY ORGANIZATION & EXPANSION
2.8 PLUG-IN MODULE
2.9 Peripheral ~~connection~~ expansion - conn, cable, power distribution
2.10 Packaging

~~SECTION 3~~ OPEN ISSUES AND SECTION 3 GOALS FOR ADDITIONAL FEATURES

3.1 PURPOSE
3.2 ~~CRADLE~~ SECURITY CRADLE
3.3 NIGHT BACK LIGHT HOOD
3.4



PRODUCT. PROOF LONESTAR INT PERF BUS S/W DESIGN

PREFACE

The following is a preliminary BML for the top PCB. It is subject to change at any time. Changes and corrections should be directed to Randy Ahlfinger X3215.

Memo
from

C. B. WILSON