MSG 39 915 ECJ FEJP CJP ALCC TO: RYOJI YONEMOTO.....FEJP

CC: YUICHI MURANO.....ECJ CHUCK BRANSON.....ALCC DARRELL WHITTEN.....HEXB

FM: C.B. WILSON.....ALC1

RE: 70020A

WE ARE STILL CONTINUING TO TRY TO FIND OUT WHAT THE REAL PROBLEM IS WITH THE SOFTWARE WE HAVE IN THE 70C20 FOR THE WAFERTAPE (GATE CODE L11001). AS I MENTIONED TO YOU WHEN I WAS IN JAPAN, WE GET A FAILURE USING THE ACTUAL PART THAT WE DON'T SEEM TO GET WHEN USING THE AMPL. SINCE THAT TIME WE HAVE FOUND A SERIOUS PROBLEM WITH OUR MACHINE LEVEL CODE, BUT THAT ERROR DOES NOT EXPLAIN WHY THE AMPL WORKS AND WE BELIEVE A SEPARATE PROBLEM IS RESPONSIBLE FOR THE ACTUAL FAILURE.

IN SEARCHING FOR THIS SECOND FAILURE, WE HAVE BEEN TESTING SOME CODE (WHICH DOES NOT USE THE MICROCODED INSTRUCTIONS OF THE L11001) ON THE 70C20A. WE ARE APPARENTLY SEEING A SUPRIZING FAILURE ON THESE 70C20A PARTS. THE FAILURE APPEARS TO BE THAT THE PART IS NOT ABLE TO BE INTERRUPTED OUT OF AN IDLE STATE WITH AN INTERRUPT 2 FROM THE TIMER. SPECIFICALLY, WE HAVE THE FOLLOWING CODE:

> MOVP %START,TIMER START = >AO, TIMER = >O3 MOVP %I2CS,IOCNTL I2CS = >4C, IOCNTL = >OO EINT CLR B IDLE BTJO %SETBIT,B,RSYNC8

THE FAILURE WE BELIEVE WE ARE SEEING IS THAT THE PART DOES NOT EVER COME OUT OF THE IDLE INSTRUCTION WHEN THIS IS EXECUTED. I AM NOT ABSOLUTELY SURE OF THIS BECAUSE WE HAVE ONLY A COUPLE OF 70C20A PARTS OVER HERE AND THIS WAS NOTICED LATE FRIDAY FOR THE FIRST TIME. WE HAVE SOME OTHER 70C20A PARTS OVER IN THE QUAL LAB WHICH I WILL GET BACK MONDAY AND WE WILL VERIFY AGAIN WITH MORE PARTS AND MAKE ABSOLUTELY SURE WE ARE NOT SEEING SOMETHING ELSE. IT IS DIFFICULT FOR ME TO IMAGINE THAT THE PART ACTUALLY HAS THIS TYPE OF FAILURE, BUT I WANTED TO ADVISE YOU OF OUR INFORMATION AND GET YOUR COMMENT.

I AM STILL INTERESTED VERY MUCH IN THE PROGRESS OF THE LOTS OF WAFERTAPE CODE ON THE 70C20A (GATE CODE L71000S). DO YOU HAVE ANY CHANGE TO THE 11/2 SHIPPING DATE FOR THESE PARTS?

BEST REGARDS, C.B. WILSON.....ALCC/ALC1 -MSG M#= 114706 FR=ALCC TO=ALCC SENT=10/14/83 06:55 PM R#=043 ST=C DIV=039 CC=0815 BY=JHPE AT=10/06/83 09:09 PM TO: C B WILSON - ECJ TO: JIM ARNORD -----ALCC CC: I KOIKE AKRI CC: Y UCHIDA / S SATO - FEJP RE: L11001 REPLY FOR YOUR TELEPHONE CALL ((DEVICE STATUS)) GATE CODE NEME OF C20A (PREVIOUSLLY CALLING L11001) IS L71000S. 2 LOTS OF L71000S PARTS ARE RUNNING AT OUR FRONT-END, AND SHIPPING COMMITMENT ARE AS FOLLOWS. SLICE OUT 10/26F.G OUT 11/1 SHIPPING 11/2PROBABLY SAME AS C71003 SHIPPING WHICH PARTS WERE PREVIOUSLLY CALLING THE GATE CODE C11006. ((FUNCTION DIFFERENCE BETWEEN C20A AND C20)) C20 C20A - PRIORITY OF INT CLR AND EN X 0 - ILLEGAL RELEASE OF IDLE STATE X n X ----- NOT CORRECT 0 ---- CORRECT = DETAILS OF PRIORITY OF INT CLR AND EN = I/O CONTROL REGISTOR SET "1 1" (CLR/EN AT THE SAME TIME), IN THIS CASE, IF INT INPUT IS ALREADY LATCHED AND INT FLG IS ACTIVE, IT IS ORDINARY MANNER TO CLEAR INT FLG PRIOR TO ACCEPT INTERRUPT WITH EN FLG="1" AND DISABLE INTERRUPT ACTION.

HOWEVER C20 WILL OCCASIONALLY PRIORITIZE EN BIT AND ACTIVE INTERRUPT DUE TO TIMING SKEW.

DETAILS OF ILLEGAL RELEASE OF IDLE STATE = WHEN CPU EXECUTES IDLE INSTRUCTION, CPU ENTERS INTO POWER SAVE MODE BY CLOCKHALT.THE RELEASE OF THIS STATE WILL BE DONE BY INT INPUT. IF THE INT INPUT NOT INFLUENCED BY INT BIT AT STATUS REGISTOR OR INT EN BIT IS USED, IT WILL CREATE THE PROBLEM. FOR EXAMPLE, AT THE STATE THAT INT3 IS DISABLE BY EN BIT OF I/O CONTROL REGISTOR, INT3 INPUT BECOMES ACTIVE FOR IDLE RELEASE, CPU NEVER ENTERS TO INT3 ROUTINE WHILE CLOCK KEEPS RUNNING.WHEN INT IS DISABLED BY INT BIT OF STATUS REGISTOR, THE SAME THING MAY HAPPEN.

BEST REGARDS. RYOJI YONEMOTO FEJP

MT358F	P10	MLP	FAMILY	ASSEMBL	.ER	1.0	16:	53: 51	10/13/80 PAG	BE 0046
	F504	02								
1067	F505	92 02		MOVP	В, Т	IME		2/3 bi	t timer	
1068	F507 F508	D5 31		CLR	СНК	SUM		set ch	ksum to ()
1069	F509 F50A	D5 30		CLR	СНК	SUM-1				
1070			*	COPY	AL	C. JCF. STRI	NGY. SRC. C	LDRINT	old mi	icrocode i
1071	F50B F50C	72 F7		MOV	%RE	ITDT/256, I	NT2V-1			
1072	F50E F50E	72 8A		MOV	%RB	ITDT-(256*	(RBITDT/2	256)), I	NT2V	
	F510	34								
1073			*	MOV	XR	DBIT1, INT2		set u	p INT2 op	code
1074			*	MOV	7.6	DBIT2, INT2	+1	set u	p INT2 pa	arameter
1075			*	CLR	IN	IT2+2		set u	p INT2 pa	arameter
1076	F511	A2		MOVP	%51	ART, TIMER		start	2/3 bit 1	timer
	F512	AO								
4077	F513	03								
10//	F514	AZ		MUVP	710	CS. TUCNIL		Select	& clear	INT2
	F515	40	-1-250-	15						
1078	F517	05		EINT				reinte	rruntidi	tu
1079	F518	C5		CLR	B			TEST		
1080	F519	01	sleepm	IDLE				TEST	•	
1081	F51A	56		BTJO	%SE	TBIT, B, RSY	NCB	test f	or 1	
	F51B	08								
	F51C	05								
1082	F51D	C5	RSYNC		B			TEST		
1083	FSIE	57		BT.17	700	TRIT. P. POV	NCO	test f	0	
1004	F520	08		DIVL	/	IBITI BIRBI	146.7	UESU T	ur u	
	F521	07								
1085	F522	C5	RSYNCE	3 CLR	B			TEST		
1086	F523	01		IDLE				TEST		
1087	F524	57		BTJZ	%SE	TBIT, B, RSY	NC7	test f	or O	
	F525	08								
1000	F 326	FO	DECTN	IMD	DEC	White			1/	
1000	F528	89	REDINF		REa	TINC		IT CWO	1.5 10 6	TOW
1089			* test	for 2	more	05				
1090	F529	C5	RSYNC	CLR	B			TEST		
1091	F52A	01		IDLE				TEST		
1092	F52B F52C	56 08		BTJO	%SE	TBIT, B, RES	INK	test f	or 1	
1000	F520	F9			_			TRAT		
1093	FJZE	01		LR	В			TEET		
1095	F530	56		BT.ID	755	TRIT. B. PES	TNIK	test f	or 1	
	F531	08		5100		10117071120		0050 1		
	F532	F4								
1096	F533	72		MOV	%4,	BITCON		bitcon	will hav	e been 1
	F534	04								
	F535	02								
1097	F536	EE		TRAP	BIT	BBA		wait e	nd of nit	ble (spac
1098			* regi	ster A	w111	have been	swapped	(space	r only)	

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0204		*				
0205		* wafer	drive	control	constant equat	es
0206	OOFE	INITOR	EQU	SEE		initialize drive
0207	0001	TNTTHE	FOU	>01		initialize wafer ddr
0208	0053	MT	FOU	DE3		turn on motor & sensor
0208	0009	MTRAP	EQU	200		turn off motor
0207	0008	MTUE	EQU	208		turn on motor, WF & sens
0210	OUFI	MIWE	EGU	2F1		toinstate DO
0211	0000	RENITW	EQU	200		
0212	OOFB	SN	EQU	>FB		turn on Eul/Bul sensor
0213	OOFB	STOP	EQU	>FB		turn off drive except se
0214	00F9	WE	EQU	>F9		turn on WE & sensor
0215		* wafer	test (contant	equates	
0216	0040	BATTRY	EQU	>40		bit-test for battery-lev
0217	0002	EOTTST	EQU	>02		bit-test for EDT
0218	0080	INPUT	EQU	>80		bit-test for input data
0210	0004	LIP	FOU	>04		bit-test for WP
0217	0004	Wi unfor	data .	roncatni	equates	
0220	0004	* warei	- uata	Lunsaund	, equaves	wafer-write invert
0221	0001	INVBIT	EGO	201		stand a Util bit
0222	0008	SETBIT	EQU	>08		store a l'Dit
0223		*				
0224		* bus a	control	constar	nt equates	
0225	0001	DROP	EQU	>01		drop HSK bit
0226	0000	HSKSET	EQU	>00<		let HSK float
0227	0004	INHIB	EQU	>04		inhibit IBC
0228	0001	RELEAS	EQU	>01		release-HSK bit
0229	0001	+ hus i	test ro	nstant (ouates	
0220	0001	HEK	FOIL	201		bus readu bit-test
0230	0001	TRA	EQU	200		hus data readu hit-test
- 0231	0008	ING	EGU	200		BAV active test
0000	~~~~					
0232	0002	BAV	EGU	202		
0232	0002	8AV *	EGO	>02		
0232 0233 0234	0002	BAV *	COPY	ALC. JCF	. STRINGY. SRC. M	HZ358
0232 0233 0234 B0001	0002	BAV *	COPY	ALC. JCF	. STRINGY. SRC. M	HZ358
0232 0233 0234 B0001 B0002	0002 000D	* timer BITIME	COPY const EQU	ALC.JCF ant equa >OD	STRINGY. SRC. M ates 3. 58MHz, 8KBaud	HZ358 data half-bit time
0232 0233 0234 B0001 B0002 B0003	0002 000D 0020	* time BITIME HALT	COPY const EQU EQU	ALC. JCF ant equa >OD >20	5. STRINGY. SRC. M ates 3. 58MHz, 8KBaud	HZ358 data half-bit time stop timer
0232 0233 0234 B0001 B0002 B0003 B0004	0002 000D 0020 00C0	* time BITIME HALT HRANGE	COPY const EQU EQU EQU	ALC. JCF ant equa >OD >20 >C0	5. STRINGY. SRC. M ates 3. 58MHz, 8KBaud 3. 58MHz	HZ358 data half-bit time stop timer high time/low freq cutof
0232 0233 0234 B0001 B0002 B0003 B0004 B0005	0002 000D 0020 00C0 0038	* time * time BITIME HALT HRANGE LRANGE	COPY const EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >C0 >38	5. STRINGY. SRC. M ates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0004	0002 0020 0020 00C0 0038 00BF	* time * time BITIME HALT HRANGE LRANGE MAX	EQU COPY Const EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >C0 >38 >BF	5. STRINGY. SRC. M ates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0004 B0005	0002 0020 0020 0020 0038 00BF 0006	* time * time BITIME HALT HRANGE LRANGE MAX DRANGE	EQU COPY EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >C0 >38 >BF >06	5. STRINGY. SRC. M ates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0004 B0005 B0004 B0007 B0008	0002 0020 0020 0000 0038 00BF 0004 0000	* time * time BITIME HALT HRANGE LRANGE MAX ORANGE SLEEP	EQU COPY EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00	5. STRINGY. SRC. M ates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0006 B0007 B0008 B0009	0002 0020 0020 0000 0038 008F 0004 0000	* timen BITIME HALT HRANGE LRANGE MAX ORANGE SLEEP	COPY Const EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00	5. STRINGY. SRC. Mates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0004 B0005 B0006 B0007 B0008 B0007	0002 0020 0020 0000 0038 00BF 0004 0000 00A0	* timen BITIME HALT HRANGE LRANGE MAX ORANGE SLEEP START	COPY const EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00 >A0	5. STRINGY. SRC. M ates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0005 B0005 B0007 B0008 B0007 B0008	0002 0020 0020 0000 0038 008F 0004 0000 00A0	* timen BITIME HALT HRANGE LRANGE MAX ORANGE SLEEP START * softu	COPY const EQU EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00 >A0 >A0 >CO	5. STRINGY. SRC. M ates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 4. 58MHz 5. 58MHz	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0004 B0007 B0008 B0007 B0008 B0007 B0010 B0011	0002 0020 0020 0000 0038 00BF 0006 0000 00A0	* timen BITIME HALT HRANGE LRANGE MAX ORANGE SLEEP START * soft BOSTIM	COPY const EQU EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00 >A0 >A0 >A0 >A0 >A0	5. STRINGY. SRC. Mates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 400 tants 3. 58MHz 5. 58MHz	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit wait valid sync (150 ms)
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0004 B0005 B0007 B0008 B0007 B0008 B0007 B0010 B0011 B0012	0002 0020 0020 0020 0038 008F 0004 0000 00A0 00A0	* timen BITIME HALT HRANGE LRANGE MAX ORANGE SLEEP START * softu BOSTIM BOTIME	COPY const EQU EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00 >A0 >A0 >67 >B6	5. STRINGY. SRC. Mates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 400 tants 3. 58MHz 3. 58MHz 3. 58MHz	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit wait valid sync (150 ms) BOT past head (300 ms)
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0004 B0005 B0006 B0007 B0008 B0007 B0008 B0007 B0010 B0011 B0012 0235	0002 0020 0020 0020 0020 0020 0020 002	* timen BITIME HALT HRANGE LRANGE MAX ORANGE SLEEP START * soft BOSTIM BOTIME *	COPY const EQU EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >20 >CO >38 >BF >06 >00 >A0 >A0 >A0 >67 >B6 ALC. JCF	5. STRINGY. SRC. Mates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 4 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 5. STRINGY. SRC. M	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit wait valid sync (150 ms) BOT past head (300 ms) HZ5
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0004 B0005 B0006 B0007 B0008 B0007 B0008 B0007 B0010 B0011 B0012 0235 0236	0002 0020 0020 0000 0038 00BF 0006 0000 00A0 00A0	* timen BITIME HALT HRANGE LRANGE MAX ORANGE SLEEP START * softu BOSTIM BOTIME *	COPY Const EQU EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00 >A0 >A0 >A0 >A0 >A0 >B6 ALC. JCF	5. STRINGY. SRC. Mates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 4. 5. 58MHz 3. 58MHz 3. 58MHz 5. 58MHz 5. STRINGY. SRC. M	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit wait valid sync (150 ms) BOT past head (300 ms) HZ5
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0006 B0007 B0008 B0007 B0008 B0007 B0010 B0011 B0012 0235 0236 0236	0002 0020 0020 0000 0038 008F 0006 0000 00A0 00A0	<pre># time1 # time1 BITIME HALT HRANGE LRANGE MAX ORANGE SLEEP START * softu BOSTIM BOTIME * * ***</pre>	COPY Const EQU EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00 >A0 >A0 >A0 >A0 >A0 >A0 >A0 >A0 >A0	5. STRINGY. SRC. Mates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 4 5. 58MHz 5. 58MHz 5. STRINGY. SRC. M	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit wait valid sync (150 ms) BOT past head (300 ms) HZ5
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0006 B0007 B0008 B0007 B0008 B0007 B0010 B0011 B0012 0235 0236 0237 0238	0002 0020 0020 0000 0038 008F 0006 0000 00A0 0067 0086	<pre># time1 # time1 BITIME HALT HRANGE LRANGE MAX ORANGE SLEEP START * softu BOSTIM BOTIME * * *</pre>	COPY Const EQU EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >O6 >O0 >A0 >A0 >A0 >A0 >A0 >A0 >A0 >A0 >A0 >A	5. STRINGY. SRC. Mates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 4. 4. 5. 58MHz 5. 58MHz 5. STRINGY. SRC. Materials 5. STRINGY. SRC. F 5. STRINGY. SRC. P	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit wait valid sync (150 ms) BOT past head (300 ms) HZ5
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0006 B0007 B0008 B0007 B0008 B0007 B0010 B0011 B0012 0235 0236 0237 0238 C0001	0002 0020 0020 0000 0038 008F 0006 0000 00A0 00A0	<pre># times # times BITIME HALT HRANGE LRANGE LRANGE MAX ORANGE SLEEP START # softs BOSTIM BOTIME # # # # # # #</pre>	COPY COPY EQU EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00 >A0 >A0 >A0 >A0 >A0 >A0 >A0 >A0 >A0	5. STRINGY. SRC. Mates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 4. 4. 5. 58MHz 5. 58MHz 5. 58MHz 5. STRINGY. SRC. M 5. STRINGY. SRC. F 5. STRINGY. SRC. P clear constant	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit wait valid sync (150 ms) BOT past head (300 ms) HZ5 E equates
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0006 B0007 B0008 B0007 B0008 B0007 B0010 B0011 B0012 0235 0236 0236 0237 0238 C0001 C0002	0002 0020 0020 0000 0038 00BF 0006 0000 00A0 00A7 00B6	<pre># times # times BITIME HALT HRANGE LRANGE LRANGE MAX ORANGE SLEEP START # softs BOSTIM BOTIME # # # # # # # # # # # # # # # # # # #</pre>	EQU COPY EQU EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00 >A0 >A0 >A0 >A0 >A0 >A0 >A0 >A0 >A0	5. STRINGY. SRC. Mates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 4. 58MHz 5. 58MHz 5. 58MHz 5. STRINGY. SRC. M 5. STRINGY. SRC. F 5. STRINGY. SRC. P clear constant	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit wait valid sync (150 ms) BOT past head (300 ms) HZ5 E equates clear and select INT1
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0006 B0007 B0008 B0007 B0008 B0007 B0010 B0011 B0012 0235 0236 0237 0238 C0001 C0002 C0003	0002 0020 0020 0020 0020 0038 008F 0006 0000 0000 0000 00047 0086	<pre># timen BITIME HALT HRANGE LRANGE LRANGE MAX ORANGE SLEEP START * softu BOSTIM BOTIME * * * inter I1CS I1230</pre>	COPY EQU EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00 >AO >AO >AO >AO >AO >AO >AO >AO >AO >AO	STRINGY. SRC. Mates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 5. 58MHz 5. STRINGY. SRC. M 5. STRINGY. SRC. F 5. STRINGY. SRC. P clear constant	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit wait valid sync (150 ms) BOT past head (300 ms) HZ5 E equates clear and select INT1 clear INT1, 2&3 flags
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0006 B0007 B0008 B0007 B0008 B0007 B0010 B0011 B0012 0235 0236 0237 0238 C0001 C0002 C0003	0002 0020 0020 0020 0020 0038 008F 0006 0000 0000 0000 00040 0067 0086	<pre># timen BITIME HALT HRANGE LRANGE LRANGE MAX ORANGE SLEEP START * softu BOSTIM BOTIME * * * inter I1CS I123C I2C</pre>	COPY EQU EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00 >AO >AO >AO >AO >AO >AO >AO >AO >AO >AO	STRINGY. SRC. Mates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 5. 58MHz 5. STRINGY. SRC. M 5. STRINGY. SRC. F 5. STRINGY. SRC. P clear constant	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit wait valid sync (150 ms) BDT past head (300 ms) HZ5 E equates clear and select INT1 clear INT1, 2&3 flags clear INT2 flag
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0004 B0007 B0008 B0007 B0008 B0007 B0010 B0011 B0012 0235 0236 0237 0238 C0001 C0002 C0003 C0004	0002 0020 0020 0020 0020 0020 0020 002	<pre># timen BITIME HALT HRANGE LRANGE LRANGE MAX ORANGE SLEEP START * softu BOSTIM BOTIME * * * inter I1CS I123C I2C</pre>	COPY EQU EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00 >AO >AO >AO >AO >AO >AO >AO >AO >AO >AO	STRINGY. SRC. Mates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 5. 58MHz 5. STRINGY. SRC. M 5. STRINGY. SRC. F 5. STRINGY. SRC. P clear constant	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit wait valid sync (150 ms) BOT past head (300 ms) HZ5 E E equates clear and select INT1 clear INT1, 2&3 flags clear INT2 flag clear and select INT2
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0005 B0005 B0007 B0008 B0007 B0008 B0007 B0010 B0011 B0012 0235 0236 0237 0238 C0001 C0002 C0003 C0004 C0005	0002 0020 0020 0020 0020 0038 008F 0006 0000 0000 0000 0000 00040 0067 0086	<pre># timen BITIME HALT HRANGE LRANGE LRANGE MAX ORANGE SLEEP START * softu BOSTIM BOTIME * * * inter I1CS I123C I2CS I2CS</pre>	COPY EQU EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00 >AO >AO >AO >AO >AO >AO >AO >AO >AO >AO	STRINGY. SRC. Mates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 4. 58MHz 5. 58MHz 5. 58MHz 5. STRINGY. SRC. M 5. STRINGY. SRC. P clear constant	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit wait valid sync (150 ms) BOT past head (300 ms) HZ5 E E equates clear and select INT1 clear INT1, 2&3 flags clear and select INT2 test INT2 select bit
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0005 B0005 B0007 B0008 B0007 B0008 B0007 B0010 B0011 B0012 0235 0236 0237 0238 C0001 C0002 C0003 C0004 C0005 C0006	0002 0020 0020 0020 0038 008F 0006 0000 00A0 00A0 0067 00B6	* timen BITIME HALT HRANGE LRANGE LRANGE MAX ORANGE SLEEP START * soft BOSTIM BOTIME * * * inter I1CS I123C I2CS I2S	COPY EQU EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00 >AO >AO >AO >AO >AO >AO >AO >AO >AO >AO	STRINGY. SRC. Mates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 5. STRINGY. SRC. M 5. STRINGY. SRC. F 5. STRINGY. SRC. P clear constant	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit wait valid sync (150 ms) BOT past head (300 ms) HZ5 E E equates clear and select INT1 clear INT1, 2&3 flags clear INT2 flag clear and select INT2 test INT2 select bit
0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0005 B0005 B0007 B0008 B0007 B0010 B0011 B0012 0235 0236 0237 0238 C0001 C0002 C0003 C0004 C0005 C0006 C0007	0002 0020 0020 0020 0038 008F 0006 0000 00A0 00A0 00A7 00B6 0043 0064 0043 0064 0048 0046	* timen BITIME HALT HRANGE LRANGE MAX ORANGE SLEEP START * soft BOSTIM BOTIME * * * * * * inter I1CS I123C I2CS I2S I2S I23C	COPY EQU EQU EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00 >AO >AO >AO >AO >AO >AO >AO >AO >AO >AO	5. STRINGY. SRC. Mates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 5. STRINGY. SRC. M 5. STRINGY. SRC. F 5. STRINGY. SRC. P clear constant	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit wait valid sync (150 ms) BOT past head (300 ms) HZ5 E E equates clear and select INT1 clear INT1, 2&3 flags clear and select INT2 test INT2 select bit clear INT2&3 flags
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0232 0233 0234 B0001 B0002 B0003 B0004 B0005 B0005 B0005 B0007 B0008 B0007 B0010 B0011 B0012 0235 0236 0237 0238 C0001 C0002 C0003 C0004 C0005 C0006 C0007 C0008 C0007	0002 0020 0020 0020 0038 008F 0004 0004 0040 0047 0086 0043 0064 0048 0042 0044 0048 0046 0048 0046	* timen BITIME HALT HRANGE LRANGE MAX ORANGE SLEEP START * softu BOSTIM BOTIME * * * * * * * * * * * * * * * * * * *	COPY COPY EQU EQU EQU EQU EQU EQU EQU EQU	ALC. JCF ant equa >OD >20 >CO >38 >BF >06 >00 >A0 >A0 >A0 >A0 >A0 >A0 >A0 >A0 >A0	5. STRINGY. SRC. Mates 3. 58MHz, 8KBaud 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 3. 58MHz 5. STRINGY. SRC. M 5. STRINGY. SRC. P clear constant	HZ358 data half-bit time stop timer high time/low freq cutof low time/high freq cutof max timer, no sleep bit to bit compare sleep mode timer-start bit wait valid sync (150 ms) BOT past head (300 ms) HZ5 E E equates clear and select INT1 clear INT1,2&3 flags clear INT2 flag clear and select INT2 test INT2 select bit clear INT2&3 flags clear and select INT2&3 clear INT3 flag