/BEGIN
/S 10
/C(IBC-I)
/S 2
/C(INTELLIGENT BUS CONTROLLER)
/S 2
/C(DATA MANUAL)
/S 12
/BEGIN INSERT
Texas Instruments
Consumer Products Group

5/10/82
/END INSERT
/DOCUMENT(IBC-I Data Manual)
/PRELIMINARY
/PB
/P1(INTRODUCTION)
/P2(DESCRIPTION)
/P
The IBC-I (Intelligent Bus Controller) is a interface device which provides capability for interfacing target system or microprocessor to the ALC peripheral bus. It will provide cost/performance advantages over discrete implementation and relieve software from numerous tasks which are necessary to supervise the bus.
/P2(KEY FEATURES)
/* 4 BIT INSTRUCTION/DATA WORD
/* FULLY COMPATIBLE WITH TMS-7000, 8085 AND 6502 MPU families
/* EASY INTERFACE TO MOST 4 BIT MICROCONTROLLERS
/* 5 MODES OF OPERATION
/* CAPABILITY TO LATCH CS AND RS SIGNALS
/* PROGRAMMABLE INTERRUPT WITH OPEN DRAIN OUPUT
/* TTL/CMOS COMPATIBLE PINS
/* LOW POWER CMOS, 3 - 7 VOLT POWER SUPPLY
/* 22-PIN, 400-MIL, DUAL-IN-LINE PLASTIC PACKAGE
/PB
/P1(ARCHITECTURE)
/P2(BLOCK DIAGRAM)
/P
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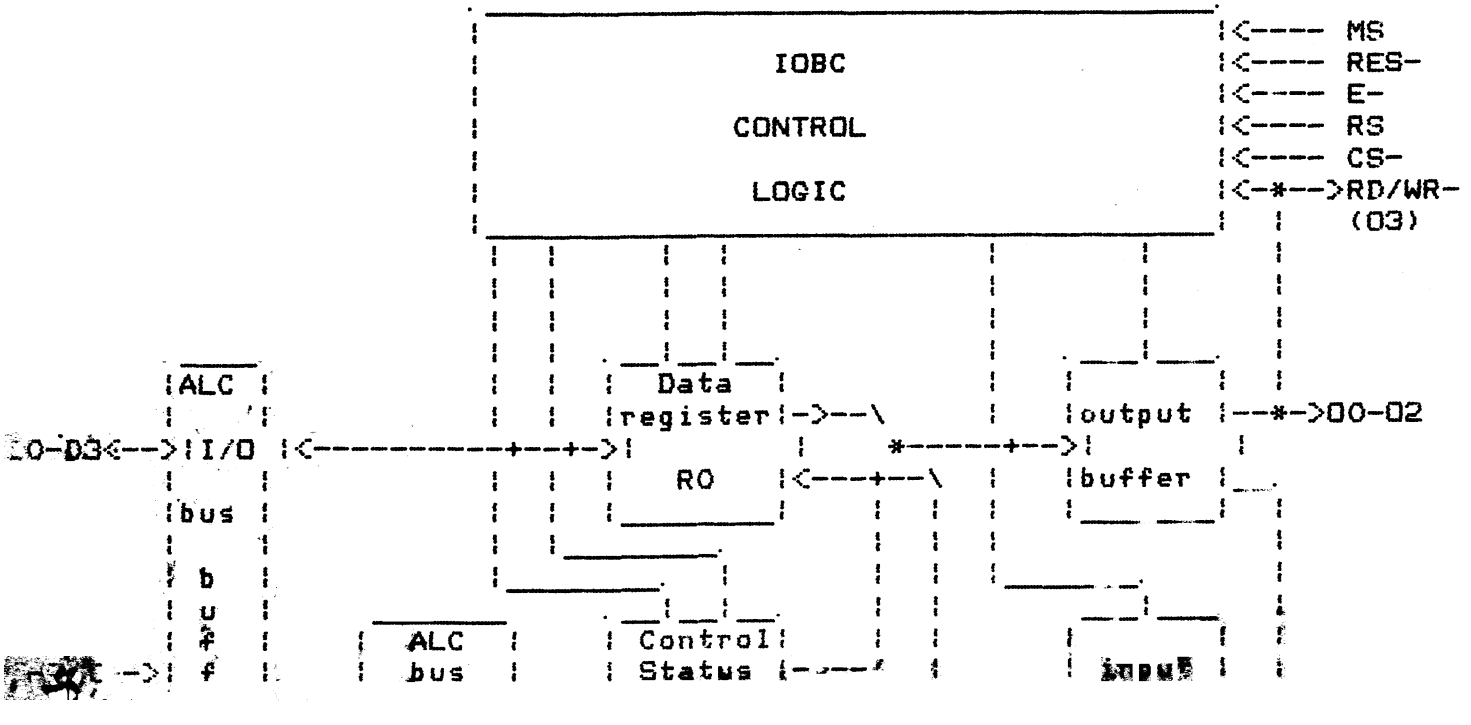

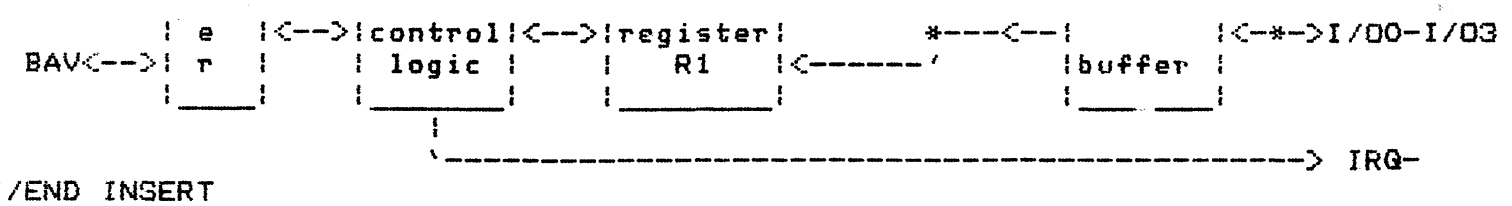

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/P2(REGISTERS)
/P
The IBC-I has four registers which are accessible to the user. All registers are 4-bit wide. Table 1 shows addressing technique used to access each register. The Control Register is used to manipulate HSK and BAV lines. The mode of operation (Inhibit, Disable and Enable) is determined by the Control Register, which is depicted in Figure 1. The Status Register is used to indicate to the processor the status of HSK and BAV lines and the state of Interrupt request and the Inhibit flag. The Status Register is shown in Figure 2. Transmit and Receive Data Registers are 4-bit buffers into and from the ALC's I/O Bus.
/P2(INTERRUPT)
/P
The IBC-I has an interrupt which indicates when the data is available on the bus. Interrupt can be disabled completely or until the next message. The interrupt output is open drain with a low active level. The pull-up resistor value is between 3.3 K and 4.7 K Ohms.
/PB
/BEGIN INSERT

Table 1. Addressing Technique.

CS-	RS	WRITE	READ
0	0	Transmit Data Register	Receiver Data Register
0	1	Control Register	Status Register

Figure 1. CONTROL REGISTER FORMAT

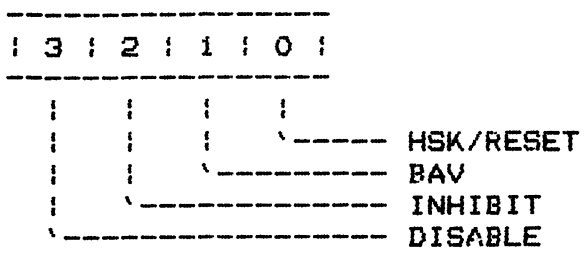
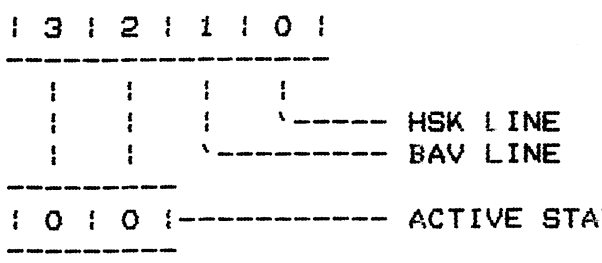


Figure 2. Status Register Format



```
                                  --------
                                  | 1 | 0 |---------- ACTIVE IRQ
                                  --------
                                  | 1 | 1 |---------- START OF MESSAGE
                                  --------

                                    3   2   1   0
                                  ----------------
                HARDWARE RESET    | 0 | 1 | X | X |
                                  ----------------
```

/END INSERT
/PB
/P2(MODES OF OPERATION)
/P
The IBC-I can operate in five different modes which allows simple interface with several popular microprocessors families.
The desired mode can be selected by setting the Mode Select input (MS).
If input MS is set low four modes can be selected by setting pins O-0 and O-1. Table 2 shows the modes selected by different bit patterns on these two pins.
/P
In addition, when MS is set low, setting pin O-2 will enable the latching capability for CS and RS signals. This feature is useful for multiplex address/data bus similar to TMS-7000 or INTEL-8085.
In this mode ALATCH is connected to the RS pin and a positive strobe on ALATCH will latch the level on I/O-0 pin as internal RS and the level on CS pin as internal CS which should be high to select the chip.
The configuration of interface and timing shown in Figure 7.
/P
If the MS is set high the IBC-I is in Mode 5 and reconfigured as shown in Figure 8.
This mode is useful with 4-bit MPUs which don't have a bidirectional bus.
Please note that pin R/W- is used as MSB of the output data.
/BEGIN INSERT

Table 2. Modes of Operation.

O-2	O-1	O-0	MODE DESCRIPTION
0	0	0	Mode 0 - ENABLE active low (see Figure 3) TMS-7000 compatible
0	0	1	Mode 1 - ENABLE active high (see Figure 4) 6500 compatible
0	1	0	Mode 2 - accepts RD- and WR- signals (see Figure 5) 8085 and 8048 compatible
1	X	X	Modes 4,5,6 - control signals for R/W- and E- correspond to non-multiplex modes 0,1,2 but addressing arranged for multiplex busses.

/END INSERT
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Figure 3-a. Mode 0 Interface Configuration.

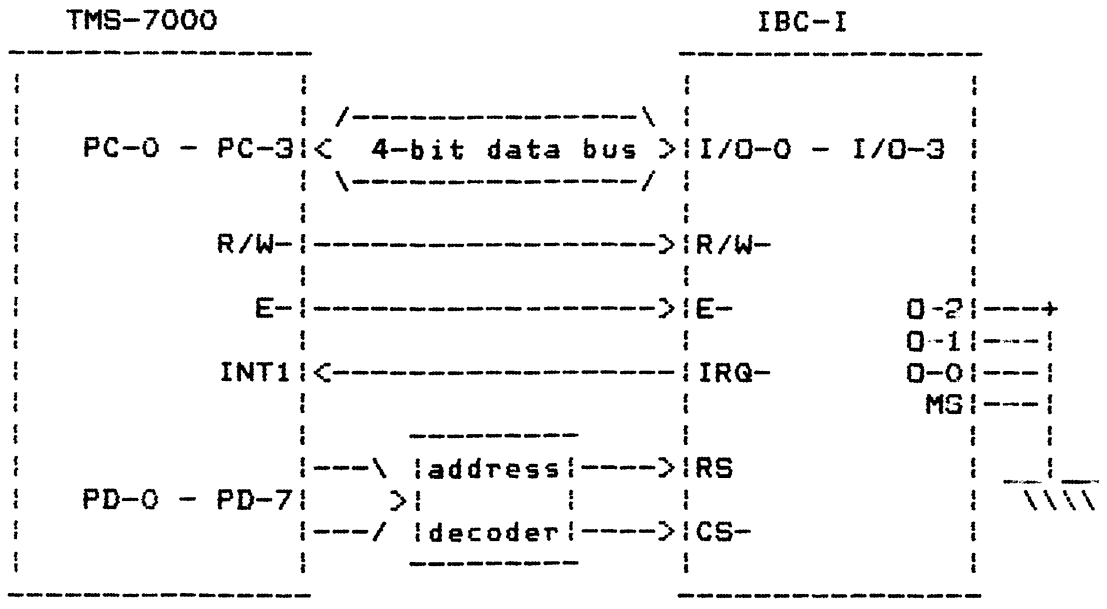
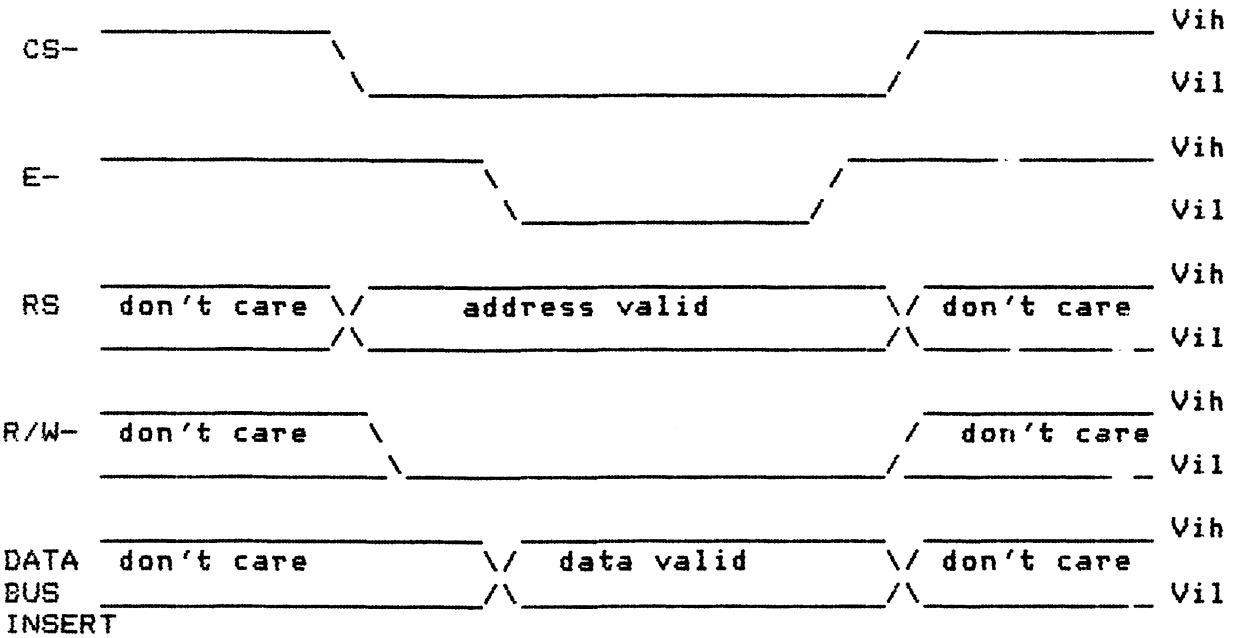


Figure 3-b. Write Timing Characteristics.



/END INSERT
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/S 5
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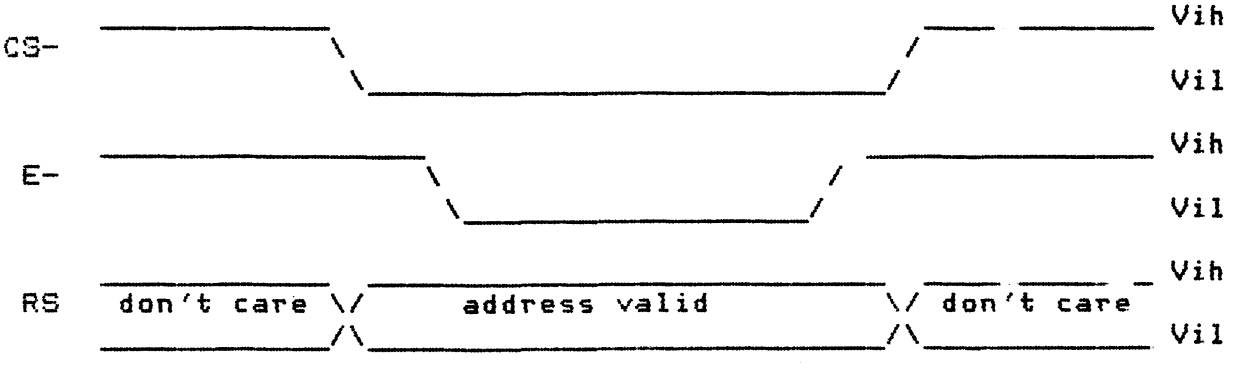
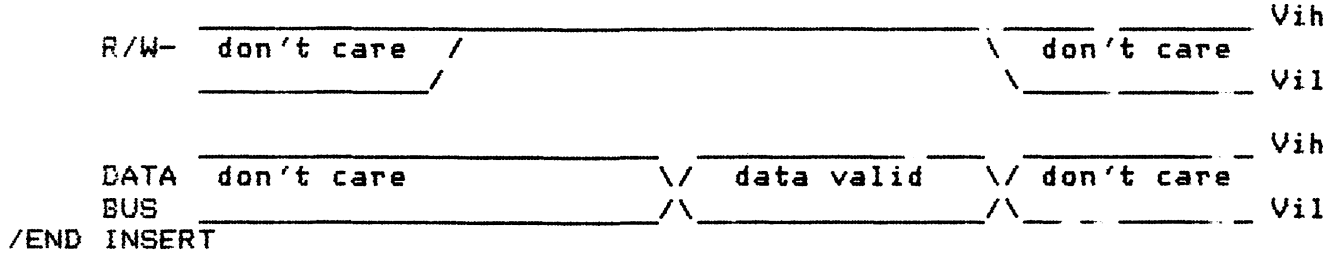
Figure 3-c. Read Timing Characteristics.





/END INSERT
/PB
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Figure 4-a. Mode 1 Interface Configuration.

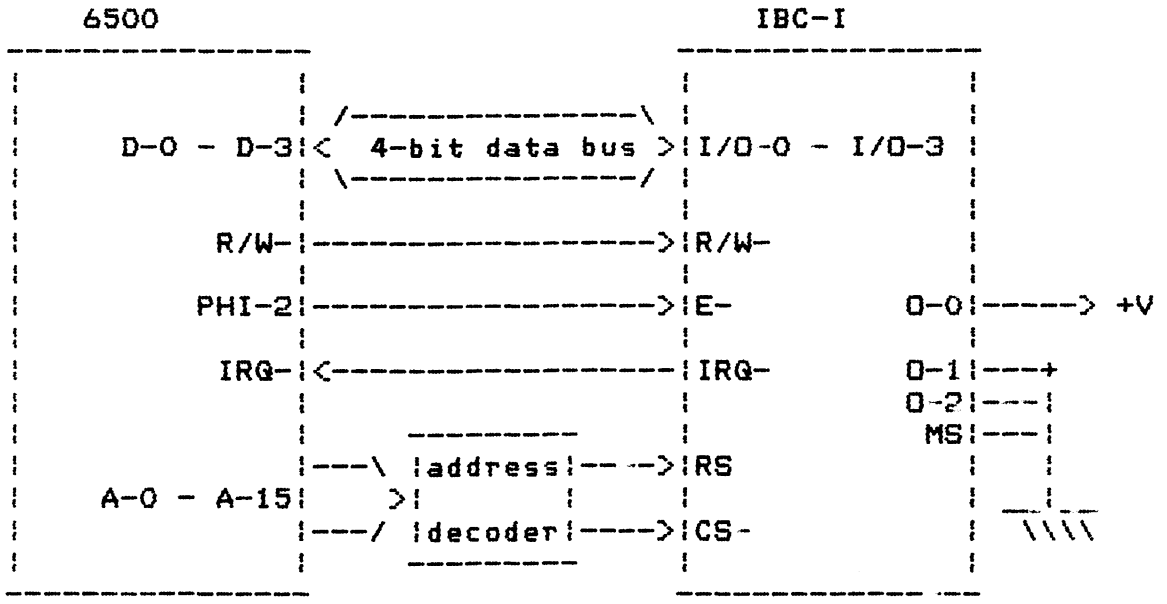
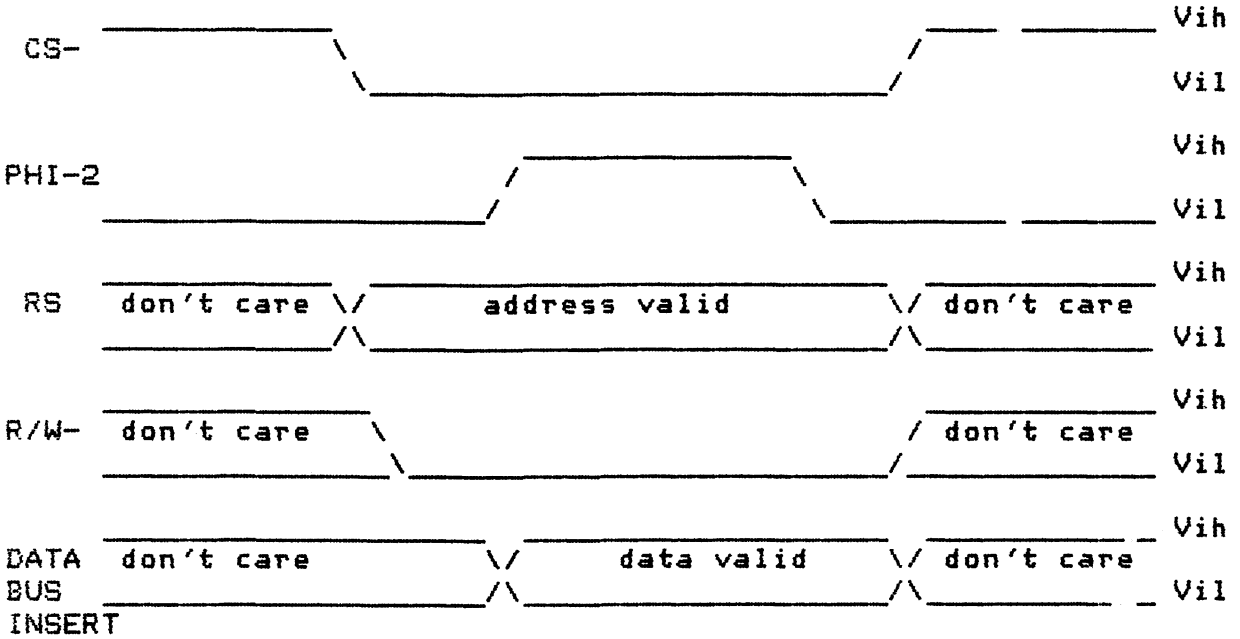
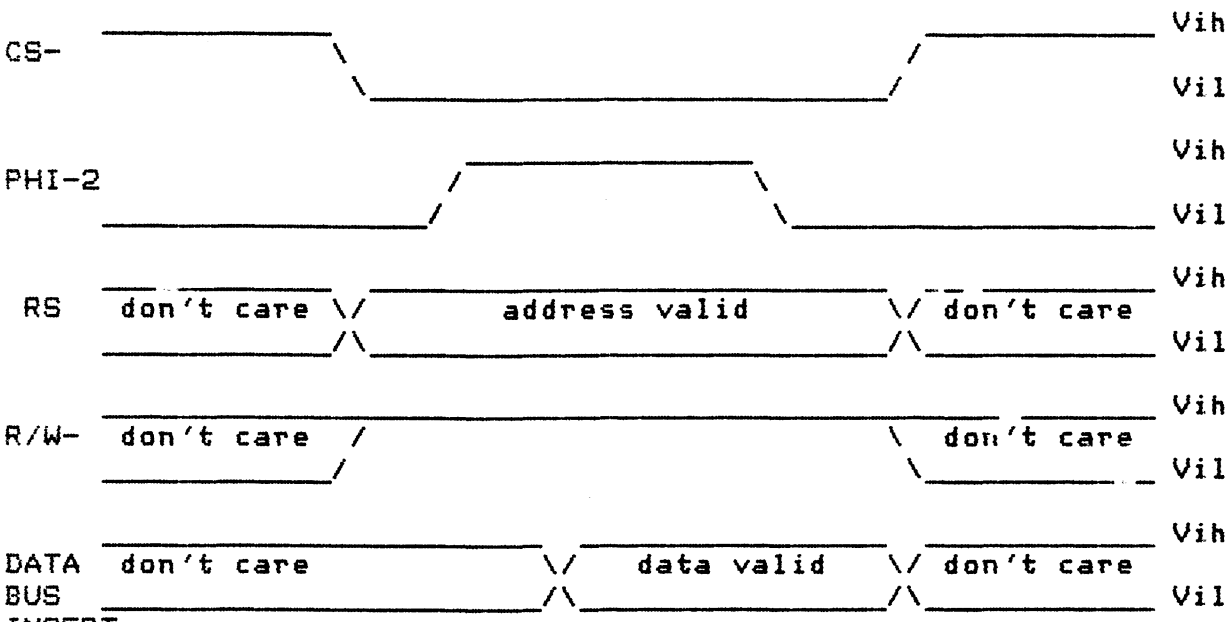


Figure 4-b. Write Timing characteristics.



/END INSERT
/PB
/S 5
/BEGIN INSERT

Figure 4-c. Read Timing Characteristics.



/END INSERT
/PB
/BEGIN INSERT

Figure 5-a. Mode 2 Interface Configuration.

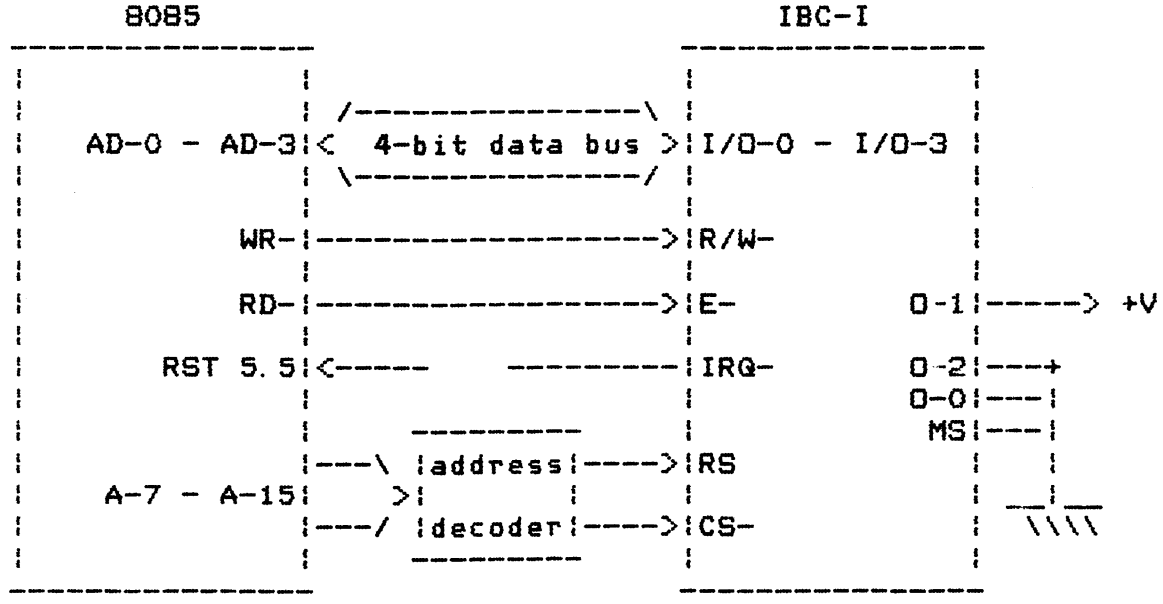
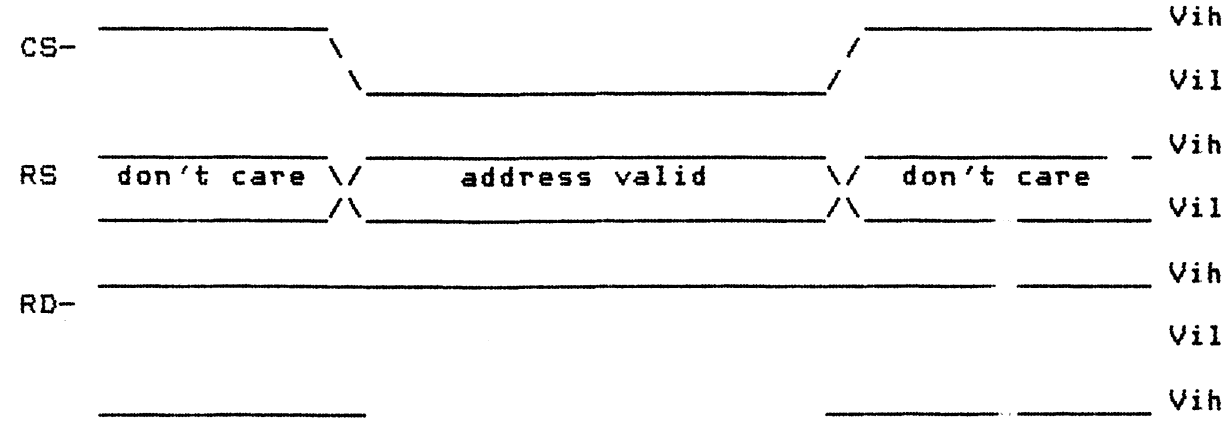
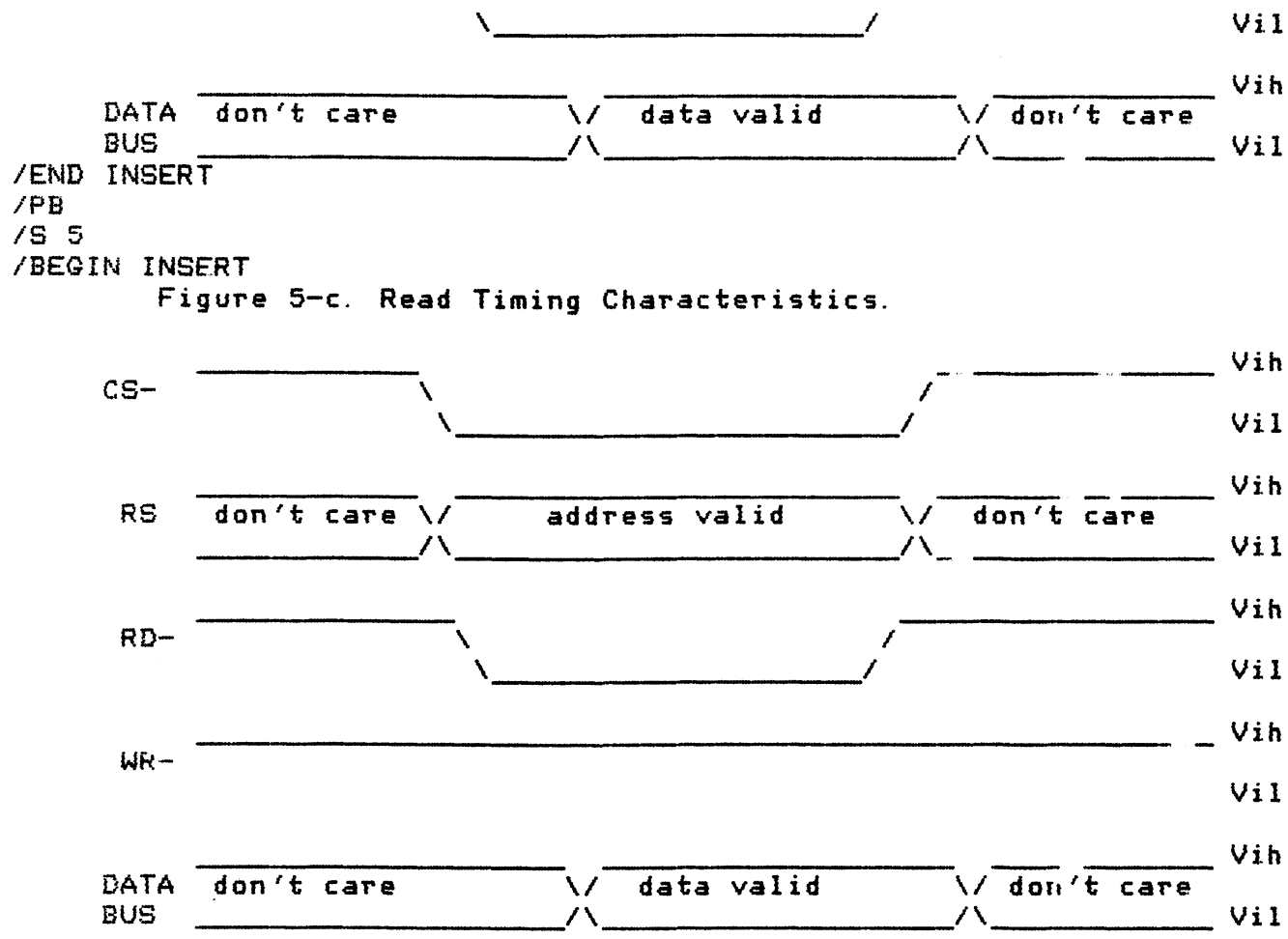


Figure 5-b. Write Timing characteristics.





/END INSERT
/PB
/S 5
/BEGIN INSERT

Figure 5-c. Read Timing Characteristics.

/END INSERT
/PB
/BEGIN INSERT

Figure 7-a. Latched Interface Configuration (Modes 4,5,6).

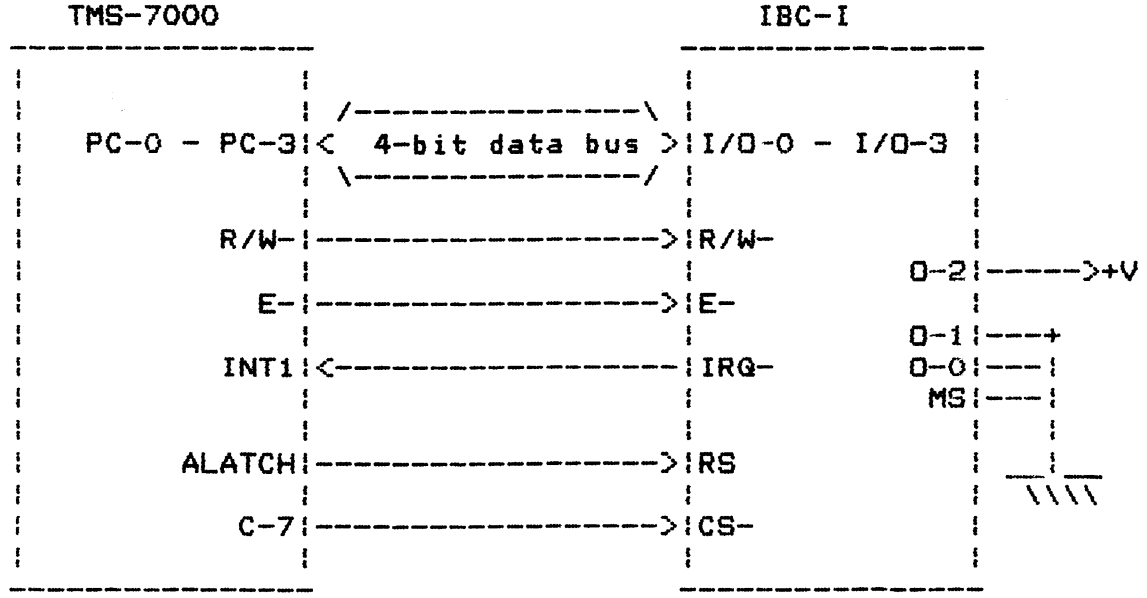
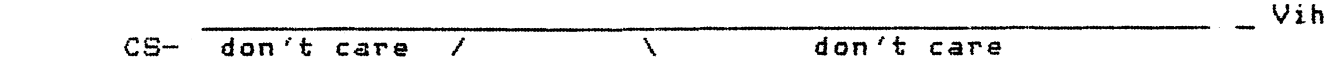
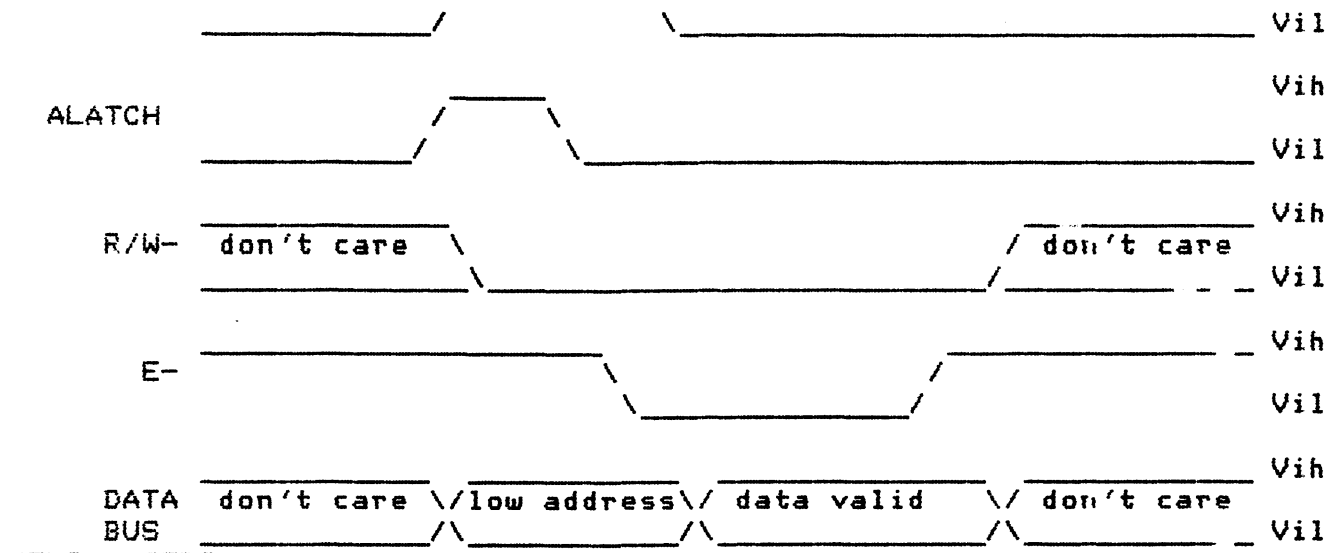


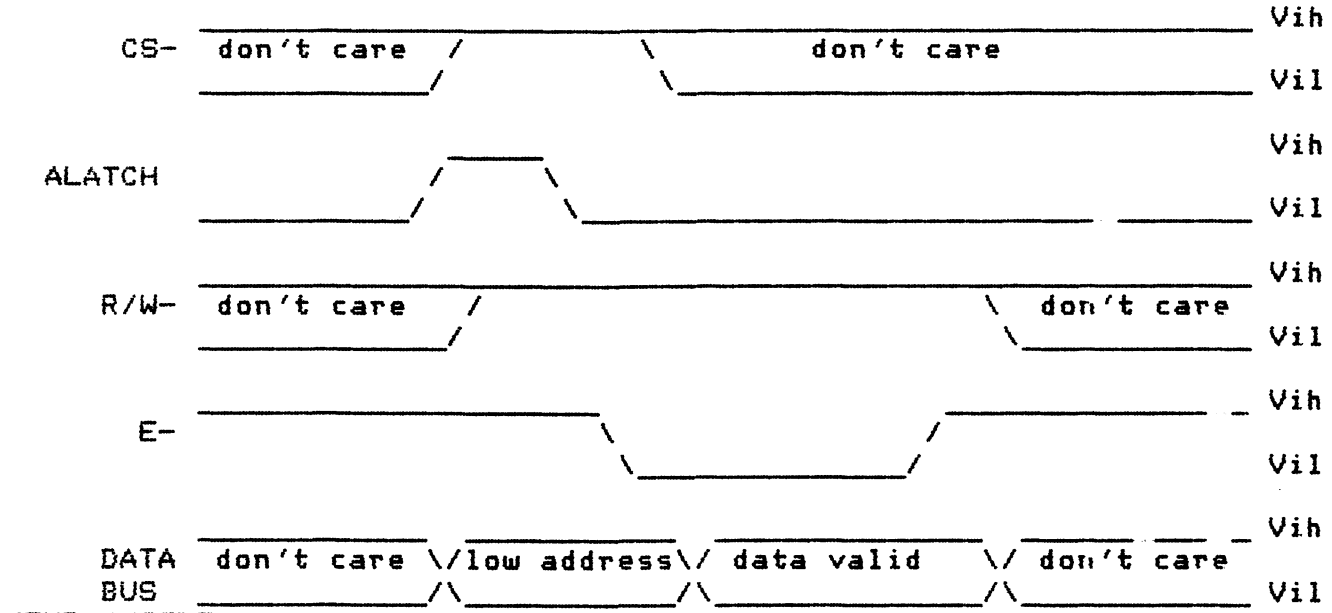
Figure 7-b. Write Timing Characteristics.





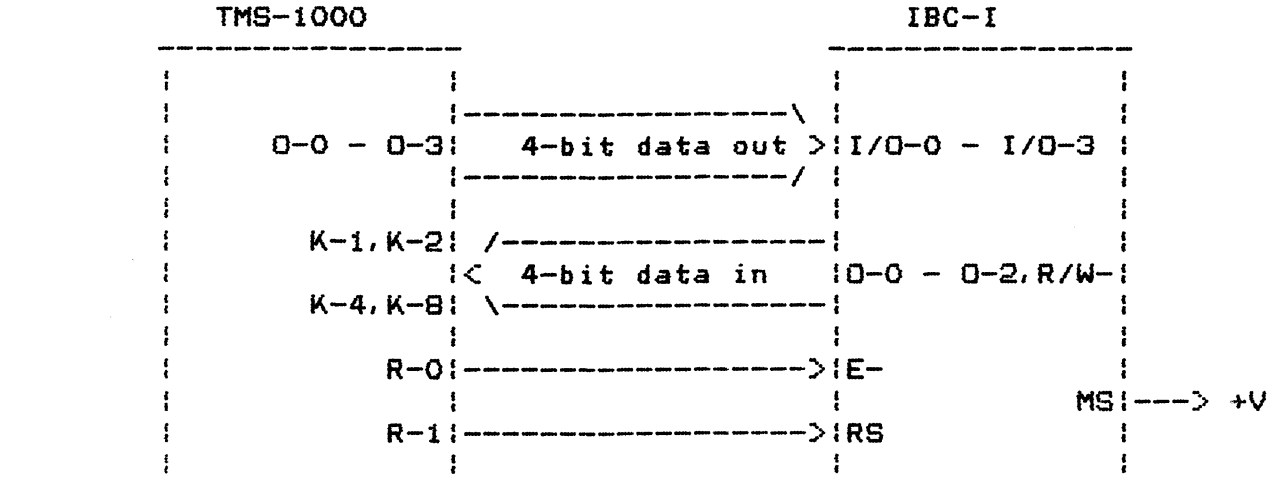
/END INSERT
/PB
/S 5
/BEGIN INSERT

Figure 7-c. Read Timing Characteristics.



/END INSERT
/PB
/BEGIN INSERT

Figure 8-a. Mode 5 Interface Configuration.



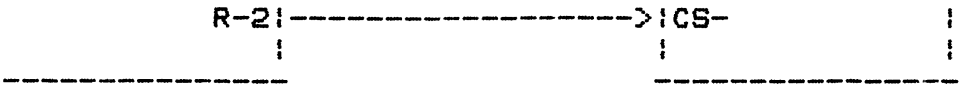
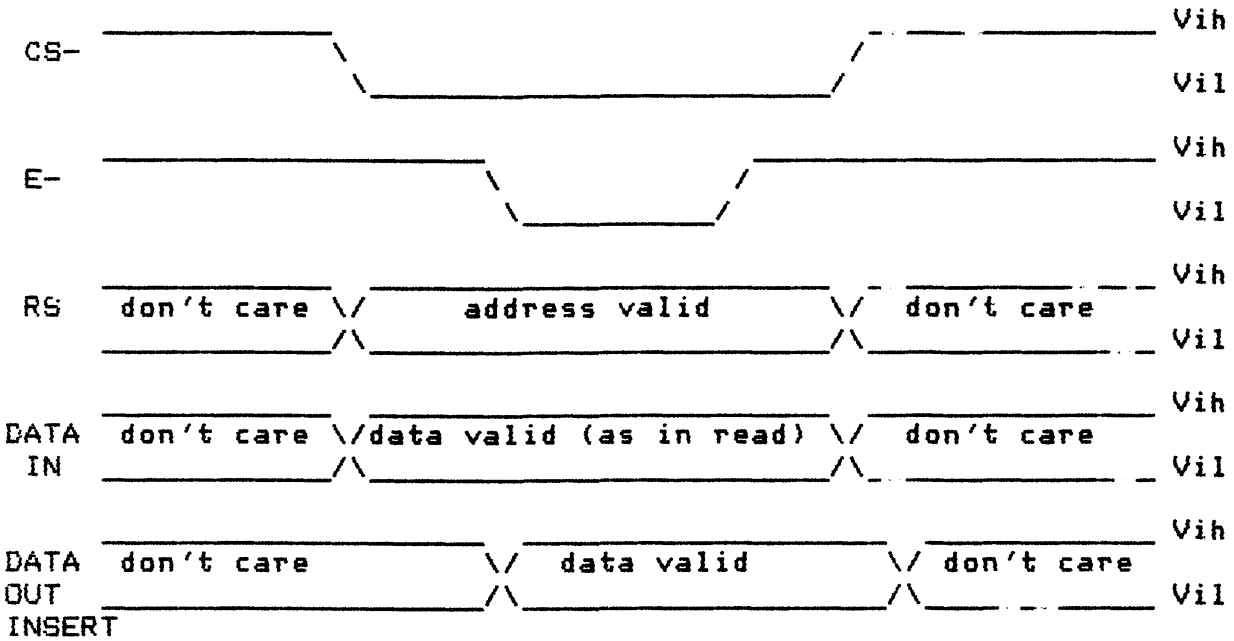
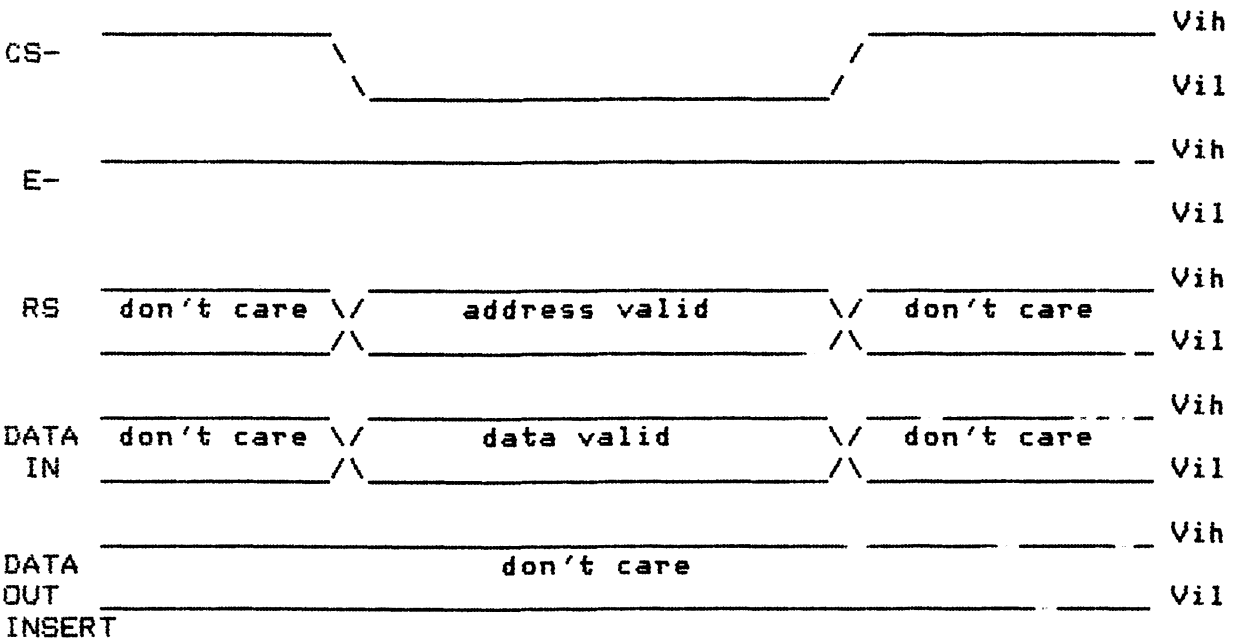


Figure 8-b. Write Timing Characteristics.



/END INSERT
/PB
/S 5
/BEGIN INSERT

Figure 8-c. Read Timing Characteristics.



/END INSERT
/PB
/P1(IBC-I FUNCTIONAL OPERATION)
/P2(POWER-UP CONSIDERATIONS)
/P
If system's power up reset is tied to the RESET pin on IBC-I the controller will come up in the Disable state which means that transitions on HSK line will not be stored and no interrupt will be generated. In order to enable the controller, the user has to Write "XXXX0000" into Control Register. However it might not be

desirable to enable the controller in the middle of the message therefore user may perform Enable with "Inhibit Until New Message" by Writing "XXXXO1OO" into Control Register. This will keep the controller in disable state until a new message starts.
/P2(SLAVE MODE)
/P
In listen mode user has to read the first two nibbles on the bus, determine if he was selected, and if he was, user can start communication with the master. If he was not selected user should perform "Inhibit Until New Message" by Writing "XXXXO1OO" into the Control Register.
/P
The capability exists for the user to monitor the communication even if he was not selected, however, this is not recommended since it may slow down the bus operation. This allows monitoring and recording of all bus communications.
/P
In transmit mode, the user has to send the data utilizing the Write Sequence, monitor the HSK line and when the HSK line goes into an inactive state the user may transmit the next data.
/P
When the user has a need to request service from the master and has permission to do so, the user may execute Request Service which is described in a later section.
/P
All receive data and transmit data can be handled by executing the Read and Write Sequences respectively. These sequences are described below.
/PB
/P2(READ SEQUENCE)
/P
The Read Sequence allows the user to obtain the data transmitted on the bus and prepares IBC-I to receive the next transmission.
The Read Sequence has to be used whenever the user is in the listen mode and receives an interrupt from IBC-I.
/BEGIN INSERT

a - Reset Interrupt - Write "XXXXOOO1" into Control Register
b - Obtain Data - Read Receiver Data Register
c - Reset HSK Latch - Write "XXXXOOOO" into Control Register

Figure 9. Read Sequence.
/END INSERT
/P2(WRITE SEQUENCE)
/P
The Write Sequence allows the user to place the data on the bus and to signal the other devices that the data is available.
The Write Sequence has to be used whenever the user is in transmit mode and ready to send the data.
/BEGIN INSERT

a - Prepare Data - Write Data into Transmit Data Register
b - Set HSK Signal - Write "XXXXOOO1" into Control Register
c - Reset HSK Signal - Write "XXXXOOOO" into Control Register

Figure 10. Write Sequence.
/END INSERT
/P2(REQUEST SERVICE SEQUENCE)
/P
The Request Service Sequence allows the user to signal the master by putting the BAV line into the low state until the first HSK transition.
The Request Service Sequence may be used whenever the user has permission from the master to request the service.
/BEGIN INSERT

a - Set BAV signal - Write "XXXX0010" into Control Register
b - Enable BAV Reset - Write "XXXX0000" into Control Register

Figure 11. Request Service Sequence.

/END INSERT
/PB
/P2(MASTER-SLAVE DIFFERENCES)
/P
The difference between master and slave modes of operation exists because in master mode the user has to hold the BAV line low during the entire message. Therefore the Read and Write Sequences shown above must be modified for master mode operation. The modification requires that all accesses to the Control Register must maintain the BAV bit in the high state (see Figure 11 below).
/BEGIN INSERT

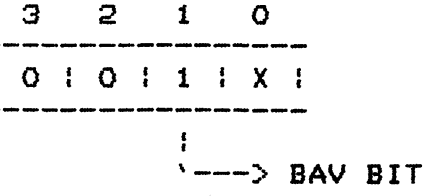


Figure 12. Control Register in Master Mode.

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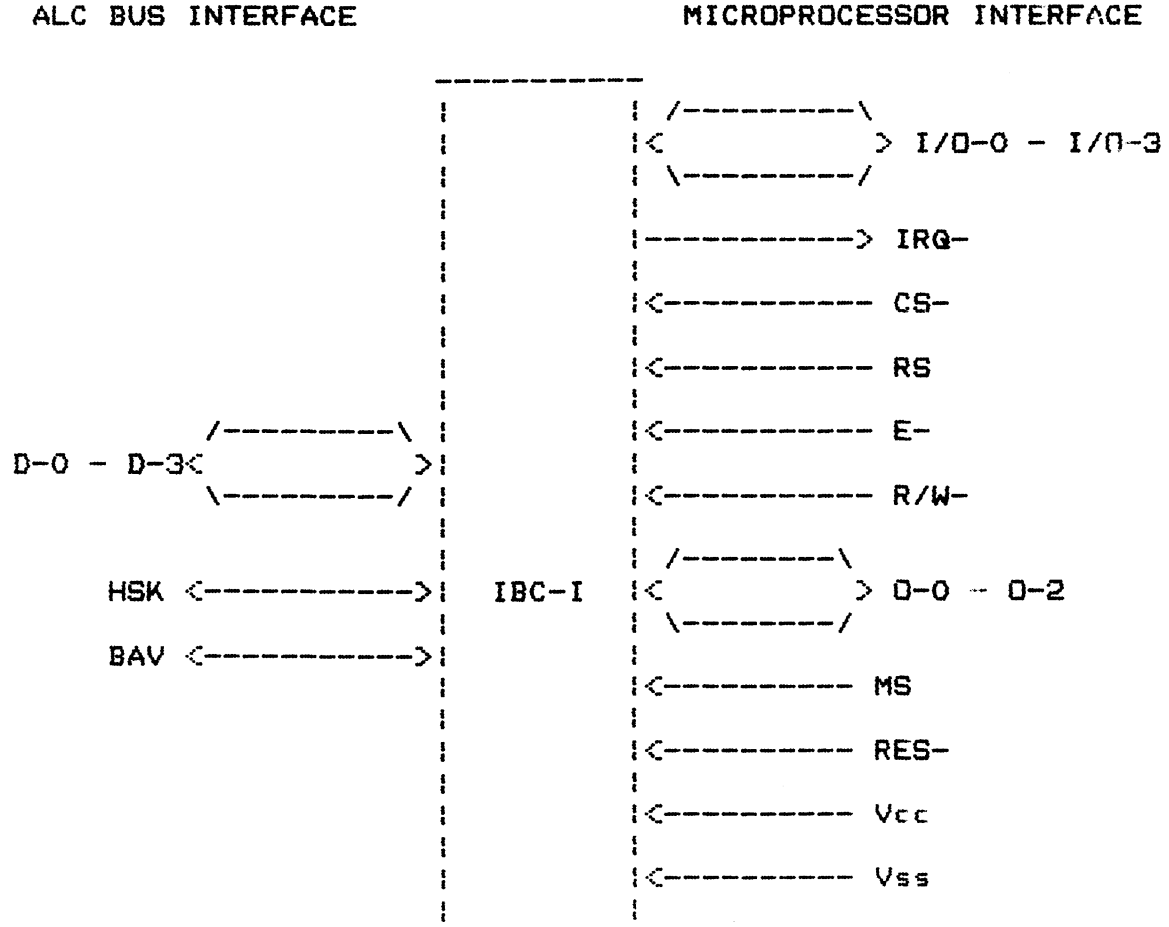
/P2(PIN DESCRIPTION)
/P
/BEGIN INSERT



/END INSERT
/PB
/S 5
/BEGIN INSERT

Name	I/O	PIN #	Description
D-0 - D-3	I/O	14, 15, 16, 17	Data I/O lines that allow data transfer between IBC-I and the ALC I/O bus.
HSK	I/O	6	HANDSHAKE LINE: set low by source device to indicate to listeners that there is valid data on the ALC I/O bus and held low by the listeners until they accept the data.
BAV	I/O	5	BUS AVAILABLE LINE: set low by source device in the beginning of the message and held low until the end of the message. The new source can originate a new message or "Request Service" only if this line is high.
I/O-0 - - I/O-3	I/O	1, 2, 3, 4	Data I/O lines that allow data transfer between IBC-I and the microprocessor. If MS=1 act as inputs only.
IRQ-	O	7	INTERRUPT OUTPUT (open drain): indicates to to the microprocessor the occurence of the next data nibble on the ALC I/O bus.
CS-	I	12	CHIP SELECT INPUT: selects and enables the IBC-I for microprocessor data transfer.
RS	I	13	REGISTER SELECT INPUT: address line through which the IBC-I registers can be accessed by the microprocessor.

/END INSERT
/PB
/S 5
/BEGIN INSERT

Name	I/O	PIN #	Description
E-	I	8	ENABLE INPUT: if MS=0 there are several options in combination with a pin R/W- for controlling data transfer between IBC-I and the microprocessor. If MS=1, E- is used as active low strobe for writing data into IBC-I. For details see text.
R/W-	I/O	11	READ-WRITE CONTROL: if MS=0 there are several options in combination with a pin E- for controlling direction of data transfer between IBC-I and the microprocessor. If MS=1, R/W- is used as most significant bit of data outputs. For details see text.
O-0 - O-2	I/O	20,	OUTPUT DATA LINES: if MS=1 these lines are

		21, 22	used as three least significant bits of data outputs. If MS=0 these lines are used for selecting the options for pins R/W-, E- and IRQ-.
MS	I	18	MODE SELECT: input which selects the mode of operation.
RES-	I	10	RESET INPUT: low level on this input will put IBC-I into reset state.
Vdd	I	19	Positive supply (4.5 - 9.5 Vdc).
Vss	I	9	0 Volt reference.

/END INSERT
/END