IOBC 1

PRELIMINARY SPECIFICATIONS

FOR ALC I/O BUS CONTROLLER

Texas Instruments
Consumer Products Group

12/16/81

1. General Description

* SMALL PACKAGE - 22 pin DIP

* SINGLE VOLTAGE WIDE RANGE POWER SUPPLY
  ... 3 to 12 Volts proposed ...

* TTL - CMOS COMPATIBILITY ON MPU INTERFACE

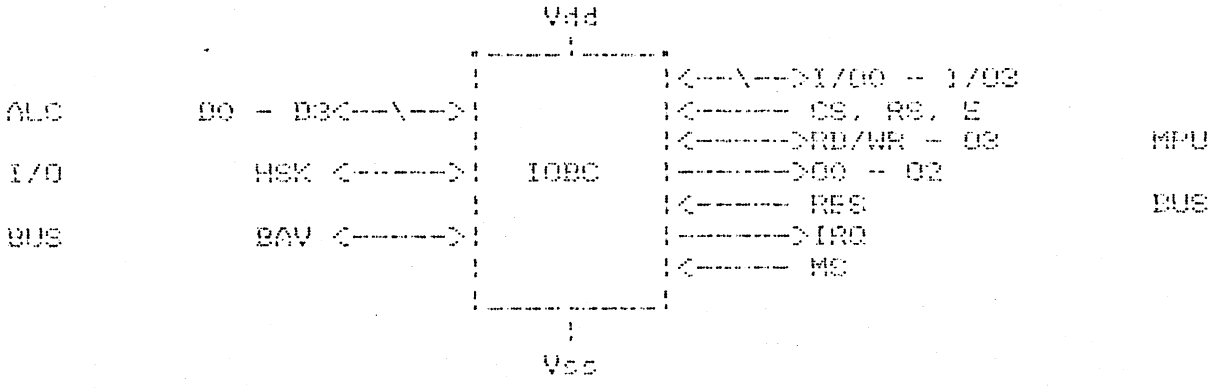
* SATISFIES ALC I/O BUS REQUIREMENTS

* EASY INTERFACE TO POPULAR MICROPROCESSORS

* HIGH SPEED OPERATION
  ... will work with 5 MHz TMS-7000 ...

* 2 MODES OF OPERATION AND TEST MODE

2. SIGNAL DESCRIPTION - MPU BUS INTERFACE



* I/00 - I/03 - BIDIRECTIONAL DATA BUS
  ... WHEN MS=1, USED AS INPUTS ONLY ...

* CS, RS, E - CONTROL LINES FOR DATA TRANSFER

* RD/WR - CONTROL LINE FOR DIRECTION OF DATA TRANSFER
  ... WHEN MS=1, USED AS MSB OF DATA OUTPUT ...

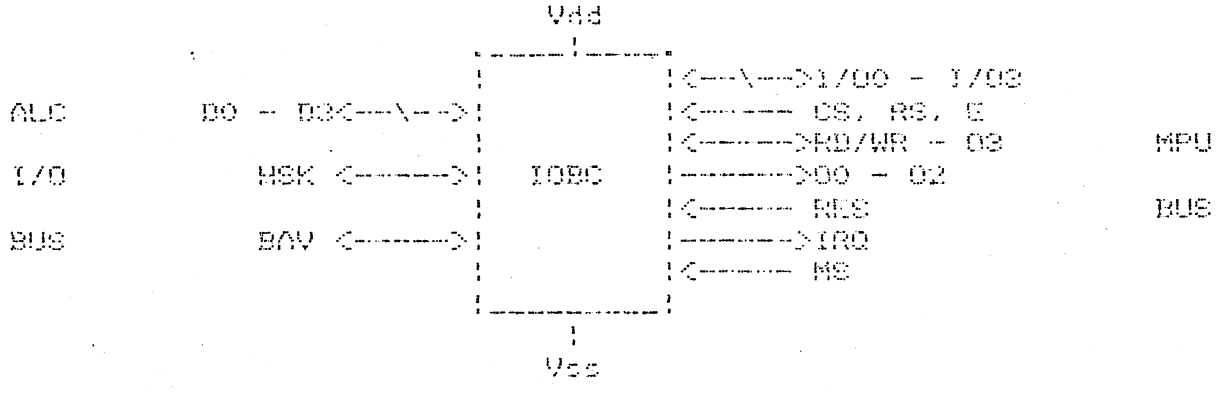
* 00 - 02 - USED AS DATA OUTPUTS WHEN MS=1

* RES - RESET/POWER UP CLEAR INPUT

* IRQ - INTERRUPT REQUEST WITH WIRED-OR CAPABILITY

* MS - MODE SELECT INPUT

3. SIGNAL DESCRIPTION - ALC I/O BUS INTERFACE



* D0-D3 - BIDIRECTIONAL DATA LINES

* HSK - BIDIRECTIONAL HANDSHAKE LINE

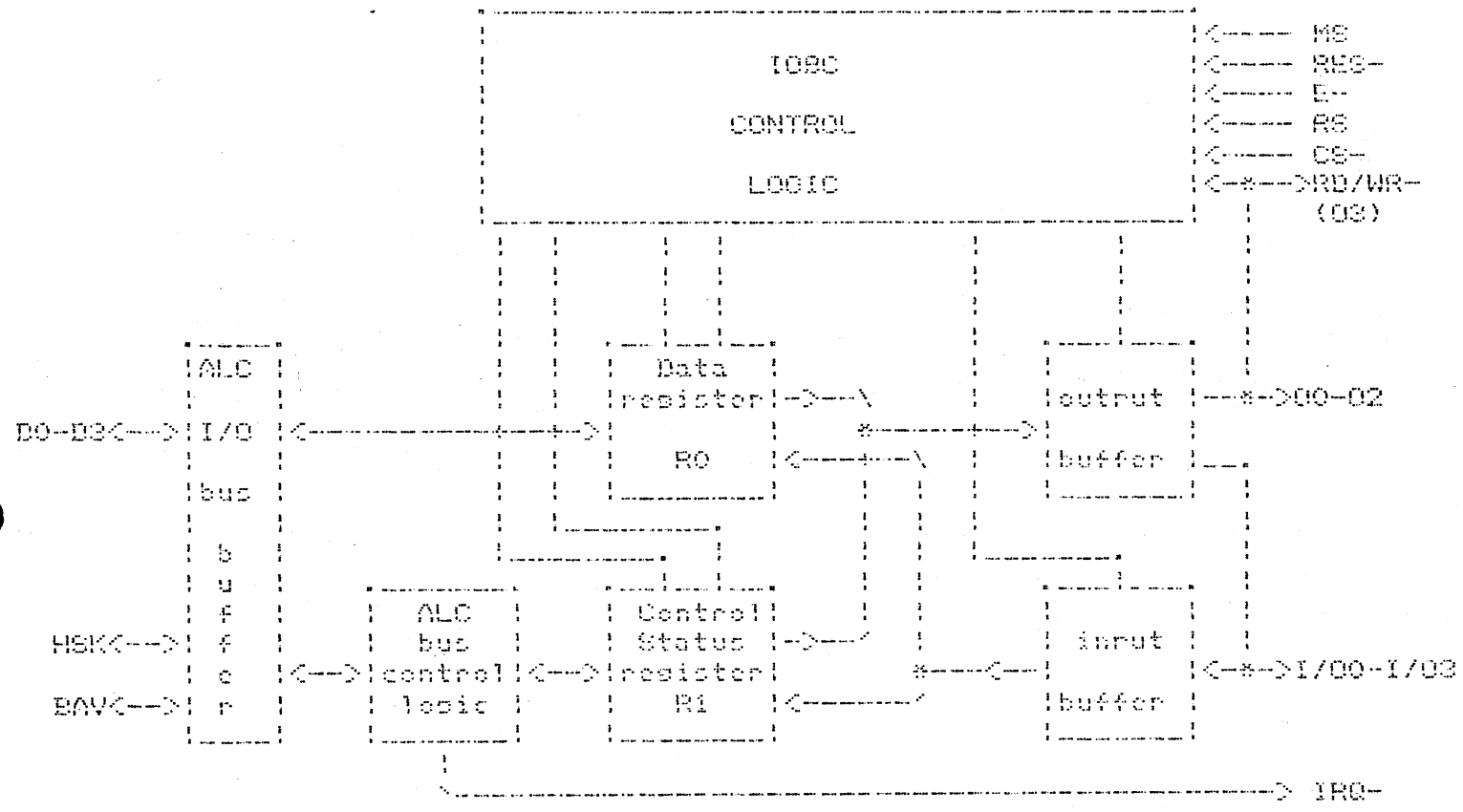
* BAV - BIDIRECTIONAL BUS-AVAILABLE LINE

* REMARKS:

  - ALL MPU INTERFACE OUTPUTS HAVE 3-STATE CAPABILITY

  - ALL ALC I/O INTERFACE LINES HAVE OPEN DRAIN OUTPUTS AND AND HIGH VOLTAGE PROTECTED INPUTS

4. INTERNAL DESCRIPTION



5. INTERNAL REGISTERS

* DATA REGISTER
... 4-BIT READ/WRITE REGISTER, ADDRESSED AS R0 (RS=0) ...

* CONTROL REGISTER
... 4-BIT WRITE-ONLY REGISTER, ADDRESSED AS R1 (RS=1 RD/WR=0) ...

MSB	3	2	1	0	LSB
				!	HSK/RESET
			!		BAV
		!			INHIBIT
	!				TEST

* STATUS REGISTER
... 4-BIT READ-ONLY REGISTER, ADDRESSED AS R1 (RS=1 RD/WR=1) ...

MSB	3	2	1	0	LSB
				!	HSK LINE
			!		BAV LINE
		!			INHIBIT/SOM (start of message)
	!				IRQ-ACTIVE

STATUS 3	2	
0	0	NORMAL STATE
0	1	INHIBIT STATE
1	0	ACTIVE IRQ
1	1	START OF MESSAGE

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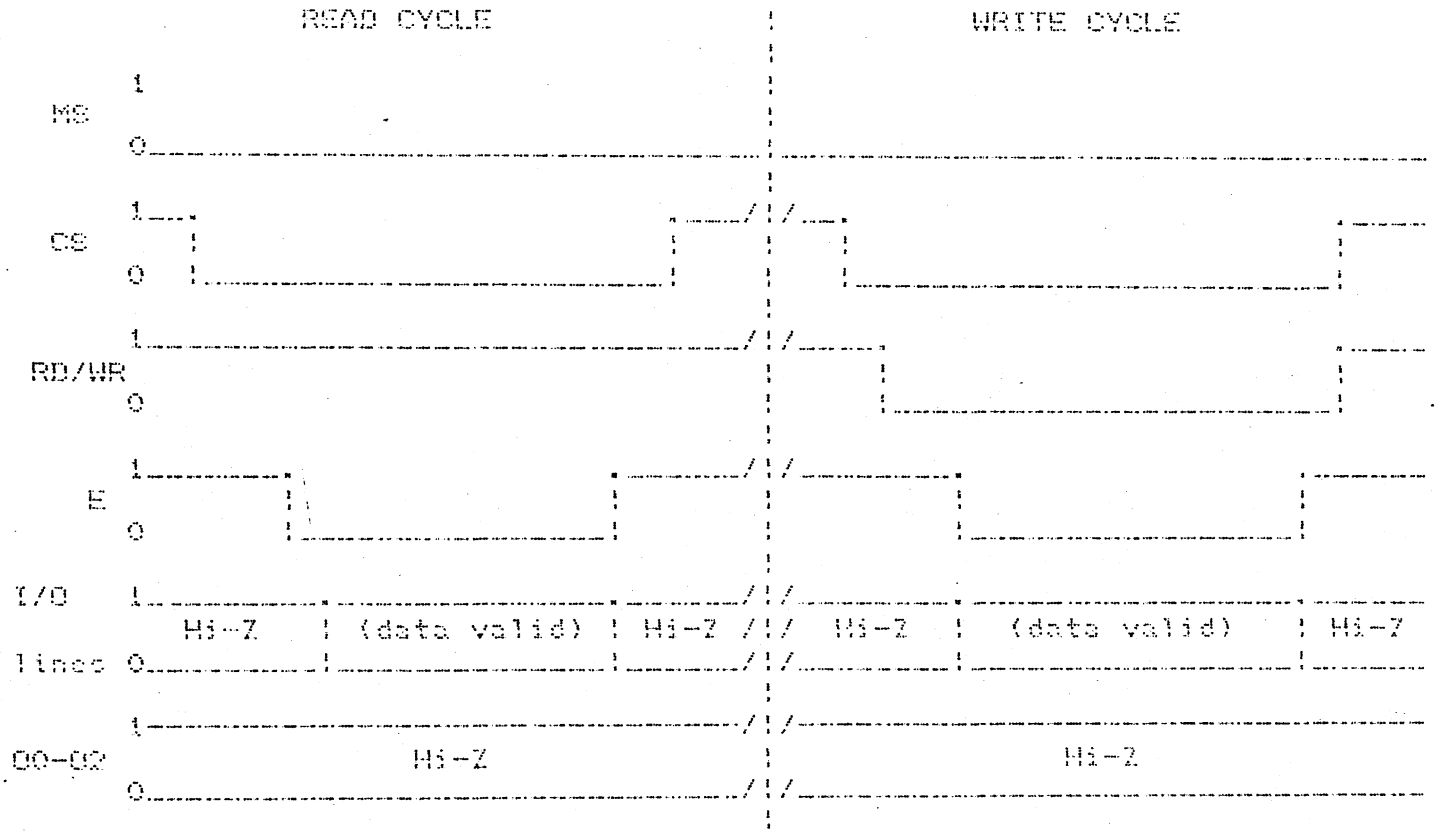
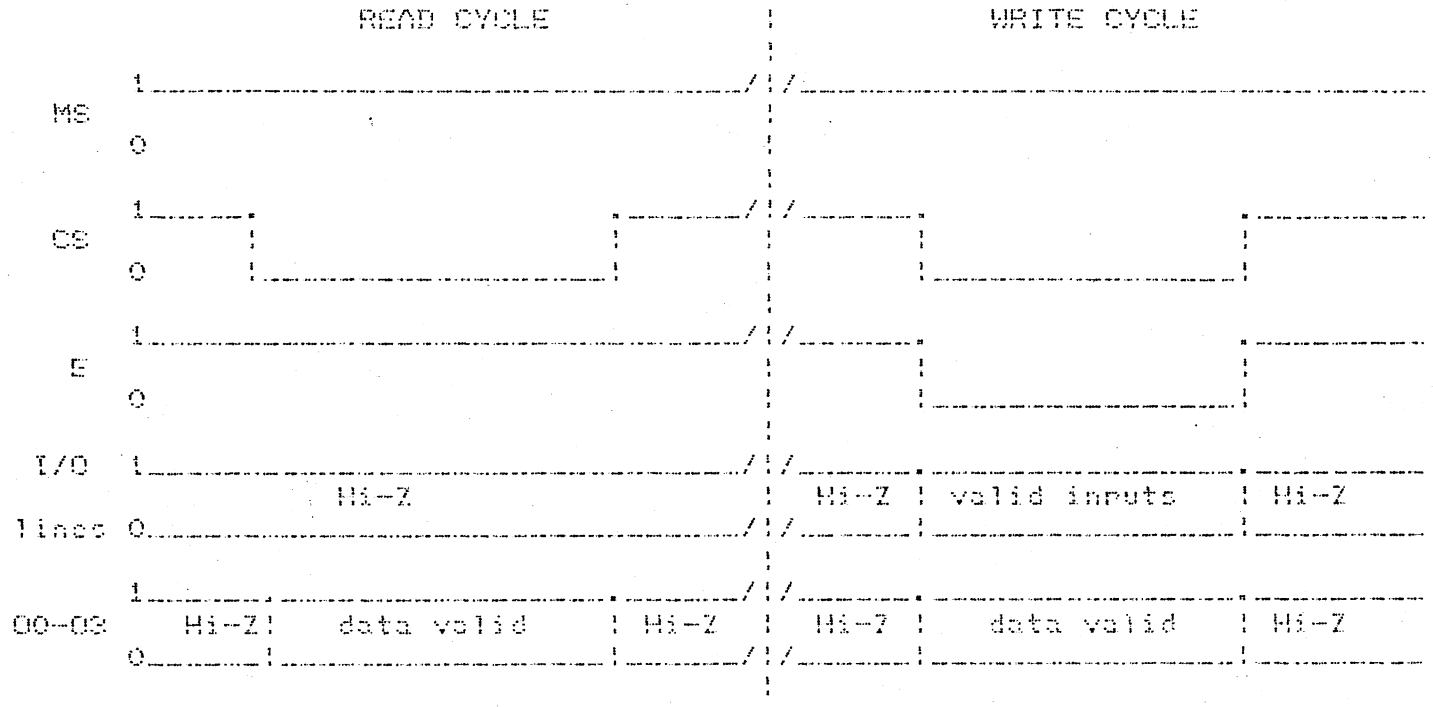
6. MPU INTERFACE TIMING - MODE 0



7. MPU INTERFACE TIMING - MODE-1



9. Electrical Characteristics

1. Technology - CMOS

2. Operating Temperature Range - 0 C - +70 C

3. Input/Output Characteristics - see Table 1 and 2

4. Timing Requirements - see Section 8

Table 1

Input-Output Characteristics for

I/O 0 - I/O 3, $\overline{CS}$, RS, E, R0/$\overline{WR}$-(O3), O 0 - O 2, $\overline{RES}$

	Vdd (Vdc)	MIN	MAX	UNIT
Vih (note 1)	5	2	5	V
	10	4	10	V
Vil (note 1)	5	0	.8	V
	10	0	3	V
Voh (note 2)	5	4.5	5	V
	10	9	10	V
Vol (note 2)	5	0	.05	V
	10	0	.1	V

Note 1 - not applicable for O 0 - O 3

Note 2 - not applicable for $\overline{CS}$, E, RS, MS and $\overline{RES}$ lines

Table 2

Input-Output Characteristics for

I/O 0 - I/O 3, $\overline{HSK}$, $\overline{DAV}$, $\overline{IRQ}$ (Open Drain Outputs)

	Vdd (Vdc)	MIN	MAX	UNIT
Vih (note 3)	5	2	10	V
	10	4	10	V
Vil (note 3)	5	0	.8	V
	10	0	1.5	V
Vol	5	0	.2	V
	10	0	.4	V
Iol (sink current)		4		mA

Note 3 - not applicable for $\overline{IRQ}$ line (output only)

Remarks:

At Vdd=5Vdc input lines I/O 0 - I/O 3, $\overline{CS}$, RS, MS, E, RD/$\overline{WR}$ and $\overline{RES}$ should be TTL compatible and output lines I/O 0 - I/O 3, D 0 - D 3 should be CMOS compatible.

9. Timing Requirements

Internal Gate Delay - 10 nsec (max @ Vdd-5 Vdc)

I/O Pair Delay - 30 nsec (max @ Vdd-5 Vdc)

Data Hold Time (note 4) - 10 nsec (max @ Vdd-5 Vdc)

Turn Off Time (3-state buffer) - 10 nsec (max @ Vdd-5 Vdc)

Note 4 - for latches indicated by letter Λ on logic diagram after active transition on CP line (from HIGH-to-LOW)

10. Logic Elements Description

1. Latches A - similar in function to SN74374 (data latched on transition from High-to-LOW on CP line, see Figure 2)

2. Gates B - have open drain outputs (Isink=4mA)

3. Gates C - have 3-state outputs (see Figure 1 below)

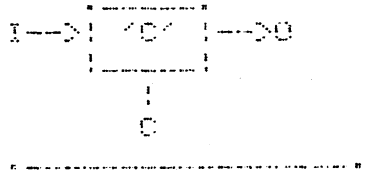
4. Gates D - have input characteristics as CD4050, but Vin(max)=12 Vdc

5. Flip-Flops E - see Figure 3 below

6. Flip-Flops F - see Figure 4 below

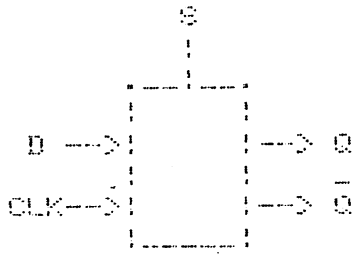
7. Flip-Flops G - see Figure 5 below

Figure 1 - Gates 'C'



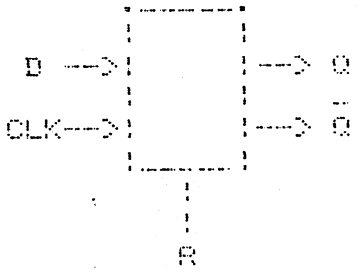
C	I	O
1	X	Hi-Z
0	0	0
0	1	1

Figure 2 - Flip-Flops 'A'



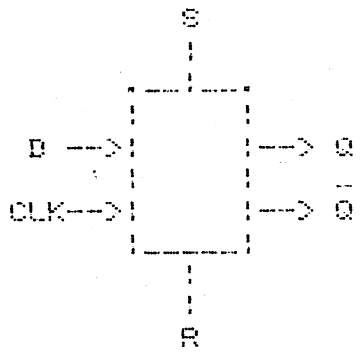
D	CLK	S	Q	$\overline{Q}$	
0	↓	0	0	1	
1	↓	0	1	0	
X	↑	0	Q	$\overline{Q}$	NO CHANGE
X	X	1	1	0	

Figure 8 - Flip-Flops 'B'



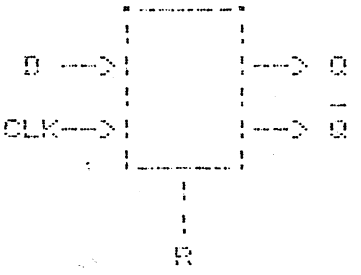
D	CLK	R	Q	$\overline{Q}$	
0	⎍	0	0	1	
1	⎍	0	1	0	
X	⎍	0	Q	$\overline{Q}$	NO CHANGE
X	X	1	0	1	

Figure 4 - Flip-Flops 'F'

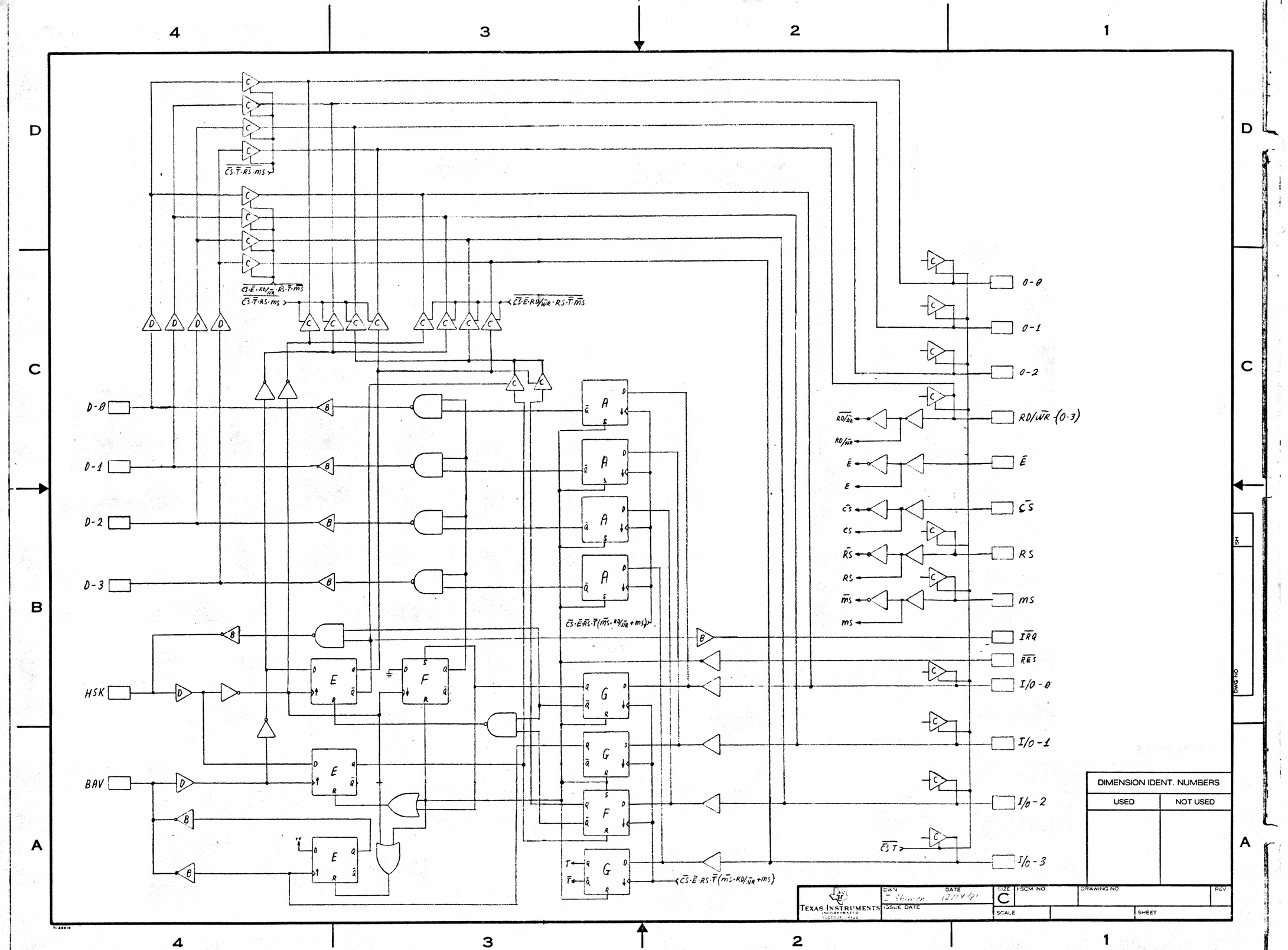


D	CLK	R	S	Q	$\overline{Q}$	
0	↓	0	0	0	1	
1	↓	0	0	1	0	
X	—	0	0	Q	$\overline{Q}$	NO CHANGE
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

Figure 5 - Flip-Flops 'G'



D	CLK	R	Q	$\overline{Q}$	
0	$\overline{\ }\backslash\_$	0	0	1	
1	$\overline{\ }\backslash\_$	0	1	0	
X	$\_/\overline{\ }$	0	Q	$\overline{Q}$	NO CHANGE
X	X	1	0	1	


4
3
2
1
D
C
B
A
D-0
D-1
D-2
D-3
HSK
BAV
$\overline{CS}\cdot\overline{T}\cdot\overline{RS}\cdot ms$
$\overline{CS}\cdot\overline{E}\cdot RD/\overline{WR}\cdot\overline{RS}\cdot\overline{T}\cdot\overline{ms}$
$\overline{CS}\cdot\overline{T}\cdot RS\cdot ms$
$\overline{CS}\cdot\overline{E}\cdot RD/\overline{WR}\cdot RS\cdot\overline{T}\cdot\overline{ms}$
$\overline{CS}\cdot\overline{E}\cdot\overline{RS}\cdot\overline{T}(\overline{ms}\cdot RD/\overline{WR}+ms)$
$\overline{CS}\cdot\overline{E}\cdot RS\cdot\overline{T}(\overline{ms}\cdot RD/\overline{WR}+ms)$
0-0
0-1
0-2
RD/WR (0-3)
$\overline{E}$
$\overline{CS}$
RS
ms
$\overline{IRQ}$
$\overline{RES}$
I/O-0
I/O-1
I/O-2
I/O-3
$\overline{CS}\,T$
DIMENSION IDENT. NUMBERS
USED
NOT USED
TEXAS INSTRUMENTS
INCORPORATED
DWN
DATE
ISSUE DATE
SIZE
C
FSCM NO
DRAWING NO
REV
SCALE
SHEET
SH
DWG NO