# Gate Array Timing Specifications

Consumer Products Group
Calculator Division

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Revision 0.5

# SECTION 1

## Electrical Characteristics

| Parameter | | min | nom | max | units |
|---|---|---|---|---|---|
| Tosc | XTAL2 cycle time | | 400 | | ns |
| Tc(H) | CLKOUT high (fast cycle) | | 400 | | ns |
| Tc(L) | CLKOUT low (fast cycle) | | 400 | | ns |
| Tc(H)' | CLKOUT high (slow cycle) | | 2800 | | ns |
| Tc(L)' | CLKOUT low (slow cycle) | | 2800 | | ns |
| Tc(C) | CLKOUT cycle time | | 800 | | ns |
| Tc(C)' | CLKOUT cycle time (slow) | | 5600 | | ns |
| Tca | CLKOUT rise to ALATCH rise | | 200 | | ns |
| Ta(A) | ALATCH active | | 260 | | ns |
| Tcy(R) | Read cycle time (fast) | | 1400 | | ns |
| Tcy(R)' | Read cycle time (slow) | | 6400 | | ns |
| Tcy(W) | Write cycle time | | 1380 | | ns |

| Parameter | | min | nom | max | units |
|---|---|---|---|---|---|
| Th(AR) | Low addr hold from ALATCH | | 200 | | ns |
| Th(AE) | High addr hold from ENABLE | | 140 | | ns |
| Tla | Low addr to low addr out | | 100 | | ns |
| Tz | Low addr high-Z to ENABLE | | 0 | | ns |
| Te(DI) | ENABLE active-data in (fast) | | 530 | | ns |
| Te(DI)' | ENABLE active-data in (slow) | | 4230 | | ns |
| Th(DA) | Data in hold to ENABLE(fast) | | 200 | | ns |
| Th(DA)' | Data in hold to ENABLE(slow) | | 1400 | | ns |
| Tea | ENABLE high to low addr lowZ | | 140 | | ns |
| Td(IN) | Data in from address (fast) | | 1230 | | ns |
| Td(IN)' | Data in from address (slow) | | 4830 | | ns |
| Ter | ENABLE inactive to RD/WR | | 200 | | ns |
| Tae | ALATCH fall to ENABLE active | | 270 | | ns |
| Ta(E) | ENABLE active (fast) | | 730 | | ns |
| Ta(E)' | ENABLE active (slow) | | 5530 | | ns |

| Parameter | | min | nom | max | units |
|---|---|---|---|---|---|
| Tacs | RAM select access time | | | 200 | ns |
| Toe | RAM OE to output valid | | | 120 | ns |
| Tclz | RAM select to out low Z | 15 | | | ns |
| Tolz | RAM OE to out low Z | 15 | | | ns |
| Te(DO) | ENABLE active to Dout | | 200 | | ns |
| Td(EI) | Dout to ENABLE inactive | | 530 | | ns |
| Tohz | Output disable to high Z | 0 | | 60 | ns |
| Tcw | RAM CS to end of write | 120 | | | ns |
| Tdw | RAM Data to write overlap | 60 | | | ns |
| Tdh | RAM Data hold from Write | 10 | | | ns |
| Twr | RAM write recovery time | 10 | | | ns |
| Taw | RAM addr valid to end of wr | 140 | | | ns |

| Parameter | | min | nom | max | units |
|---|---|---|---|---|---|
| Tas1 | ROM addr setup time | 500 | | | ns |
| Tas2 | LCD addr setup time | 900 | | | ns |
| Tce | ROM chip enable delay | | | 4000 | ns |
| Toff | ROM data off delay time | | | 1000 | ns |
| Tp | ROM chip enable precharge | 1000 | | | ns |
| Th | LCD hold time | 900 | | | ns |
| Tepw | LCD enable pulse width | 1800 | | | ns |
| Tddr | LCD data delay time | | | 900 | ns |
| Tdsw | LCD data setup time | 900 | | | ns |