ADD #2

SR-70 HARDWARE FUNCTIONAL SPECIFICATIONS

ADD memo

12
9940 Stat MB
141000 Proto BB
51
8A VV RS232
PWRSTAB TO TMS1000

PREPARED BY	DATE	TEXAS INSTRUMENTS INCORPORATED				
CHECKED BY	DATE	TITLE:				
ENGINEER	DATE					
APPROVED BY	DATE					
RELEASED BY	DATE	CODE IDENTITY NUMBER 01295	REVISION LETTER	A SIZE		SHEET 1

M E M O R A N D U M

22 May 1978

TO: Johnny Acker, Mike Anderson, David Brown, Mike Bunyard, Byron Crowe, Mike Fulghum, Bill Ham, Roy Smith, Roger Tilbury, Dick Houghton, Steve Indvik, Gary LaGrange, Jerry Maxwell, Jerry Ogarek, Stav Prodromou, Gary Slagel, Jerry Wardrum

COPY TO: Rex Naden, Deene Ogden, Ron Webb

FROM: Don Mills

SUBJECT: SR-70 HARDWARE FUNCTIONAL SPECIFICATION REVIEW

A review of the SR-70 Functional Specification was held in Lubbock on May 16, 1978. The specification was thoroughly overviewed, and was received without major comment. Two areas were indicated as requiring redefinition:

- The disk controller and drives must be redefined for the ADD drive. At present, the double density, single sided mini floppy controller and drive are specified.
- The power supply specification will be rewritten in light of the current power supply purchase part specification.

The enclosures detail all major and minor exceptions to the specification and the action items required to obtain closure on the specification signoff. An ACTION ITEM REPORT summarized needed activity.

Due to the extent of the updates required, due to the inclusion of the ADD controller specification, the formal signoff must be slipped to 6/30. All other updates will be required to be included by 5/30.

Donald V Mills

Don Mills

de
Attachment

DESIGN REVIEW

FUNCTIONAL DESCRIPTION

The "SR-70 Functional Specifications" is a hardware design specification and is not a concise functional description of the system. A user oriented functional description of approximately 10 pages is required which outlines the hardware and software features of the SR-70.

KEYBOARD - Section 3.7

- Exact operation of the repeat key must be added as paragraph 3.7.3.2.
- A technique for ease of service of the keyboard should be discovered and implemented and described.
- Inputs on key definitions from Jerry Wardrum are to be added to Table 3.7.2.5.
- The requirement for a keyboard lockout feature is to be added as paragraph 3.7.4. This feature inhibits the keyboard interrupt.
- The definition of n-key rollover for the SR-70 keyboard must be added to paragraph 3.7.2.4.
- The possibility of a color coded SYSTEM CLEAR key must be investigated to determine the impact on styling and human factors.
- The current plan of forcing the user to identify special function keys on a card which rests in front of the keyboard was identified as a potential problem area. Special "clear key" sets, color coded keys, or an overlay approach were suggested as alternatives.
- Paragraph 3.7.5 must be added to the specification which describes a general procedure for implementing non-US keyboards for the SR-70. Each keyboard will, in all probability, require a separate keyboard encoder to take care of the differing key positions found on non-US keyboards.

MONITOR - Section 3.13

- Discussion indicated the necessity of specifying the level of adjustment and repair which will be made on monitors in incoming inspection. DSG, Austin, will be consulted. This information is to be added to the monitor purchase part specification, A 1018487.
- Roger Tilbury agreed to investigate the tradeoffs associated with selling the SR-70 into European markets with the monitor packaged/sold separately versus the monitor packged/sold integrally with the mainframe.

MONITOR - Section 3.13 (cont.)

- Stav Prodromou suggested that Steve Indvik investigate the commonality between the DSG 770 monitor and the SR-70 monitor in an effort to determine if the same monitor can be utilized.

PRINTER - Section 3.8

- Marketing requirement for the printer rate is 2.5 lines per second. This requirement must be weighted against its impact on both the controller and the power supply.

- The description of the EPN3116S printhead must be added to Section 3.8 and the specification added as Appendix M.

- Print quality requirements are to be obtained from Gary LaGrange and added to paragraph 6.6 as a part of the printer test plan.

- C.B. Wilson suggested that a programmable character genertor be added to the printer controller. This will be investigated when the controller is designed and hardware impact determined.

MLB3 - Section 3.6.3

- The specification is to be expanded to include the number of screen updates/second.

- Discussion indicated that a DSR for the 733ASR terminal should be included in the DSR library.

MLB4 - Section 3.6.4

- The specification will be expanded to include a checksum feature to be added to each program in BROM (TMC 0350) as well as an overall checksum for each TMC0350 device. This will facilitiate error detection during system startup as well as during operation. Overall checksum will also be added to each ROM (TMS 4732).

TESTABILITY - Section 6.0

- Time required for final burn-in of the SR-70 system is to be added to paragraph 6.9.

- General test requirements for each subsystem within the SR-70 are to be added to the applicable sections within Section 6.0.

POWER SUPPLY - Section 3.10

- This specification is currently being revised by Mike Anderson and Jerry Ogarek. This section will be updated per this revision.

MLSB2 - Section 3.6.2

- The SR-70 will be featured with ADD instead of double density floppy disk drives. As a result, the disk drive must be rewritten to reflect the ADD controller.

- A meeting between the SR-70 design crew and the ADD personnel to identify and resolve system conflicts. These include environmental requirements, a motor speed lock control signal, and the power quality signal.

DISK DRIVES - Section 6.4

- Respecify in terms of the ADD drive. This section currently specifies the double density, single sided mini-floppy drive.

- Include in this section the specification of the ADD sector format.

CRU PORT - Paragraph 3.12.2

- A paragraph will be added to this section discussing the general characteristics of CRU based controllers which will be implemented on this port. This will serve as a general guideline for future development of external CRU controllers for the SR-70. A separate, detailed design guideline will be written by Mike Bunyard.

GENERAL MECHANICAL

- The environmental specification in Section 7.0 must be studied and enhanced. The stated specifications are currently in conflict with ADD and other subsystem environmental requirements. These conflicts must be resolved.

- Packaging and shipping requirements must be added to Section 7.0.

- It was indicated that the outboard (CRU, RS232C, monitor) connector schemes should be restudied in light of cable capturing techniques. The identified solutions must encompass provisions for the following:

  - Stress relief on connectors at the PCB's and case.

  - Cable restraints which allow forcible removal of the mating connector without damage to the PCB, case, or connector.

- Steve Indvik identified that MCB3 has a potential heat dissipation problem due to connector blockage of airflow out of the rear of the case. This must be identified in terms of the SR-70 airflow model to access the magnitude of the problem.

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ACTION ITEM REPORT

STAMP CLASSIFICATION AS REQUIRED

PROGRAM	PROGRAM MANAGER	STATUS DATE
SR-70 FUNCTIONAL SPECIFICATION	DONALD MILLS	5/18/78

PROBLEM	ACTION	ASSIGNMENT	COMPLETION TARGET
AN SR-70 FUNCTIONAL DESCRIPTION IS REQUIRED.	AUTHOR THE SPECIFICATION	BUNYARD	6/30
KEYBOARD SPECIFICATION DEFICIENCIES	DEFINE THE REPEAT KEY OPERATION	BUNYARD	5/30
	STUDY THE SERVICEABILITY REQUIREMENTS	FULGHUM	5/26
	DEFINE THE SMALL BUSINESS SYSTEM SPECIAL KEYS	WARDRUM	5/26
	DEFINE KEYBOARD LOCKOUT	BUNYARD	5/30
	COLOR CODED SYSTEM CLEAR KEY IMPACT	BROWN	5/26
	INVESTIGATE ALTERNATIVES TO THE CURRENTLY DEFINED SPECIAL FUNCTION CARD	BROWN	6/30
	DEFINE THE IMPLEMENTATION SCHEME FOR NON-US KEYBOARDS	BUNYARD	5/30
MONITOR SPECIFICATION DEFICIENCIES	SPECIFY INCOMING INSPECTION REPAIR/ADJUSTMENT IN PURCHASE SPEC	INDVIK/ INCOMING	6/30
	TRADE OFF STUDY ON SEPARATELY PACKAGED MONITOR/ MAINFRAME IN EUROPE	TILBURY	8/30
	INVESTIGATE 770/SR-70 MONITOR COMPATIBILITY	INDVIK	5/30
PRINTER DESCRIPTION DEFICIENCIES	INVESTIGATE H/W IMPACT OF 2.5 LINE/SEC PRINTER	OGAREK/ ANDERSON/ BUNYARD	5/30
	ADD EPN3116S DESCRIPTION TO SPEC.	BUNYARD	5/30
	ADD PRINT QUALITY REQUIREMENTS	BUNYARD/ LAGRANGE	5/30
	INVESTIGATE PROGRAMMABLE CHARACTER GENERATOR FOR PRINTER	BUNYARD	6/30

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ACTION ITEM REPORT

STAMP CLASSIFICATION AS REQUIRED

PROGRAM	PROGRAM MANAGER	STATUS DATE
SR-70 FUNCTIONAL SPECIFICATION	DONALD MILLS	5/18/78

PROBLEM	ACTION	ASSIGNMENT	COMPLETION TARGET
MLB3 DESCRIPTION DEFICIENCIES	SPECIFY SCREEN UPDATES/SEC	BUNYARD	5/30
	INCLUDE 733ASR DSR IN S/W	ACKER	3Q78
MLB4 DESCRIPTION DEFICIENCIES	ADD CHECKSUM FEATURE TO SPECIFICATION FOR ROM (TMS 4732), BROM(TMC 0350)	BUNYARD/ ACKER/ WARDRUM	5/30
TESTABILITY DESCRIPTION DEFICIENCIES	ADD SYSTEM BURN-IN TIME TO SPEC. INCLUDE GENERAL TEST REQUIREMENTS FOR EACH SUBSYSTEM. (THIS WILL BE ECN'ED TO SPEC AS EACH SUBSYSTEM REQUIREMENT IS DETERMINED)	BUNYARD STAFF	5/30 8/30
POWER SUPPLY SPECIFICATION DEFICIENCIES	UPDATE SPEC	ANDERSON/ OGAREK	5/30
MLB2 SPECIFICATION DEFICIENCIES	ELIMINATE THE FLOPPY DISK DRIVE CONTROLLER DESCRIPTION AND REPLACE THE DESCRIPTION WITH THE ADD CONTROLLER DESCRIPTION	BUNYARD/ FULGHUM	6/30
DISK DRIVE SPECIFICATION DEFICIENCIES	REPLACE THE FLOPPY DRIVE SPECIFICATION WITH THE ADD DRIVE SPECIFICATION	BUNYARD	5/30
CRU PORT SPECIFICATION DEFICIENCIES	ADD GUIDELINE FOR EXTERNAL CRU MODULE DESIGN TO SPEC	BUNYARD	5/30

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ACTION ITEM REPORT

STAMP CLASSIFICATION AS REQUIRED

PROGRAM	PROGRAM MANAGER	STATUS DATE
SR-70 FUNCTIONAL SPECIFICATION	DONALD MILLS	5/18/78

PROBLEM	ACTION	ASSIGNMENT	COMPLETION TARGET
GENERAL MECHANICAL SPECIFICATION DEFICIENCIES	ENHANCE ENVIRONMENTAL SPEC	LAGRANGE	5/30
	ADD PACKAGING/SHIPPING REQUIREMENTS	LAGRANGE	5/30
	STUDY OUTBOARD CONNECTOR SCHEME IN TERMS OF STRESS RELIEF AND CONNECTOR CAPTURE	BROWN	6/30
	REVIEW MLB3 HEAT DISSIPATION	BROWN	6/30

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1.0 Introduction

The SR-70 is a small business oriented machine that has the following characteristics:

- A TMS 9900 Microprocessor based system
- 32K bytes of Dynamic RAM
- 32K bytes of ROM
- Dual, single-sided, MFM floppy disk drives
- 12" video monitor
- Solid State Software library in TMC 0350 BROM's (512K bytes)
- RS-232-C outside world interface
- 2K line CRU outside world interface
- IEEE 488 bus interface option
- 48 column printer
- QUERTY keyboard

2.0 Applicable Documents

- Commercial Personal Computer Total Marketing Plan (SR-70) TI Strictly Private
- Equipment Group TTL Designers Guide, Dwg 932142
- CALD # 1031293, # 1030226 for motor drive characteristics
- CALD # 101824-1 Keyboard Mechanical Definition
- CALD # 1500506-4 Thermal Paper
- CALD # 1018454 Printhead Specifications

2.1 Symbol Definition

Signal names followed by an asterix denote a Low true signal (MEMEN*).

Since some system functions may span several clock cycles, the number of the clock cycles shall be appended to the end of the clock phase number. PH3*(2) denotes the second PH3* clock in the time period of interest. The CPU MEMEN* signal will have a PH1(1) and a PH1(2) associated with it.

Standard LE and TE denote the Leading Edge and Training edge respectively of a function.

2.1 Symbol Definition (Continued)

All CRU and memory addresses are assumed to be hexadecimal unless otherwise designated.

A period (.) in a logical expression denotes the AND function and the plus (+) denotes the OR function.

3.0 Hardware Description

All logic design shall be done according to practices outlined in the Equipment Group # 932142 TTL Logic Designers Guide to provide a stable system. This design must also be cost effective with built in learning, producible in volume, reliable, and maintainable if the SR-70 is to be a successful product.

3.1 SR-70 System Memory Map

The System Memory Map is shown in FIG. 3.1, and is composed of three basic spaces. There are 32K bytes of DRAM, 8K bytes of paged space, and 24K bytes of ROM space.

The paged space is the "garbage can space" in that all memory mapped internal IO resides in this space along with any Primary ROM over 24K. This 8K byte paged space is shared between 8K bytes of ROM and two memory mapped peripherals. A pair of CRU bits are utilized as page control bits to select one desired function out of four in the 8K byte paged space.

The Floppy Disk Controller chip is accessed at a memory base of 9000 after its CRU page has been selected (060C=1 and 060E=0).

The SMC CRT5027 chip is accessed at a memory base of 8800, and the 2K byte video character buffer at 8000 after its CRU page has been selected (060C=1, 060E=1).

The 8K byte paged ROM between 8000 and 9FFF is accessed when the ROM page is selected (060C=0, 060E=0).

Any other future functions may be easily added to this space in a simi lar method utilizing existing spare (Not Assigned) CRU output bits. Static RAM's, test ROM's, etc. fall into this category.

The Primary ROM page is selected by either the Power On Clear or Software Reset.

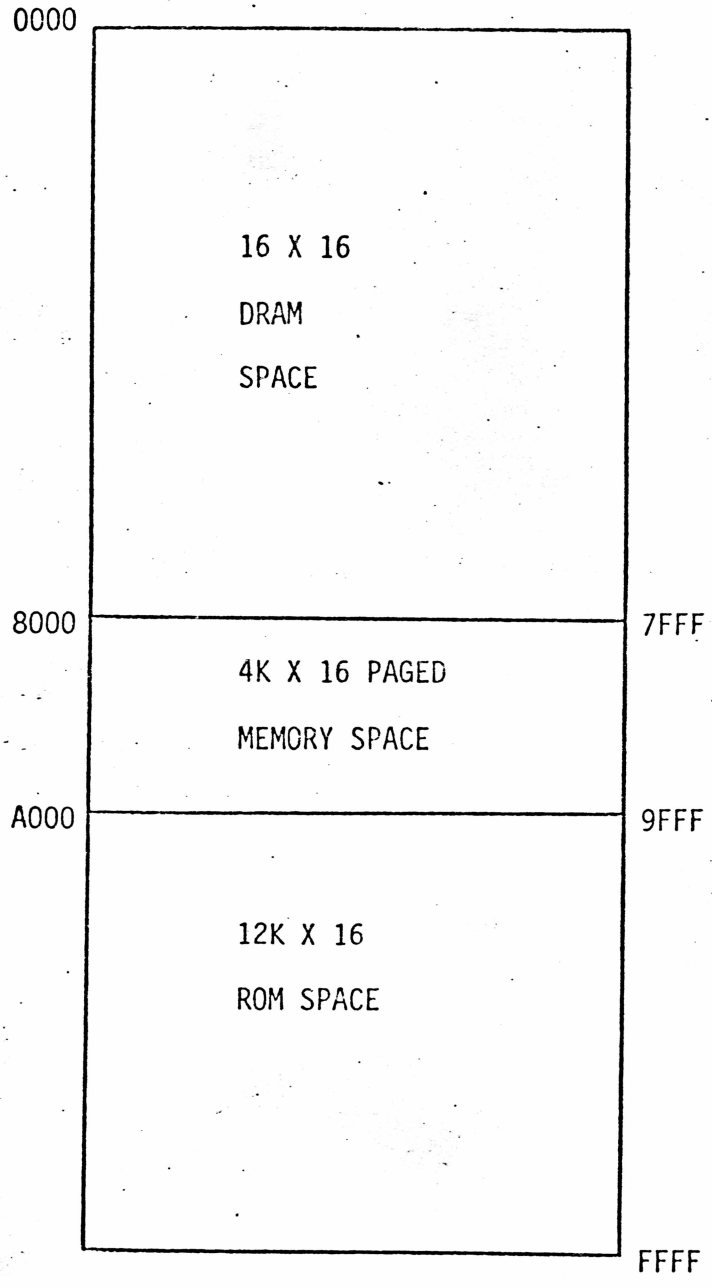


FIGURE 3.1 SR-70 MEMORY SEGMENTATION

3.1.1 Detailed SR-70 Memory Map

ADDRESS	RANGE		FUNCTION ADDRESSED	
0000	7FFF		DRAM - 32K Bytes	R/W
8000	9FFF		ROM (MLB4) ROM page bit @ 602 must be high	R
8000	87FF		TV Buffer - 2K Bytes TV PAGE bit @ 060E must be set high	R/W
8800	8FFF		TV Controller Chip	
8800	880C		TV Chip setup/control data See Appendix J for SMC CRT 5027 definition	W
	8818	MSBY	Cursor row position (set)	W
	881A	MSBY	Cursor column position (set)	W
	881C	MSBY	Cursor row position (sense)	R
	881E	MSBY	Cursor column position (sense) TV PAGE is selected when the bits @ 060C and 060E are High	R
9000	9FFF	MSBY	Floppy Disk Controller Chip	
	9008	MSBY	Status Register	R
	9000	MSBY	Command Register	W
	9002	MSBY	Track Register (R=900A)	W
	9004	MSBY	Sector Register (R=900C)	W
	9006	MSBY	Data Register (R=900E) Disk PAGE is selected for CRU bits 060C=1 and 060E=0	W
A000	FFFE		ROM (MLB4A,B)	R

3.2 SR-70 System CRU Map

The SR-70 Communications Register Unit (CRU) space is divided in half with the lower 2K bit serving the SR-70 internal functions. This 2K space is in turn decoded into 256 bit spaces, and these blocks serve the various functions with no further upper address decode (multiple addresses for the same function within the 256 bit block). The TMS 9902 RS-232-C controller space is an exception to this type of decode.

The upper 2K bits form the basis for the CRU Port for Outside World use. The user who implements his own logic on this port determines bit definitions.

3.2.1 Detailed SR-70 CRU Map

All CRU Address spaces (but the one at 0000) utilized for internal machine control have an address span of 1FE, and functions are not uniquely decoded in this span (multiple addressing for the same function is possible). An example of this for a CRU base of 0E00 is that the DMAC enable bit found at 0E40. Address shown in this map shall be used exclusively to provide for future expansion.

Base Address	Displacement							
0000	TMS 9902 ACC Input Bit Address Assignments							
	$ADDRESS_2$					$ADDRESS_{10}$	NAME	DESCRIPTION
	0	1	2	3	4			
	1	1	1	1	1	31	INT	Interrupt
	1	1	1	1	0	30	FLAG	Register Load Control Flag Set
	1	1	1	0	1	29	DSCH	Data Set Status Change
	1	1	1	0	0	28	CTS	Clear To Send
	1	1	0	1	1	27	DSR	Data Set Ready
	1	1	0	1	0	26	RTS	Request To Send
	1	1	0	0	1	25	TIMELP	Timer Elapsed
	1	1	0	0	0	24	TIMERR	Timer Error
TMS 9902	1	0	1	1	1	23	XSRE	Transmit Shift Register Empty
(MLB3)	1	0	1	1	0	22	XBRE	Transmit Buffer Register Empty
	1	0	1	0	1	21	RBRL	Receive Buffer Register Loaded
	1	0	1	0	0	20	DSCINT	Data Set Status Change Interr.
	1	0	0	1	1	19	TIMINT	Timer Interrupt
	1	0	0	1	0	18	-	Not used (always = 0)
	1	0	0	0	1	17	XBINT	Transmitter Interrupt
	1	0	0	0	0	16	RBINT	Receiver Interrupt
	0	1	1	1	1	15	RIN	Receiver Input
	0	1	1	1	0	14	RSBD	Receiver Start Bit Detect
	0	1	1	0	1	13	RFBD	Receive Full Bit Detect
	0	1	1	0	0	12	RFER	Receive Framing Error
	0	1	0	1	1	11	ROVER	Receive Overrun Error
	0	1	0	1	0	10	RPER	Receive Parity Error
	0	1	0	0	1	9	RCVERR	Receive Error
	0	1	0	0	0	8	-	Not used (always = 0)
						7-0	RBR7-RBR0	Receive Buffer Register

Base Address	Displacement	Function
0000		TMS 9902 ACC Output Bit Address Assignments

$ADDRESS_2$ 0 1 2 3 4	$ADDRESS_{10}$	NAME	DESCRIPTION
1 1 1 1 1	31	RESET	Reset device
	30-22	-	Not used
1 0 1 0 1	21	DSCENB	Data Set Status Change Interrupt Enable
1 0 1 0 0	20	TIMENB	Timer Interrupt Enable
1 0 0 1 1	19	XBIENB	Transmitter Interrupt Enable
1 0 0 1 0	18	RIENB	Receiver Interrupt Enable
1 0 0 0 1	17	BRKON	Break On
1 0 0 0 0	16	RTSON	Request To Send On
0 1 1 1 1	15	TSTMD	Test Mode
0 1 1 1 0	14	LDCTRL	Load Control Register
0 1 1 0 1	13	LDIR	Load Interval Register
0 1 1 0 0	12	LRDR	Load Receiver Data Rate Regis.
0 1 0 1 1	11	LXDR	Load Transmit Data Rate Regis.
	10-0		Control, Interval, Receive Data Rate, Transmit Data Rate, & Transmit Buffer Registers

	Displacement	Miscellaneous CRU Input Bit Assignment	Test Only
0040	0	External Printer (on RS-232-C port) BUSY	1 = BUSY, 0 = Ready
	1	Not Assigned	
	2	Not Assigned	
	3	Not Assigned	
	4	Test Loop sense - connect to out bit at 0606	
	5	Not Assigned	
	6	Not Assigned	
	7	Not Assigned	

3.2.1 Detailed SR-70 CRU Map (Continued)

Base Address	Displacement		Function	
0200	0		Control bit (CR)	R/W
	1	CR=0	INT1*- Power Going Down	R
	1	"	INT1 - Mask	W
	2	"	INT2*- Keyboard	R
	2	"	INT2 - Mask	W
	3	"	INT3*- Interval Timer	R
	3	"	INT3 - Mask	W
	4	"	INT4*- Not Assigned	R
TMS 9901	4	"	INT4 - Mask	W
(MLB1)	5	"	INT5*- Disk	R
	5	"	INT5 - Mask	W
	6	"	INT6*- CRU Port I1	R
	6	"	INT6 - Mask	W
	7	"	INT7*- UART 9902	R
	7	"	INT7 - Mask	W
	8	"	INT8*- Print Complete	R
	8	"	INT8 - Mask	W
	9	"	INT9*- Not Assigned	R
	9	"	INT9 - Mask	W
	A	"	INT10*- CRU Port I2	R
	A	"	INT10 - Mask	W
	B	"	INT11*- CRU Port I3	R
	B	"	INT11 - Mask	W
	C	"	INT12*- CRU Port I4	R
	C	"	INT12 - Mask	W
	D	"	INT13*- CRU Port I5	R
	D	"	INT13 - Mask	W
	E	"	Assigned to KBD Data	-
	F	"	Assigned to KBD Data	-
	10	CR=Don't Care	KBD Receive Data, LSB	R
	11	"	KBD Data	R
	12	"	KBD Data	R
	13	"	KBD Data	R
	14	"	KBD Data	R
	15	"	KBD Data	R
	16	"	KBD Data	R
	17	"	KBD Data MSB	R
	18	"	KBS Interrupt Reset Bit (KBIRST*) low to Reset KBD Interrupt - to enable KBD Interrupt...(source at KBD is disabled when this bit is low)	W

TMS 9901 Programmable Real Time CLock

The clock consists of a 14 bit counter that decrements at a rate that results in a maximum interval of 349 ms with a resolution of 21.3 us, and can be used as either an interval timer or as an event timer.

The clock is accessed by writing a one into the control bit to force CRU bits 1-15 to clock mode. Writing a nonzero value into the clock register then enables the clock and sets its frequency. The clock functions as an interval timer by decrementing to zero, issuing an interrupt, and

TMS 9901 Programmable Real Time Clock (Con't)

restarting at the programmed start value. When the clock interrupt is active, the clock mask (mask bit 3) must be written into (with either a "1" or a "0") to clear the interrupt.

If a value other than that initially programmed is required, a new 14-bit clock start value is similarly programmed by executing a CRU write operation to the same locations. During programming the decrementer is restarted with the current start value after each start value bit is written. A timer restart can be easily implemented by writing a single bit to any of the clock bits.

The clock is disabled by a system reset by writing a zero value into the clock register. Enabling the clock programs the third priority interrupt (INT3*) as the clock interrupt and disables generation of interrupts from the INT3* input pin. When accessing the clock all interrupts should be disabled to ensure that system integrity is maintained.

The clock can also function as an event timer since whenever the device is switched to the clock mode, by writing a one to the control bit, the current value of the clock is stored in the clock read register. Reading this value, and thus the esapsed event time, is accomplished by executing a 14 bit CRU read operation (addresses 1-14 displaced from 0200).

The current status of the machine can always be obtained by reading the control (address zero) bit. A "0" inidicates the machine is in a interrupt mode. A "1" read on the control bit indicates that the TMS 9901 is in the clock mode.

A software reset RST2* can be performed by writing a "1" to the control bit followed by writing a "1" to bit 15 (displaced from 0200), which forces all I/O ports to the input mode.

Base Address	Displacement	Function	
0400		To be used for future ADDs control	
0600			
	0	Not Assigned	W
	1	Not Assigned	W
	2	Not Assigned	W

Base Address	Displacement	Function	
0600	3	CRU Test Loop CRU OUT bit 3 is conected to CUR IN bit 4 @ 0048 to provide a test path	W
	4	Beeper (an audible device for signaling the operator, and requires a one to be on and a zero to be off. A 50% duty cycle on a 1 sec period is required)	W
	5	Print Request (ON, OFF Protocol)	W
	6,7	Page select bits. bit 6=0, bit 7=0 is primary ROM page, bit 6=0, bit 7=1 is not assigned page, bit 6=1, bit 7=0 is Disk page, and bit 6=1, bit 7=1 is the TV page.	
	NOTE:	ALL 0600 BITS ARE SET TO ZERO, by Power On Clear or Software Reset	
0800	0	Address Nibble bit #1 LSB	W
	0	BROM data Byte bit #1 LSB	R
	1	Address Nibble bit #2	W
	1	BROM Data Byte bit # 2	R
	2	Address Nibble bit # 3	W
	2	BROM Data Byte bit # 3	R
	3	Address Nibble bit # 4 MSB	W
	3	BROM Data Byte bit # 4	R
	4	BROM IO Control Line	W
	4	BROM Data Byte bit # 5	R
	5	BROM I1 Control Line	W
	5	BROM Data Byte bit #6	R
	6	BROM Group Select LSB	W
	6	BROM Data Byte bit #7	R
	7	BROM Group Select MSB	W
	7	BROM Data Byte bit # 8 MSB See table 3.6.5.4B for I1, IO functional definition.	R
0A00		Not Assigned	
0C00		Not Assigned	
0E00	0	Enables DMAC, Data Manager logic, "0" holds logic "RESET"; "1" enables logic to function	W
	1	DMAC data direction control "1" is transfer from Disk to system DRAM	W
	2	TMS 9940 Printer Reset 0=Reset, 1=Run	W
	3	Not Assigned	W
	4	DISK 0/1 select: 0=Disk 0, 1=Disk 1	W
	5	Not Assigned	W

	selected, 0= Page not selected	
6	FDC chip reset bit, "0" is RESET, "1" is RUN	W
7	Software System RESET, "1" is RESET - When set to a "1", there will be no other instruction before a hardware "LOAD" will be performed. and all hardward will be reset. (See note at the end of the 0E00 space definition)	W
8	Motor ON, 1=ON, 0=OFF	W
9	For future use as head side select	W

NOTE 1: Bit 4 (Disk 0/1 select) controls which disk drive motor latch is activated. If bit 4=0 the motor latch for Drive 0 may be either set to a one or a zero, and that for Drive 1 is not effected. Changing bit 4 shall not effect either motor control latch.

CPU to TMS 9940 (Printer) data transfer (16 bits only) is based at 0E20. Data is transferred from directly the system CRU Bus into the internal TMS 9940 MPSI CRU Register.

NOTE: ALL 0E00 BITS SHALL BE SET TO ZERO, by either a Power On Clear or a Software Reset.

Base Address	Displacement	Function
1000 to 1FFF		CRU Port User Function defined

3.3 Interrupt Definition

Thirteen of the sixteen possible TMS9900 interrupt levels have been implemented thru the TMS 9901 with eight levels being devoted to internal machine control(2 are spares). The other five levels are are being driven by the CRU port, and it will be up to the user to unmask as well as service these levels.

Interrupt level 0 is not used as a TMS 9901 controls the interrupt logic, and there is no provision in the TMS 9901 to implement INTO*.

Hardware will drive the TMS 9900 "Reset" pin during both Power On Clear and Software Reset execution, and the CPU will obtain the Level 0 Workspace Pointer and Program Counter. It will also store the present Workspace Pointer, Program Counter, and Status with respect to the Level 0 Workspace Pointer, but it will execute no Level 0 PC code because the CPU "Load" pin is also driven Low as a function of the System Reset. See Figure 3.4.2.

Table 3.3 depicts the detailed interrupt definition. Individual DSR specifications detail the Interrupt sequence control.

TABLE
3.3 INTERRUPT LEVEL DEFINITION, TMS 9901 CONTROLLED

Level	Function
0	Reset Only (not Hardware executable)
1	Power going down from Power Supply See Figure 3.10.20 for timing.
2	Keyboard "New Character", see Section 3.6.1.2 for interrupt control, and Section 3.7 for KBD specs
3	9901 Interval Timer
4	Not Assigned
5	Disk, see Sections 3.6.2.3 and 3.9 for control description
6	External CRU Level 1, user defined and programmed
7	TMS 9902 UART, see Section 3.2.1 for detailed operation
8	Print complete from printer, see Section 3.8 for this TMS 9940 originated interrupt
9	Not Assigned
10	External CRU Level 2, user defined and programmed
11	External CRU Level 3, user defined and programmed
12	External CRU Level 4, user defined and programmed
13	External CRU Level 5, user defined and programmed
	Not Assigned

3.4.1 System Clock

The system clock is generated by a TIM9904/SN74LS362N clock generator operating with a 48 MHz crystal and tank to provide a 3MHz 4 phase clock. A 12 MHz single phase tap (TTL output) in the counter chain is provided for disk use. The 4 phase TTL clock outputs are provided on the System Bus backplane (see Section 3.6.5.1) for system timing & con-

3.4.2 Power-up/Reset Sequence

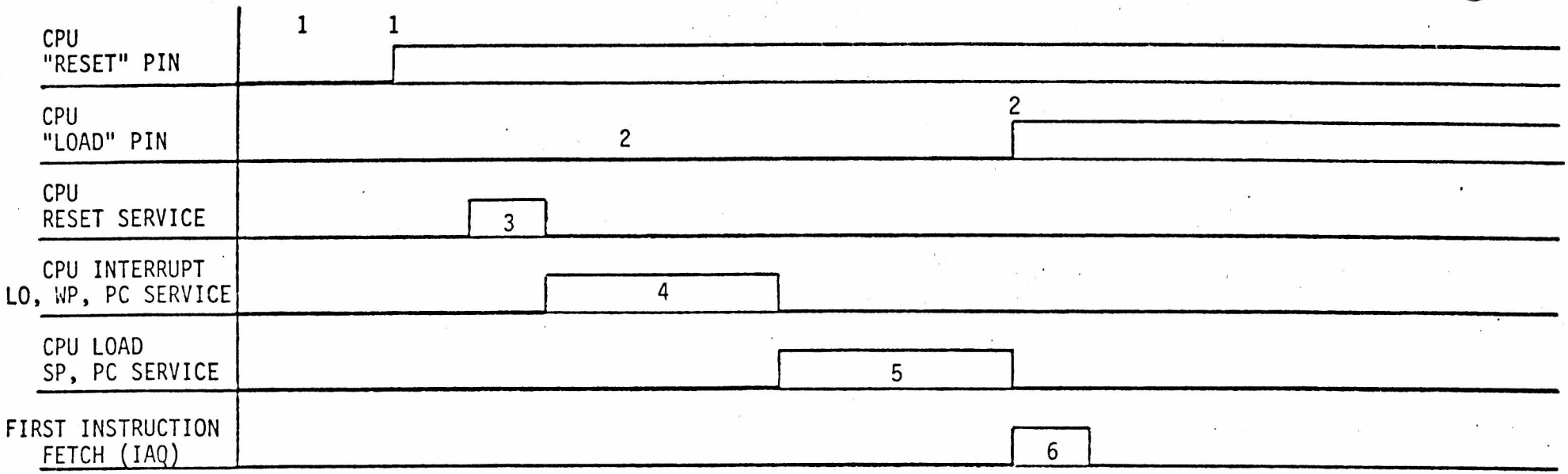
The TMS9900 will come up in the "LOAD" mode (see Fig. 3.4.2) from either a Power On Clear condition from the power supply, or a Software Reset (same hardware effects as the Power on condition). All maskable Interrupt Levels will be masked, the DMAC, Data Manager, Printer, and Floppy Disk Controller will be held RESET until software enabled, and all page bits will be RESET. All MOS CRU bits will be set to the input mode (will float high) and all TTL CRU Output bits will be set to zero.

3.5 System Block Diagram

The system block diagram is shown in Fig. 3.5, and has been broken down into mainframe and peripheral areas. The majority of the logic is contained on four main logic boards - MLB1, MLB2, MLB3, and MLB4. MLB1 is the heart of the system, and has the 4 phase clock, the TMS9900, the TMS9901, the DRAM memory controller, the 32K byte DRAM, and misc buffer logic. It also interfaces to the keyboard.

MLB2 has both the thermal printer and disk control logic. MLB3 contains the outside world interface logic for the video monitor, the RS-232-C port, and the CRU port. MLB4 is a ROM board, and contains direct access ROM on the system bus (primary memory) as well as the sequentially accessed BROM (secondary memory) which indirectly connects to the CRU bus.

The keyboard, the TMS9940 based thermal printer control, the disk drives, and the power supply are separate subassemblies not integral with the mainframe. Cable assemblies link these peripheral blocks with the mainframe.



NOTES

1 CPU "RESET*" PIN, GOES HIGH OBEYING PHI REQUIREMENTS

2 CPU "LOAD*" PIN, GOES HIGH ON FIRST INSTRUCTION EXECUTED

3 CPU PARTIAL EXECUTION OF THE RESET SEQUENCE

4 CPU SERVICE OF LEVEL 0 WP AND PC

5 CPU SERVICE OF LOAD WP AND PC

6 FIRST INSTRUCTION FETCH FROM RESET SEQUENCE START

FIGURE 3.4.2 BASIC CPU LOAD-ON-RESET TIMING

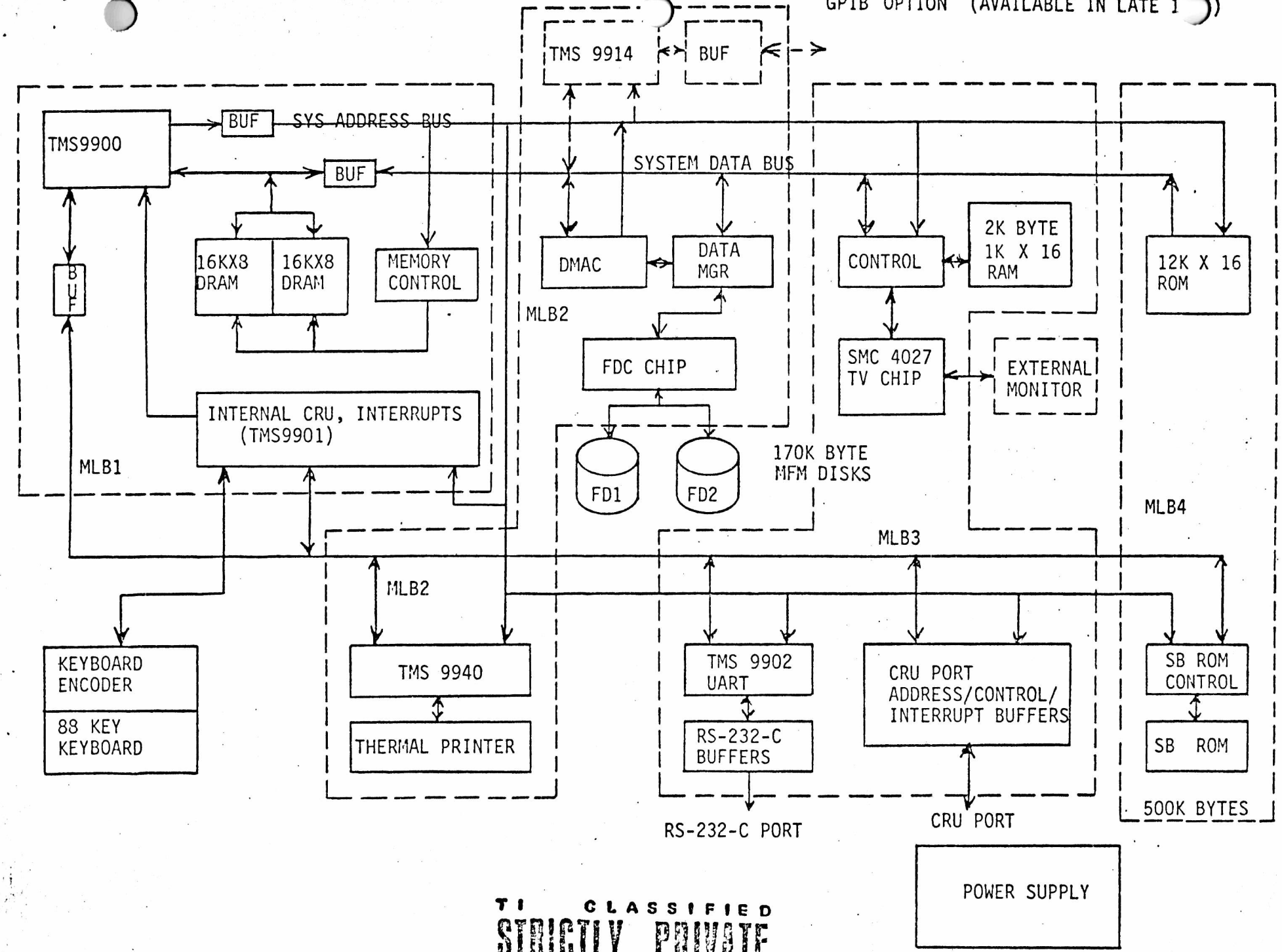


FIGURE 3.5 SYSTEM BLOCK DIAGRAM

3.6 Mainframe

The mainframe consists of four PCBs each of which contains a discrete logic function necessary to accomplish SR-70 system level requirements. With the exception of the signal CRUIN to the TMS 9900, only TTL signals appear at the system level on the mainframe. CRUIN is adequately guarded on the System Data Bus. See Appendix D.

3.6.1 MLB1

MLB1 is the heart of the SR-70 mainframe in that it contains the TMS9900, the 32K byte DRAM, the system clock, signal buffers, the TMS9901 IO device, and miscellaneous timing and control. MLB1 shall be adequately bypassed to insure stable operation. See Section 3.0.

3.6.1.1 MLB1 Basic Block Diagram

Figure 3.6.1 depicts the functional characteristics of MLB1.

3.6.1.2 MLB1 Functional Characteristics

For specification Figure 3.6.1 may be broken up into some six basic areas. The first of which is the TMS9900 microprocessor. Only the TMS 9900 five interrupt inputs, four clock phases, and the IAQ output do not become system level signals. All system level output and bidirectional signals are buffered before leaving MLB1 in order to present low impedance drivers to the system bus.

The second area is the TIM9904/SN74LS362 clock chip which utilizes a 48 MHz crystal necessary to obtain a 3 MHz 4 phase clock for system use. A 12 MHz non-symmetrical single phase clock is also derived for system use.

Sixteen TMS4116 16K X 1 DRAMS which operate in the "Early Write" mode comprise the third area. "Early Write" is implemented by stabilizing the W* input prior to allowing CAS* to go low; thus, the data input (D) and the data output (Q) pins may be tied together with no data bus conflict. Figure 3.6.1.2 shows the DRAM timing. They are connected to the CPU data bus to keep MOS drivers off of the system data bus.

The fourth area is the memory controller. To perform its function it needs inputs from the CPU control logic, the DMAC logic, and the refresh logic. Both the CPU and DMAC request memory cycles on a PH2LE/PH2/PH2LE basis, and to provide for Refresh cycles logic must be included to inhibit the DMAC request or put the CPU in a wait state during the refresh time periods.

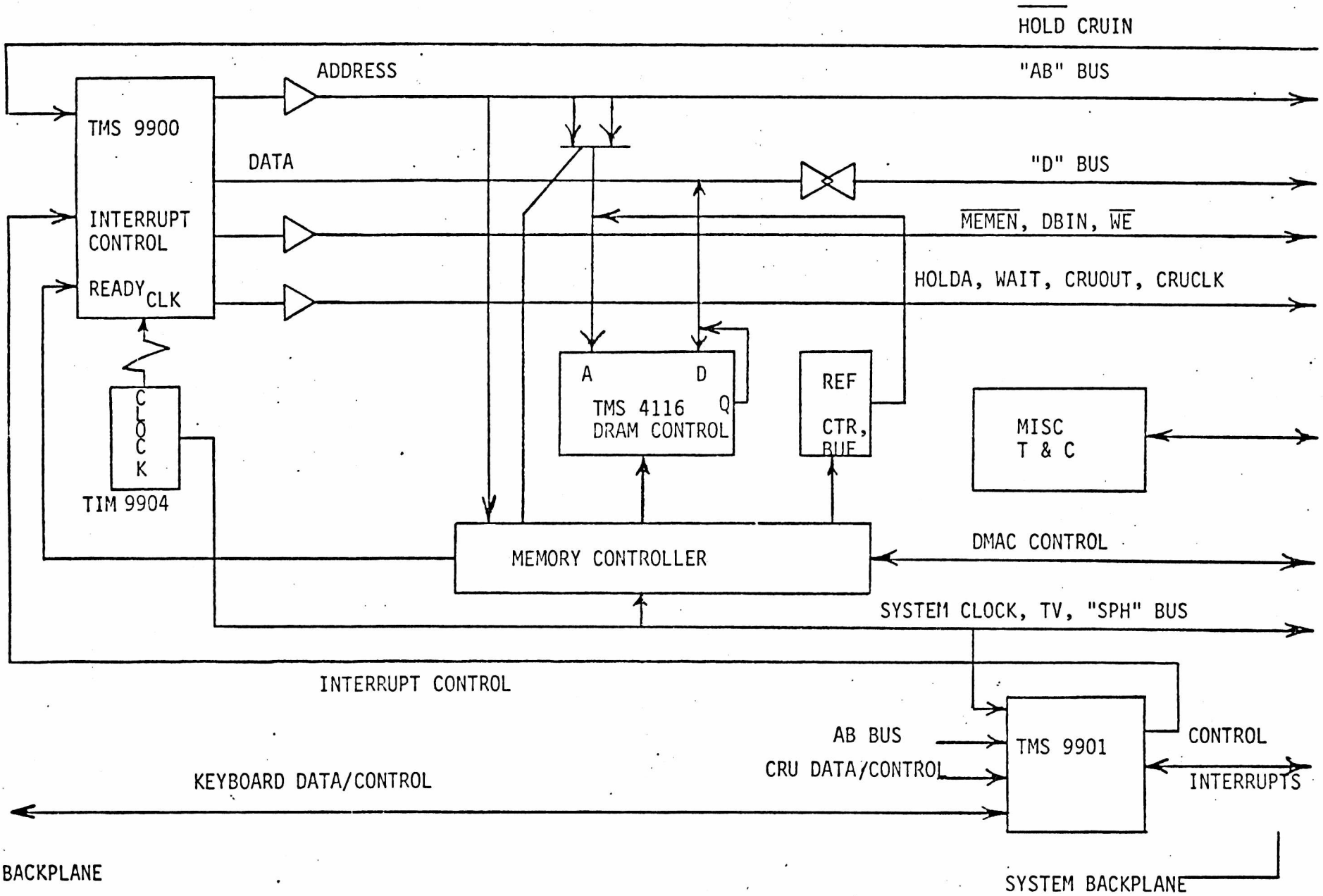


FIGURE 3.6.1 MLB1 BLOCK DIAGRAM

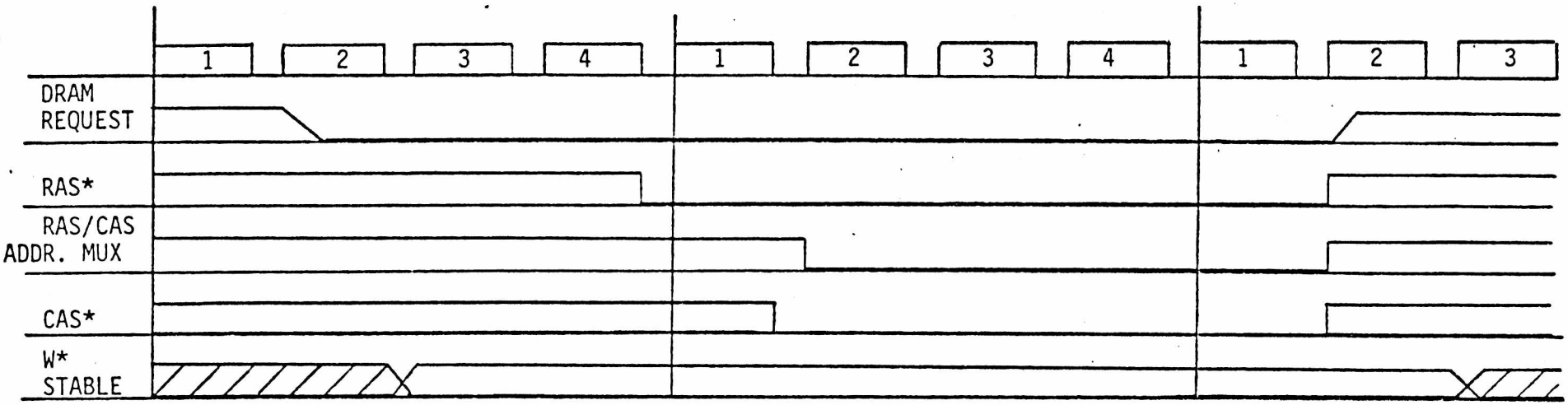


FIGURE 3.6.1.2 DRAM EARLY WRITE TIMING

3.6.1.2 MLB1 Functional Characteristics (Continued)

The Memory Controller shall have the following characteristics:

1 It must complete a Refresh cycle every 2 ms, and Refresh requests have priority over either CPU or DMAC requests;

2 It must provide the Refresh Address and its gating to the DRAM address bus;

3 It must inhibit CAS* during a Refresh cycle, and force the DRAM R/W to the Read mode;

4 It must provide a DMAC cycle inhibit during a Refresh cycle.

5 The basic memory cycle timing will be: R/W is synchronized on the LE of PH3(1) - Phase 3, first clock cycle of a memory request;RAS* goes low true on the TE of PH4(1); the row address changes to the column address on the TE of PH1(2); CAS* goes low true on the LE PH2(2); READ data will be taken by the CPU during PH1(2);and RAS*, CAS*, and the address control are Reset on the LE PH2(2);

6 The DRAM must cycle on a byte basis for DMAC requests, and on a word basis for CPU requests. Both RAS and CAS on the byte not selected will be inhibited in the byte mode;

7 It must provide signals necessary for system operation;

8 It must provide for "Early Write" operation (W* stable prior to CAS*).

Two test points are provided by the Memory Controller that may be utilized by Production for PWB testing. TP2, when low, causes the Refresh divide by 45 counter to be held clear, and TP3, when held low, causes the DRAM to function as a word oriented memory during a DMAC memory request. Both of these test points have pull-up resistors to keep them inactive during normal operation.

TABLE 3.6.1 Keyboard CRU Definition

KBD	MLB1 9901	DISPLACEMENT FROM 200
KBI*	INT6*	6
KBIRST*	P8 - Normally = 1. Set to	18
KB7 (MSB)	P7 zero to clear the KBD	17
KB6	P6 interrupt, and then back	16
KB5	P5 to one to enable the	15
KB4	P4 next possible KBD	14
KB3	P3 interrupt.	13
KB2	P2	12
KB1	P1	11
KB0 (LSB)	P0	10

KBIRST* is a low-true, normally high signal used to RESET the keyboard interrupt source.

3.6.1.2 MLB1 Functional Characteristics (Continued)

The keyboard interface is the fifth area of interest. The KBD furnishes MLB1 with 8 bits of data and one low true level controlled interrupt signal. MLB1 furnishes the KBD logic with a low true Interrupt Reset line. The CRU signal addresses are tabulated in Table 3.6.1, and the Interrupt definition is in Section 3.3.

The general sequence of KBD operation starts when a key is depressed. The key data is first stabilized, and then the interrupt Level 2 line is driven low. It is the responsibility of the KBD interrupt service routine to Reset the KBD Interrupt source with the KBIRST* signal as is noted Table 3.6.1. See Section 3.7 for additional keyboard details, and Figure 3.7.6 for a basic Interrupt Service Flow Chart for a keyboard Interrupt.

The sixth area of interest is in the Buffering and Control logic. The 15 address lines, MEMEN*, DBIN, and WE* from the CPU are buffered to form a TTL Tri-state signal group. HOLDA, WAIT, CRUOUT, and CRUCLK from the CPU are buffered to form an ungated buffered group. The data bus bidirectional drivers must be controlled as a function of MEMEN*, DBIN, the MSB of the address Bus, and the DMAC cycle indicator. The DMAC has priority over the CPU since it is the DMAC that places the CPU on HOLD to gain access to the memory. A Refresh Cycle has priority over both the CPU and DMAC.

Control must be provided to insure that the CPU comes up from Reset in the LOAD mode, that either the software Reset or Power-on-clear signal cause the CPU Reset pin to be low at least four full clock cycles, and that the CPU READY line can be driven from the system bus or the Refresh logic. MLB1 will also furnish to the system a high true decode to indicate the CRU address space (A0*.A1*.A2*).

3.6.2 MLB2

The purpose of MLB2 is to provide system interface to both the floppy disk drive pair and the thermal printer. MLB2 shall be designed according to Section 3.0.

3.6.2.1 MLB2 Basic Block Diagram

Figure 3.6.2 shows the basic outline of MLB2.

3.6.2.2 MLB2 Functional Characteristics

For characterization MLB2 may be broken into the five basic areas which are enclosed by dashed lines in Figure 3.6.2.

The DMAC section requires a 16 bit Address Counter for byte addressing, a tri-state Counter to Address Bus driver, and the necessary logic to emulate the CPU MEMEN, DBIN, and WE* timing. The Address Counter must be loaded from the system Data Bus, and functions as "Write Only Memory" organized at F000. With the exception of the method of loading the Address Counter, the DMAC section shall be easily replacable with the future TMS 9911 DMAC chip. The LSB of the Address Counter is

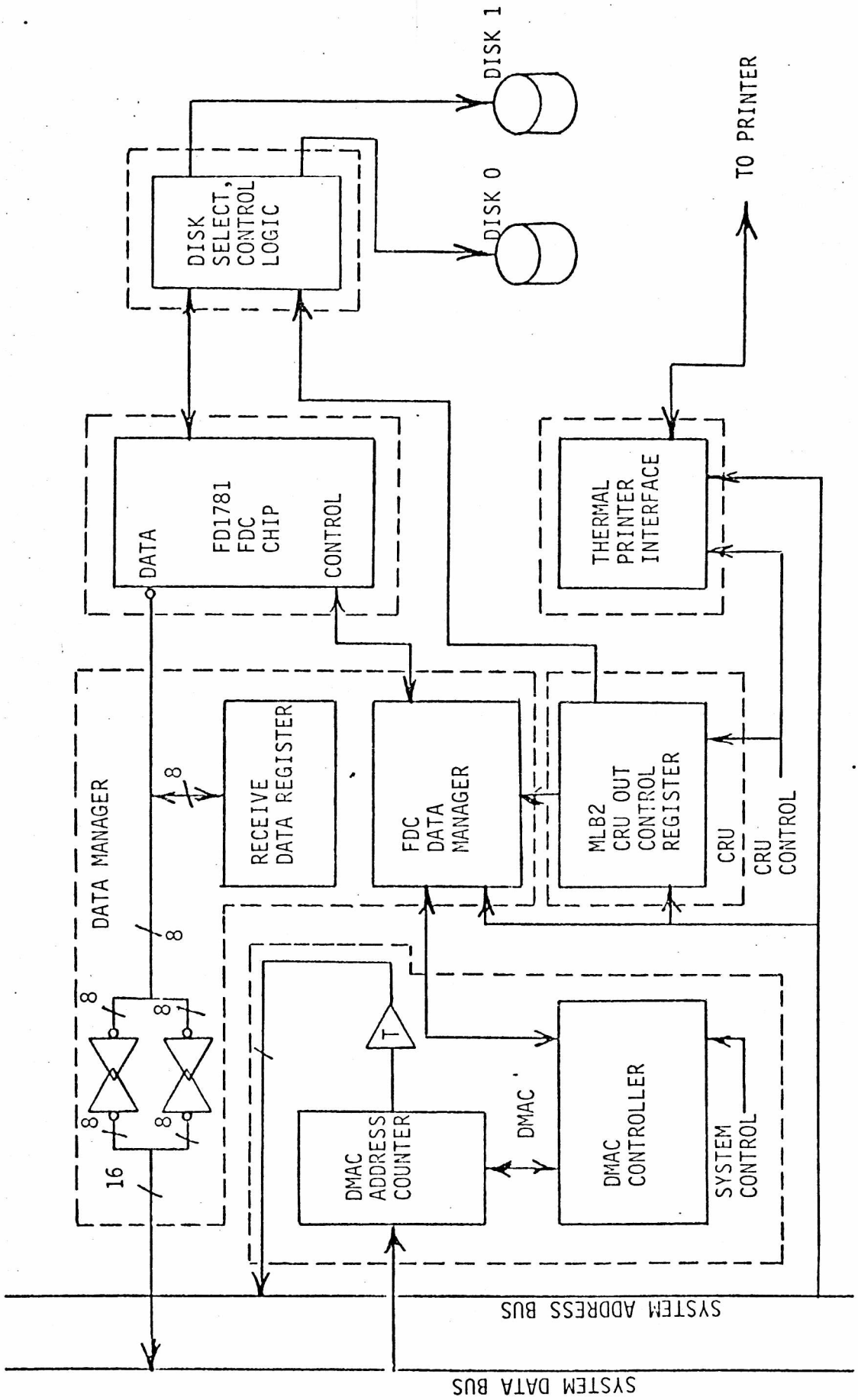


FIGURE 3.6.2 MLB2 BASIC BLOCK DIAGRAM

synchronized with PH3 and sent to MLB1 as a BYTE Pointer for the DRAM area. When zero it indicates the MSBY, and when one it selects the LSBY.

The Data Manager serves as an interface between the TMS9900 based system architecture and the FD1781 Floppy Disk Controller chip. It must provide the 100 ns address set up time before before a control strobe as well as the 50 ns address hold time after it. It must also provide for a 500 ns Read access from a Read strobe (this is a 600 ns + cycle time), and a 350 ns min Write strobe pulse width. Data must be held for 10 ns after the Write strobe goes false (high). See Figure 3.6.2.2.

The Data Manager must also provide the byte switching on the data bus and request DMAC cycles as they are required by the Floppy Disk Controller chip. Byte switching is utilized to pack pairs of 8 bit bytes from the Floppy Disk Controller chip into 16 bit DRAM words on MLB1. This is accomplished by controlling the Floppy Disk Controller data path to the System Data Bus (see Figure 3.6.2), as well as by placing the DRAM Memory Controller in the byte mode. The DMAC Address Counter provides the Memory Controller with the proper byte selection as was previously mentioned.

A 16 bit CRU output register on MLB2 based at E00 and semicontiguous in nature in the CRU address space will provide the necessary control for MLB2 logic. The bit definitions are found in Section 3.2.1.

The Floppy Disk Controller chip requirements were discussed briefly earlier in this section, and Appendix H is the manufacturer data sheets. Programming characteristics are found in Section 3.9.4.

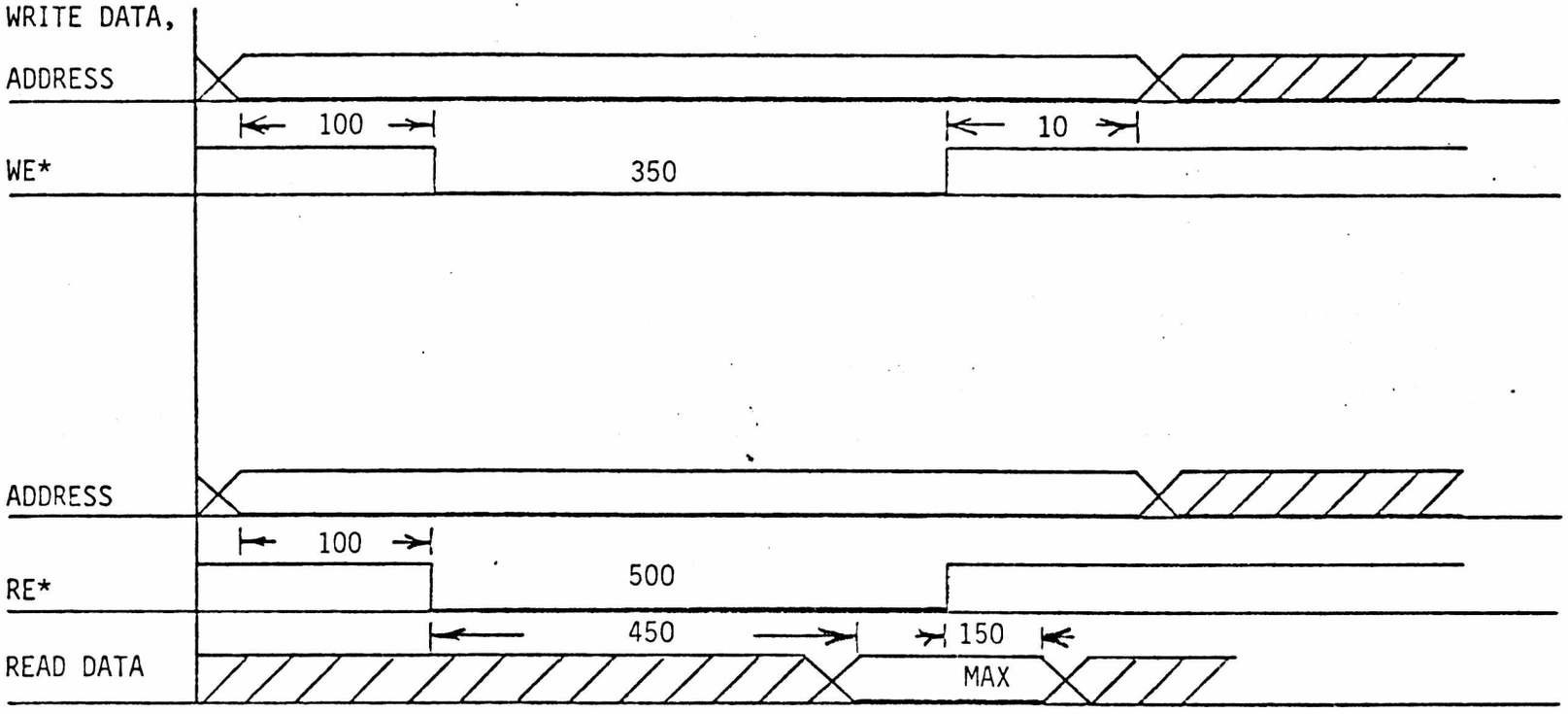


FIGURE 3.6.2.2 FLOPPY DISK CONTROLLER CHIP

3.6.2.3 Hardware Description

The mini-floppy controller hardware specification may be grouped into seven small sub blocks that are labelled Floppy Disk Control, clock circuit, head load counter, line receivers, line drivers, write channel, and read channel. Figure 3.6.2.3 shows these sub blocks. The floppy disk controller interface to the system Mainframe consists of the CRU bus and the most significant byte of the data bus. Status, commands, and data bytes are transferred to the system over the data bus. Control bits such as disk select, floppy disk controller reset, and motor-on are derived from the CRU bus. Data transfer during read and write operations is achieved by the DMA controller and Data Manager which are described in Section 3.6.2.2. Cable interface to the floppy disk consists of two 34 line ribbon cables and connectors. Of the 34 lines, odd numbered pins are tied to ground and only twelve of the even numbered pins are used. For line assignments see Section 3.11.2.4. The mini-floppy signal interface lines are Low true. The sub block noted as the Floppy Disk Controller consists only of the Western Digital 1781 floppy disk controller integrated circuit. Its operation is detailed in Section 3.9.4, and complete manufacturer's data is included in Appendix H.

3.6.2.3.1 Controller Clocks

The clock circuit sub section provides the Floppy Disk Controller with a 73.6 millisecond delay for head loading use.

3.5.2.3.2 Line Receivers

The Line Receivers must provide termination for the open collector signals generated by the floppy disk drive circuitry. These signals are Read-Data, Write-Protect, Track-00, and Index/Sector.

Outputs from both drives are tied together at the line receiver input circuitry. The required termination is in the range from 100 to 150. ohms at the input of a 74LS14 Schmitt Trigger inverting buffer (the input impedance of the Schmitt Trigger is disregarded in the impedance specification).

3.6.2.3.3 Line Drivers

The line driver circuitry must buffer all controller outputs to the disk drives. The drivers should be 7438 open collector gates. The buffered outputs are two side-selects, two motor-on lines, two drive-selects, a write-gate, write-data, direction-select, and step lines. The step, motor-on, head-select, and drive-select lines are individually controllable.

3.6.2.3.4 Write Channel

The write channel circuitry shall encode data according to the MFM rules, and insert the proper address marks. Input data shall be of the form in the Floppy Disk Controller spec (see Appendix H) as delivered by the Floppy Disk Controller. Output data shall conform to floppy drive specifications of selected vendor/vendors.

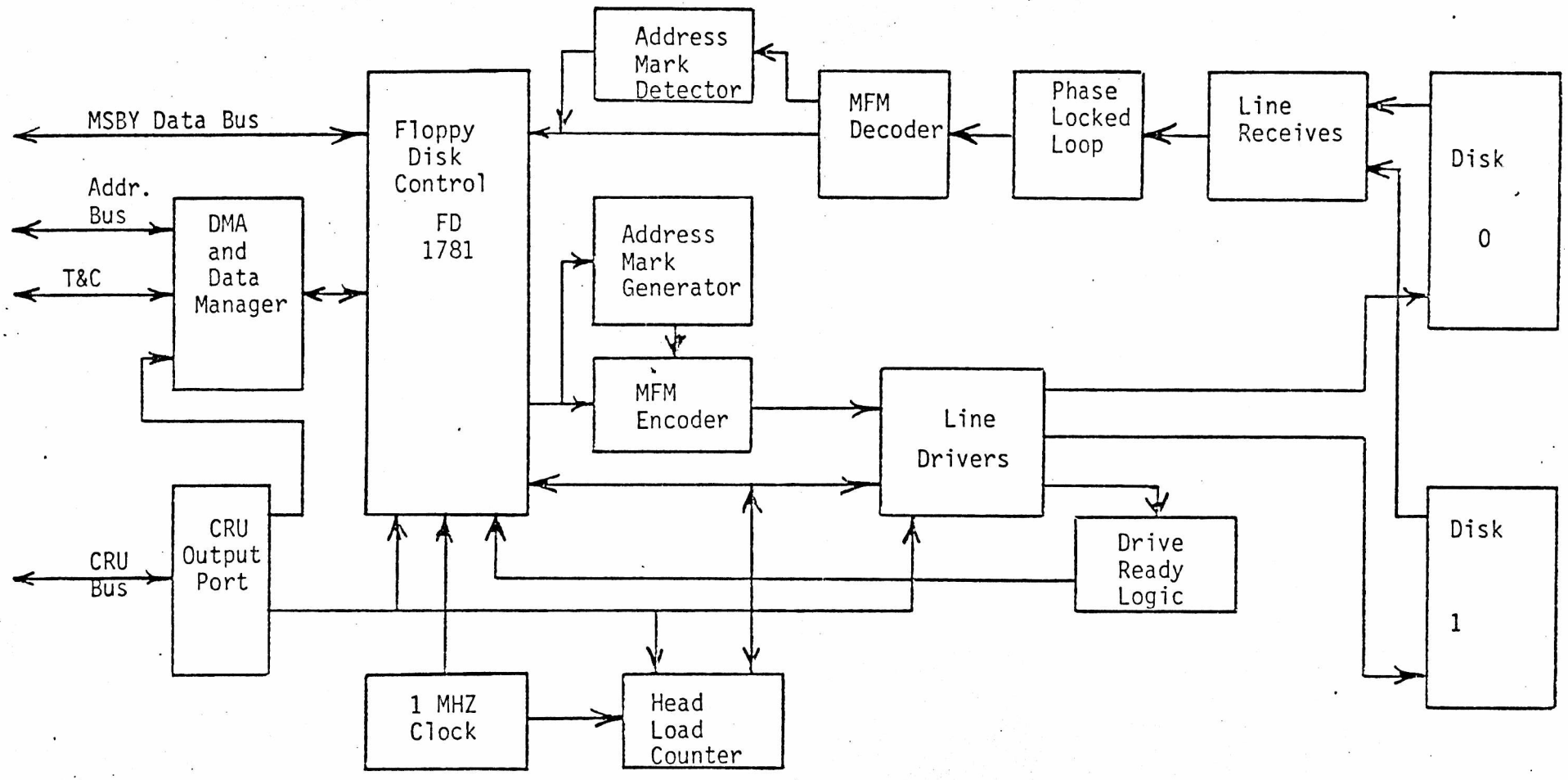


Figure 3.6.2.3 MFM Disk Controller Block Diagram

3.6.2.3.5 Read Channel

The read channel shall accept data from the floppy disk and separate it into clock and data streams. Separation shall be accomplished by using a phase locked loop. The read channel must also be capable of detecting and recovering address marks.

3.6.2.4 Printer Interface Description

The Thermal Printer interface from the system to the TMS9940 based Thermal Printer involves both the CRU Bus and Interrupt logic. The CRU will be based on E20 for data transfer and at E00 for any control required. The CPU Interrupt Level will be #8. The communication protocol between the CPU and the printer is defined in Section 3.8.

3.6.3 MLB3

The purpose of MLB3 is to provide outside world communications interface in the form of an RS-232-C port as well as a 2K bit CRU port, and to provide a monitor interface.

3.6.3.1 MLB3 Basic Block Diagram

Figure 3.6.3.1 shows the video/CRU demarkation for MLB3. The CRU partition is further subdivided into the RS-232-C and the 2K bit CRU port.

3.6.3.2 MLB3 Functional Characteristics

3.6.3.2.1 Video Characteristics

The fundamental Video Timing and Control shall be generated by a SMC CRT 5027 chip (which will be second sourced by TI). See Appendix J for CRT 5027 details. The CPU may directly access the video chip by first setting a TV page bit High in the On Board CRU. See Figure 3.6.3.2 for a basic flow chart depicting the chip access.

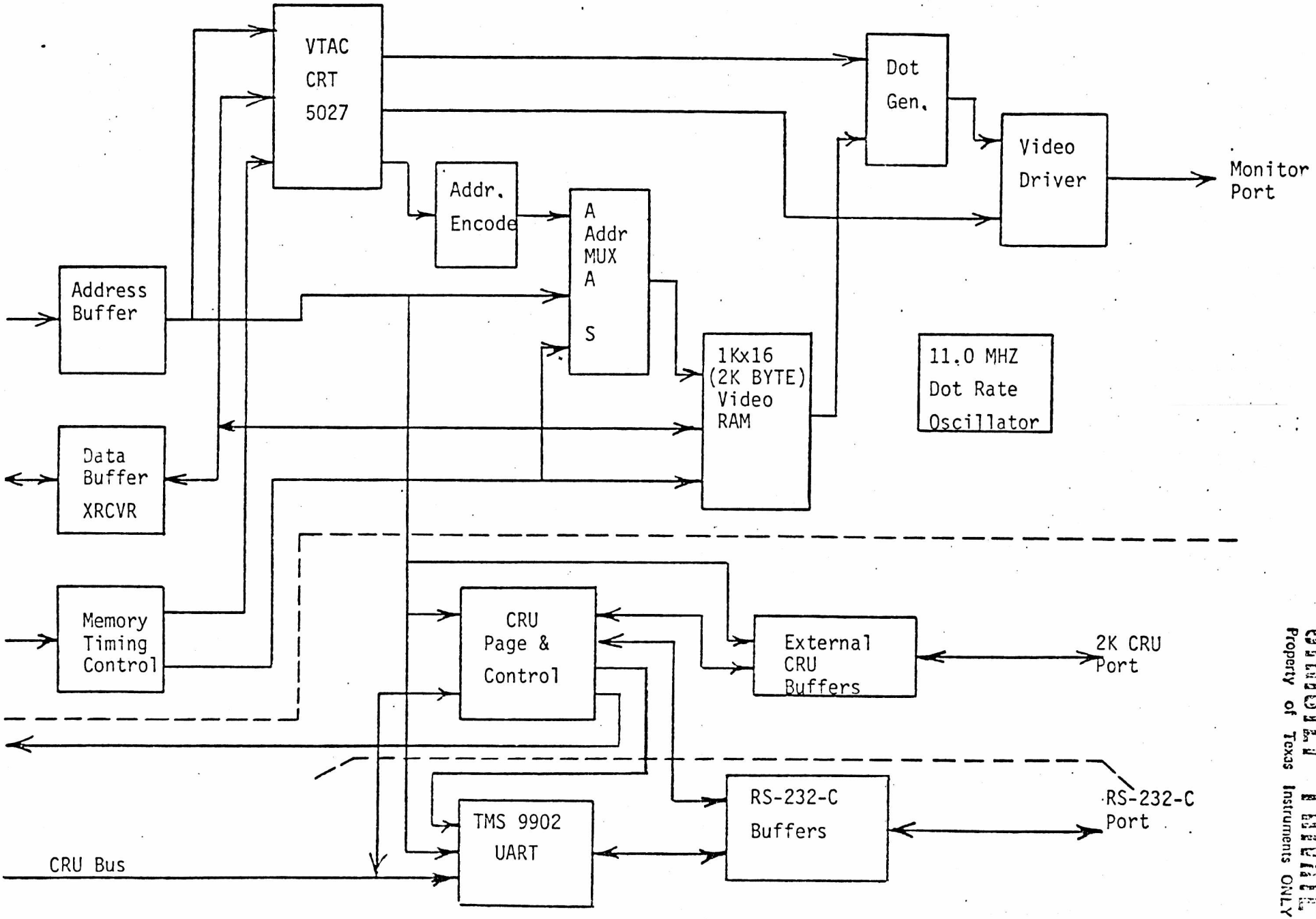
All signals derived from the System Bus shall drive 1 74LS unit load maximum; therefore, all data and address lines shall be buffered prior to their utilization in the video logic.

A 2K byte Video RAM organized as a 1K X 16 RAM based at 8000 when paged in shall be included. The CPU shall be able to directly access this RAM in a READ/WRITE mode, and "Early Write" will be the process utilized for Write cycles (the W* input is set up prior to and held after the chip select input is driven). Standard CPU 500 ns Memory Cycle timing shall be used for CPU Accesses, and 636 ns timing shall be used for Dot Generator Accesses. Character packing in the Video RAM shall be sequential in nature for assending addresses. The upper left hand character on the screen shall be located at the Zero address (8000 system level). Figure 3.6.3.3 is a basic flow chart depicting CPU access of the Video RAM.

The Dot Generator shall access the Video RAM to obtain ASCII characters, and produce dots on a 5 X 7 character font basis. There shall be a 7 X 10 Field Matrix, an 80 character Row, and 24 characters per Frame. The dot rate shall be 11.0 MHz which in turn yields a 1.571 MHz Character rate. A separate 11.0 MHz on board oscillator shall be utilized to obtain the previously specified dot rate.

There shall be 128 defined ASCII characters. Included in this set shall be: upper case alpha, pseudo lower case alpha, and graphics characters. Appendix K denotes the ASCII code.

Scrolling is accomplished thru the SMC CRT 5027 chip. See Appendix J for the CRT 5027 Data Sheet. The cursor shall blink at a 2 Hz rate.



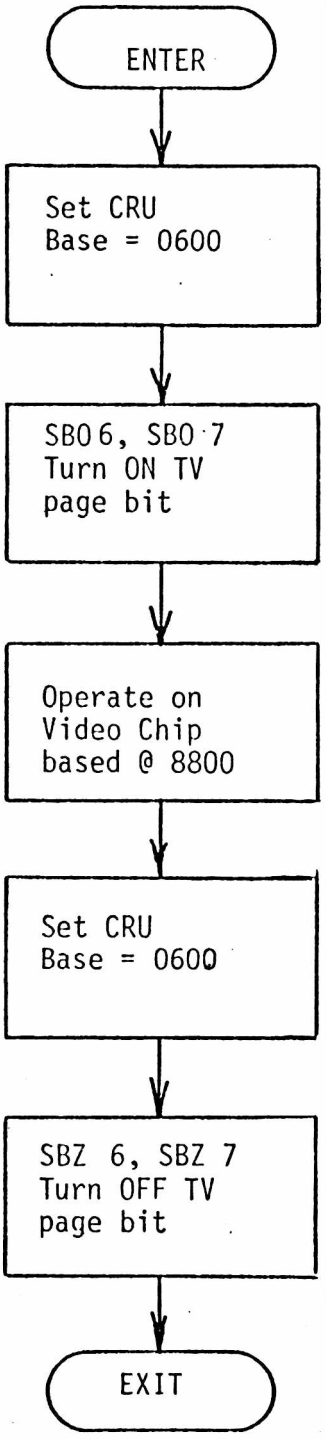


Figure 3.6.3.2 Basic Flow Chart for CRT5027 Access

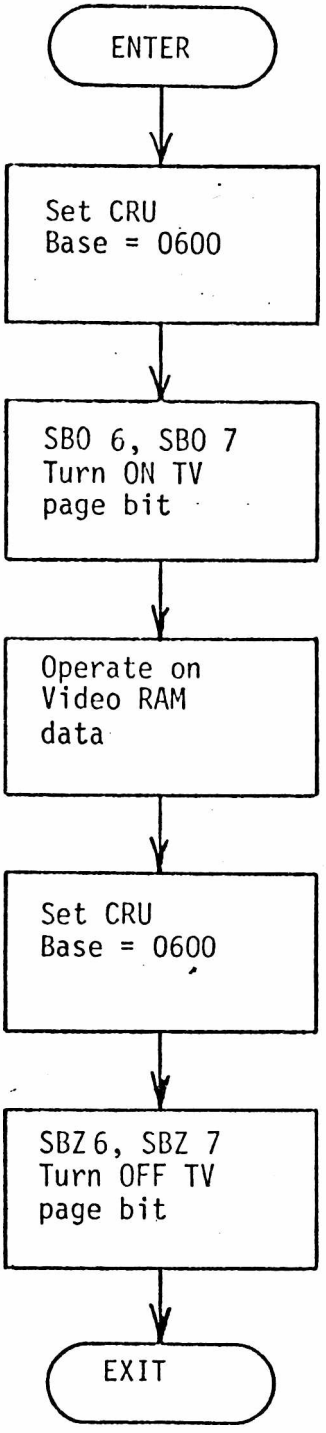


Figure 3.6.3.3 Basic Flow Chart for Video RAM Access

Three TTL level signals shall be provided on MBL3 for cable connection to the monitor. Horizontal drive control, vertical drive control, and video comprise this set. The Monitor Supply voltage of +15VDC shall also be supplied from MLB3 to the Monitor Cable such that only one cable connects the Monitor to the system. See Section 3.10 for the Monitor power specifications, and Section 3.13 for Monitor characteristics.

3.6.3.3 CRU Characteristics

The CRU Section on MLB3 shall serve three purposes. It shall provide paging for Operating System ROM, TV chip, and any future blocks that may be paged ON in the 8000 to 9FFF memory space. Section 3.2 defines the bit positions for this space based at 0600.

A TMS 9902 UART shall be utilized to provide a controller for the RS-232-C port. Additional lines required in the RS-232-C port, but not provided for in the MTS 9902, shall be interfaced to the MLB3 on-board CRU Input port. The TMS 9902 is based at 0000, and the additional lines not provided for in the TMS 9902 are based at 0040. Section 3.2.1 has a detailed bit definition for each function in the CRU space. Figure 3.6.3.4 a basic Flow Chart of the TMS 9902 Device Service Routine.

The 2K bit outside world CRU interface shall provide the following buffered lines:

- the least significant 11 address bits,
- CRUOUT, CRUCLK, CRUIN, for the CRU Bus,
- five interrupt lines (each shall be pulled up to +5V by a 390 resistor). See Section 3.3 for Interrupt Level definitions,
- System Reset, and System Phase 3* clock for TMS 9901/TMS 9902 use, and
- outside world space selected line (low True).

Section 3.12 contains complete bit definitions for both the RS-232-C port and the CRU port.

Careful consideration shall be given to the connection of I/O Grounds to the system ground on MLB3.

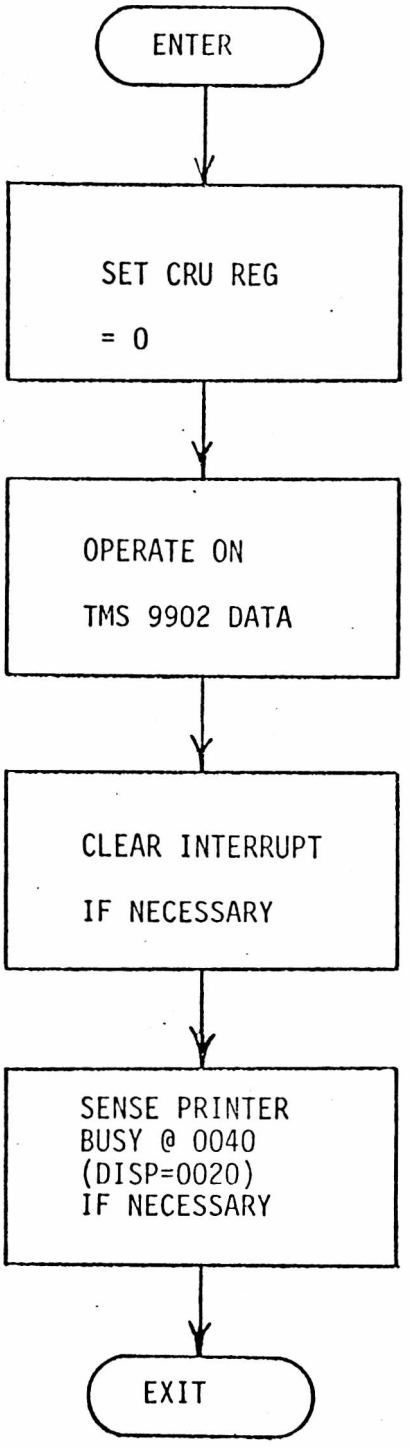


FIGURE 3.6.3.4 BASIC TMS 9902 SERVICE FLOW CHART

3.6.4 MLB4

The purpose of MLB4 is to provide both Primary and Secondary ROM storage.

3.6.4.1 Basic MLB4 Block Diagram

Figure 3.6.4.1 shows a basic block diagram of MLB4 dividing it into the Primary and Secondary ROM functions. All system level signals shall be buffered prior to their use.

3.6.4.2 Primary ROM

The Primary ROM shall occupy the System Memory Space from 8000 thru FFFF, and shall be contiguous in nature from A000 thru FFFF. The section contiguous from 8000 thru 9FFF is in the Paged memory area (see Section 3.1.1), and when paged in the memory space from 8000 to FFFF will be contiguous. Primary ROM chips shall be 4K X 8, 450 ns, 5V only parts (TMS 4732).

3.6.4.3 Secondary ROM

Secondary storage in the form of TMC 0350 "BROMs" shall be provided. The BROM has its own Memory Address counter which operates under external control Appendix L provides a TMC 0350 data sheet.

Complete access of the Secondary ROM shall be affected thru the system CRU.

The BROM chips shall be organized in pairs (16 pairs, total) to form an 8 bit wide bus for reading and a 4 bit wide bus for internal address loading. The least significant address nibble is loaded first in loading the BROM internal Address Counter, and a dummy READ is required before the first word is available at the output pins. Figure 3.6.4.3 is a basic Flow Chart of a typical BROM Access.

Table 3.6.4.3A shows the BROM CRU bit definitions, and Table 3.5.4.3.B gives the BROM control pin (I1, I0) definitions.

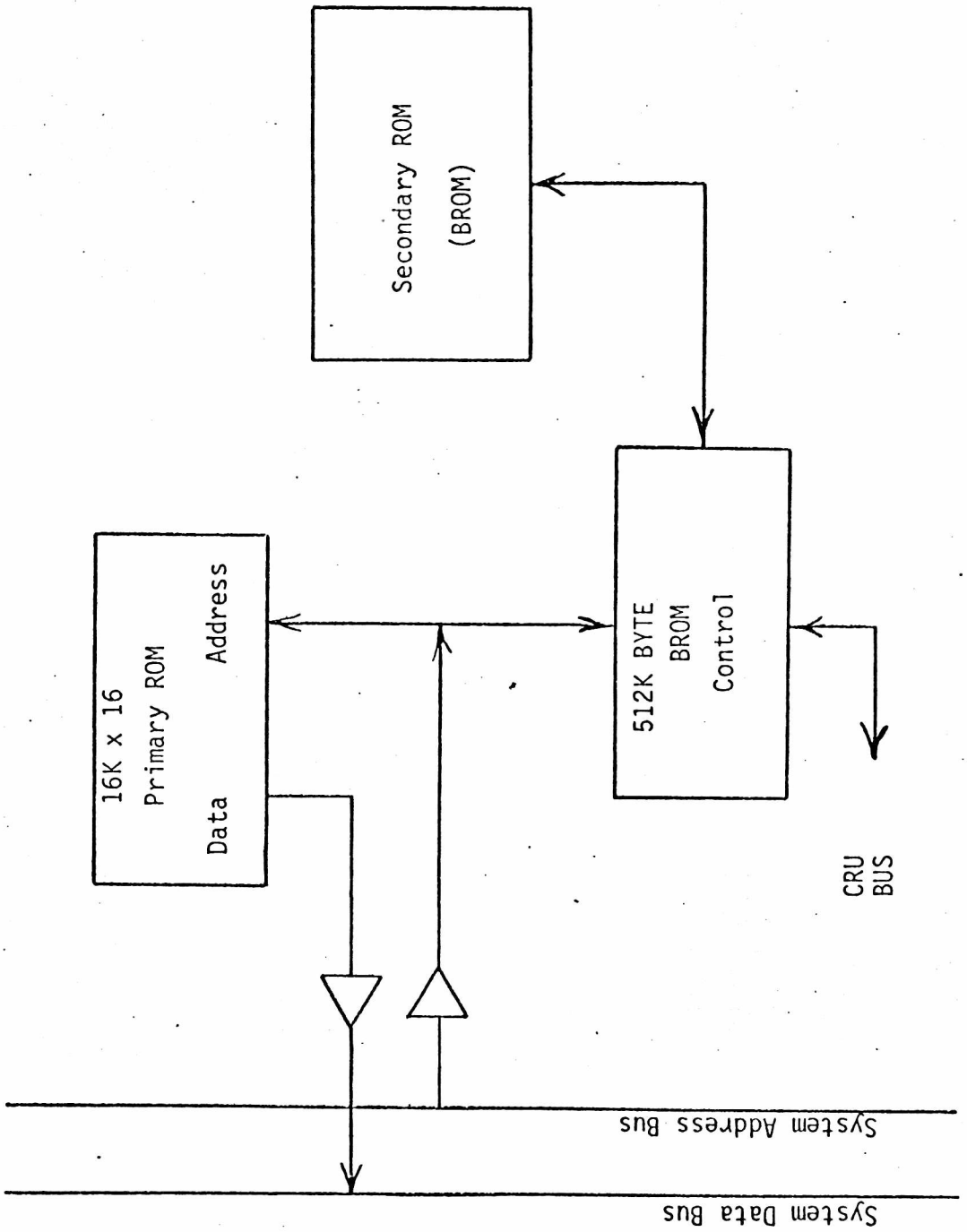


Figure 3.6.4.1 Basic MLB4 Block Diagram

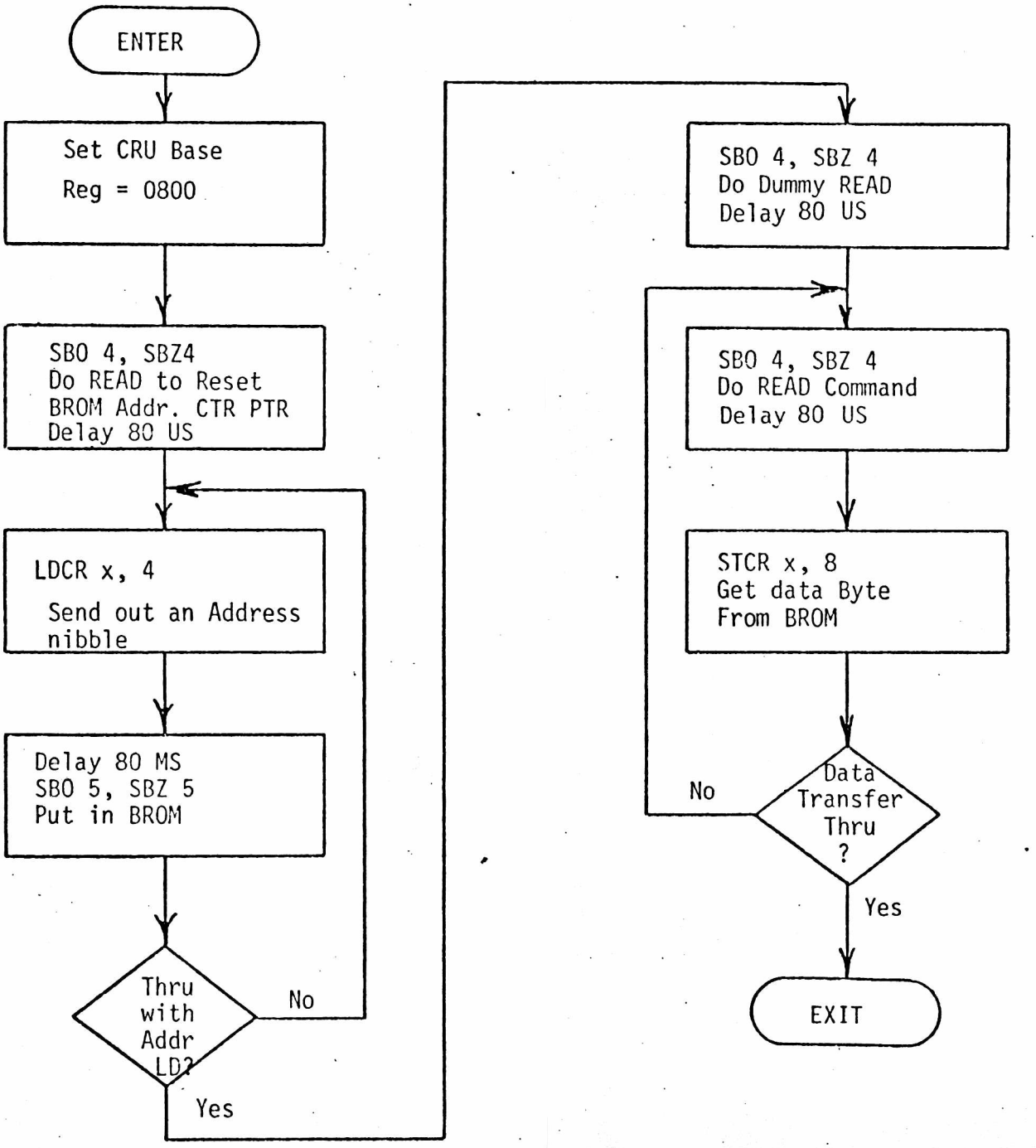


Figure 3.6.4.3 Basic BROM Access Flow Chart

Table 3.6.4.3A BROM CRU Bit Definitions

Displacement From 0800	Output Function
0	Address nibble #1 LSB
1	Address nibble #2
2	Address nibble #3
3	Address nibble #4 MSB
4	IO Control Line
5	I1 Control Line
6	SBROM Group Select LSB
7	SBROM Group Select MSB

Displacement From 0800	Input Function
0	BROM Data Bit #1 LSB
1	BROM Data Bit #2
2	BROM Data Bit #3
3	BROM Data Bit #4
4	BROM Data Bit #5
5	BROM Data Bit #6
6	BROM Data Bit #7
7	BROM Data Bit #8 MSB

Table 3.6.5.4.B BROM Control Bit Definition

Out Bit # 5	Out Bit # 4	
0	0	No operation - normal state
0	1	Read Byte
1	0	Load Address Nibble
1	1	Read and Branch - not implemented

3.6.5 Mainframe Interconnect

There are two back planes which provide MLB/MLB connection. Bus level signals may be tapped for one 74LS TTL unit load per MLB.

3.6.5.1 System Interconnect PLB

This PLB is utilized to provide a path between Main Logic Boards for signals common to several MLB's. Physically, it is located close to the SR-70 case; therefore, it may not be utilized for mainframe to internal peripheral connection. Appendix D defines the pin connections of the 100 pin (.125" spacing) connector.

A solid ground path is provided for power ground gridding purposes, and a static ground guards groups of high frequency signals; i.e., the clocks as a group. Common groups will be given sequential pin numbers (Address, Data, Clocks, etc.)

3.6.5.2 I/O Interconnect PLB

The purpose of the I/O Interconnect back plane is to provide MLB power in the form of GND, -12, -5, +5, +12, and +15V (for monitor), as well as a means of connecting the mainframe to the various internal SR-70 peripherals. Section 3.11 deals with the mainframe to peripheral connection scheme. Some CRU output register bits that are not presently assigned appear on this PLB. Appendix E lists each of the pin definitions of the 100 pin (.125" spacing) connector.

3.7 Keyboard

The SR-70 has an eighty-seven key X-Y matrix keyboard consisting of a QUERTY typewriter pad, numeric pad, and system control keys. The keyboard is an integral sub-section of the SR-70 with an encoder to deliver ASCII type code to the system. Keyboard mechanical requirements are described in CALD Drawing Number 101824-1.

3.7.1 Keyboard Basic Block Diagram

Figure 3.7.1 depicts the keyboard peripheral block diagram, and three basic sections are enclosed by dotted lines. The mechanical keyboard, the electronic keyboard encoder, and the control electronics comprise these three areas.

3.7.2 Keyboard Encoder Fundamental Characteristics

3.7.2.1 Encoder X-Y Scan

The keyboard encoder shall have a 10 X 10 scan capability.

3.7.2.2 Encoder Debounce

The keyboard encoder shall provide at least 10 ms of debounce time, but not greater than 20 ms.

3.7.2.3 X-Y Phantom Key Detection

The keyboard encoder shall detect a phantom key condition, and inhibit both a data strobe and a change of data at the encoder outputs.

3.7.2.4 Rollover

The keyboard encoder shall provide N-key rollover.

3.7.2.5 Encoding ROM

Table 3.7.2.5 depicts the bit pattern presented at the output for each key position and Figure 3.7.2.5 shows the relative key positions. The encoding ROM must present four different codes for each "data" key as a function of several control keys (or their past sequence).

Internal "shift" and "shift lock" circuitry must be provided. These two keys along with the "repeat" and "second function" keys must be wired directly to the keyboard encoder to provide the required 4 levels of code plus the "repeat" and "shift lock" functions.

The "shift lock" feature is provided by depressing either of the shift keys, and is removed by depressing either "shift" key again.

3.7.2.6 Output Data Latch

The keyboard encoder chip shall provide an output data latch that provides stable data no later than the leading edge of the data strobe. This output data shall remain stable until the next data strobe.

Keyboard lock

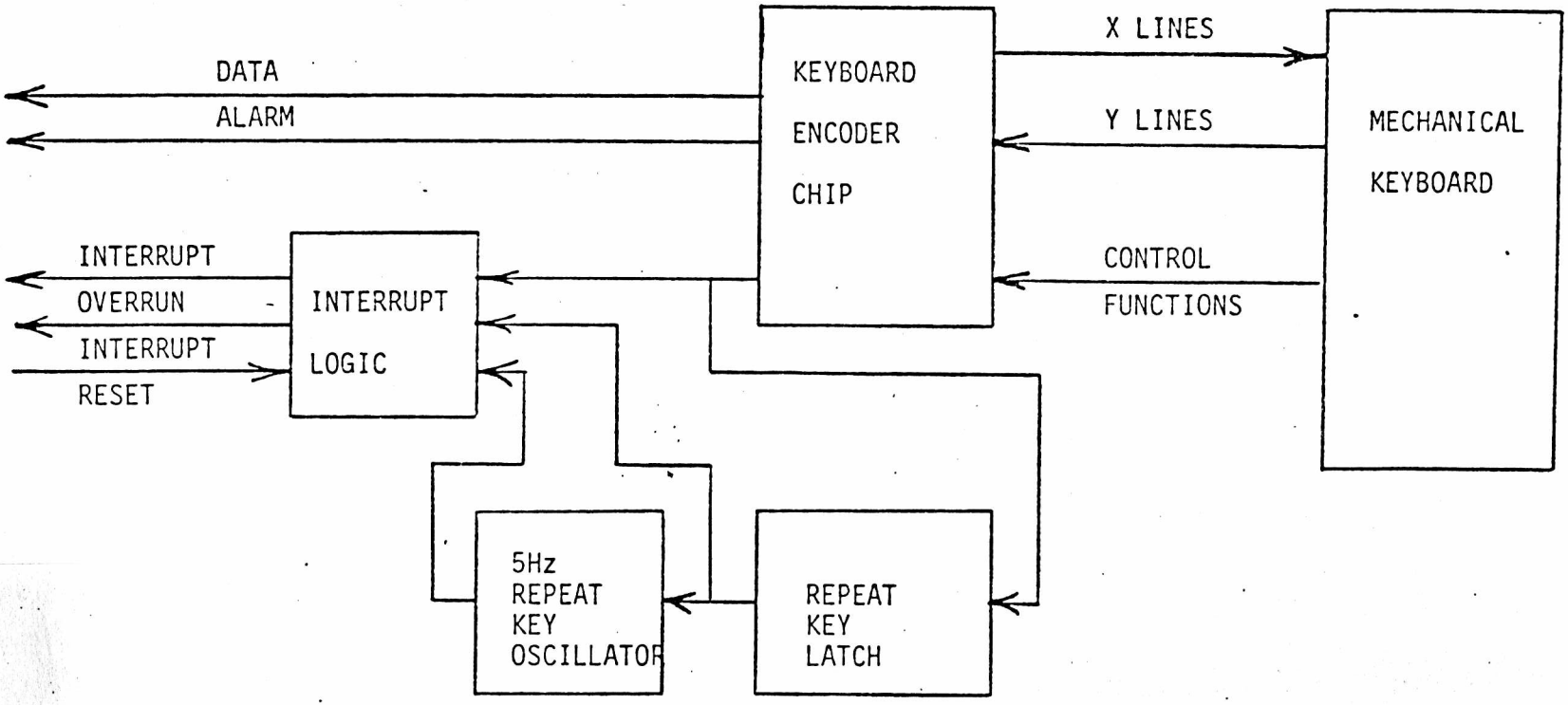


FIGURE 3.7.1 KEYBOARD BASIC BLOCK DIAGRAM

TABLE 3.7.2.5 Key Code Definitions

KEY #	NS	S	2ND	S2ND	FUNCTION	2 FUNCTION
1	10	10	10	10	HOLD	NONE
2	11	11	11	11	HELP	NONE
3	12	12	12	12	CONTINUE	NONE
4	13	13	13	13	STEP	NONE
5	14	14	14	14	BREAK	NONE
6	15	15	15	15	SYSTEM CLEAR	NONE
7	08	08	08	08	←	NONE
8	18	18	18	18	→	NONE
9	19	19	19	19	↑	NONE
10	1A	1A	1A	1A	↓	NONE
11	1B	1B	1B	1B	INSERT CHARA	NONE
12	1C	1C	1C	1C	DELETE CHARA	NONE
13	1D	1D	9D	9D	PRINT MONITOR	NONE
14	1E	1E	9E	9E	PAPER ADVANCE	NONE
15	09	09	89	89	TAB	BACK TAB
16	31	21	B1	B1	1 !	AUTONUM
17	32	40	B2	B2	2 @	BRKPNT
18	33	23	B3	B3	3 #	ECHO
19	34	24	B4	B4	4 $	EDIT
20	35	25	B5	B5	5 %	LIST
21	36	7C	B6	B6	6 |	LOAD
22	37	26	B7	B7	7 &	MERGE
23	38	2A	B8	B8	8 *	RENUM
24	39	28	B9	B9	9 (	RUN
25	30	29	B0	B0	0)	SAVE
26	2D	5F	AD	AD	- _	TRACE
27	3D	2B	BD	BD	= +	UNLOAD
28	60	7E	E0	E0	' ~	NOT ASSIGNED
29	71	51	F1	F1	q Q	ASSIGN
30	77	57	F7	F7	w W	CALL
31	65	45	E5	E5	e E	CLOSE
32	72	52	F2	F2	r R	DATA
33	74	54	F4	F4	t T	DEF
34	79	59	F9	F9	y Y	DIM
35	75	55	F5	F5	u U	DISPLAY
36	69	49	E9	E9	i I	ECHO
37	6F	4F	EF	EF	o O	ELSE
38	70	50	F0	F0	p P	END
39	5C	5E	DC	DC	\ ^	NOT ASSIGNED
40	5B	7B	DB	DB	[{	NOT ASSIGNED
41	5D	7D	DD	DD	] }	NOT ASSIGNED
42	ND	ND	ND	ND	SHIFT LOCK	NOT DEFINED
43	61	41	E1	E1	a A	FNEND
44	73	53	F3	F3	s S	FOR
45	64	44	E4	E4	d D	GOSUB
46	66	46	E6	E6	f F	GOTO
47	67	47	E7	E7	g G	IMAGE
48	68	48	E8	E8	h H	INKEY$
49	6A	4A	EA	EA	j J	INPUT
50	6B	4B	EB	EB	k K	INTEGER

Congruence with Asset control code

TABLE 3.7.2.5 Key Code Definitions (Continued)

KEY #	NS	S	2ND	S2ND	FUNCTION	2 FUNCTION
51	6C	4C	EC	EC	l L	LET
52	3B	3A	BB	BB	; :	NEXT
53	27	22	A7	A7	' "	NOT ASSIGNED
54	OD	OD	BD	BD	ENTER	REPLAY
55	ND	ND	ND	ND	SHIFT	NOT DEFINED
56	7A	5A	FA	FA	z Z	PRINT
57	78	58	F8	F8	x X	REAL
58	63	43	E3	E3	c C	REM
59	76	56	F6	F6	v V	RESTORE
60	62	42	E2	E2	b B	RETURN
61	6E	4E	EE	EE	n N	STOP
62	6D	4D	ED	ED	m M	THEN
63	2C	3C	AC	AC	, <	UNIT
64	2E	3E	AE	AE	. >	USING
65	2F	3F	AF	AF	/ ?	NOT ASSIGNED
66	ND	ND	ND	ND	SHIFT	NOT DEFINED
67	ND	ND	ND	ND	2 FUNCTION	NOT DEFINED
68	20	20	20	20	SPACE	NOT ASSIGNED
69	ND	ND	ND	ND	REPEAT	NOT DEFINED
70	01	01	81	81	CALC	CLEAR ENTRY
71	28	28	A8	A8	(	NOT ASSIGNED
72	29	29	A9	A9	)	NOT ASSIGNED
73	2F	2F	AF	AF	/	NOT ASSIGNED
74	37	37	B7	B7	7	NOT ASSIGNED
75	38	38	B8	B8	8	NOT ASSIGNED
76	39	39	B9	B9	9	NOT ASSIGNED
77	2A	2A	AA	AA	*	NOT ASSIGNED
78	34	34	B4	B4	4	NOT ASSIGNED
79	35	35	B5	B5	5	NOT ASSIGNED
80	36	36	B6	B6	6	NOT ASSIGNED
81	2D	2D	AD	AD	-	NOT ASSIGNED
82	31	31	B1	B1	1	NOT ASSIGNED
83	32	32	B2	B2	2	NOT ASSIGNED
84	33	33	B3	B3	3	NOT ASSIGNED
85	30	30	B0	B0	0	NOT ASSIGNED
86	2E	2E	AE	AE	.	NOT ASSIGNED
87	2B	2B	AB	AB	+	NOT ASSIGNED

NOTE: KEYS 42, 55, 66, 67, and 69 are not X-Y DECODED, BUT SPECIAL, UNIQUE KEYS.

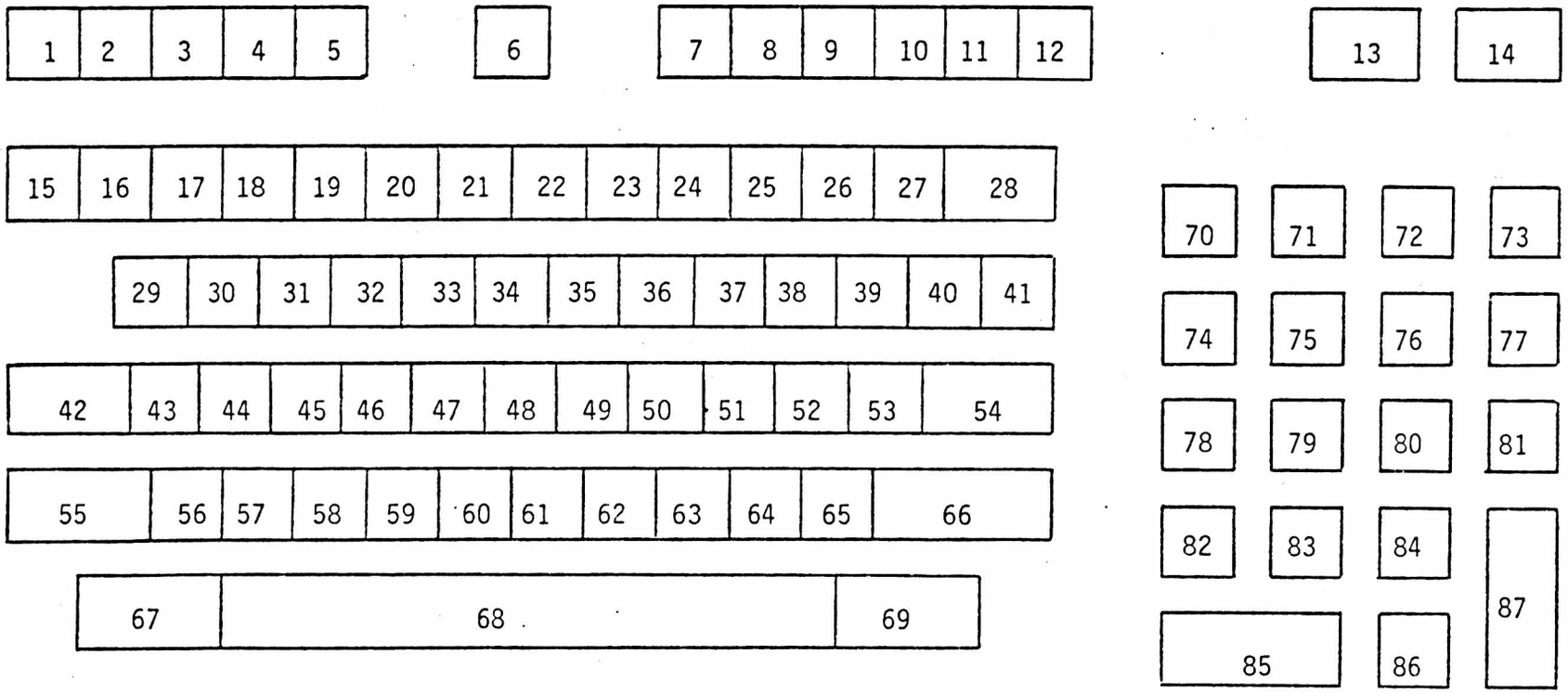


FIGURE 3.7.2.5 KEYBOARD KEY POSITIONS

3.7.3 Repeat Key Characteristics

3.7.3.1 Repeat Frequency

The repeat key shall cause a data repetative strobe from 4.5 Hz to 5.5 Hz. The generation of this shall be external to the keyboard encoder chip.

3.7.3.2 Repeat Oscillator

The repeat oscillator shall be external to the keyboard encoder chip.

3.7.3.3 Repeat Key Latch

The repeat key latch shall be external to the keyboard encoder chip.

3.7.3.4 Repeat Key Operation

The repeat key decode line from the keyboard encoder will provide from an external source strobes on a 4.5 Hz to 5.5Hz frequency to repeat the next key depressed decode. This repeat strobe will continue as long as the repeat key is held down.

3.7.4 Data Overrun

Data overrun logic shall be provided to detect the occurrence of a second data strobe from the strobe logic (keyboard encoder ORed with repeat oscillator) before the previous keyboard interrupt was reset by the CPU (new data in output Register before CPU has read the previous key decode data).

3.7.5 Keyboard DSR Characteristics

Each key has four levels of operation. The lower case (non-shift mode) is the first level. Level II consists of all capitalized or shifted keys. Levels III and IV will produce the same ASCII type code for each key. The third level uses the second function key as a higher level of shift. By using the shift and second function keys one will obtain the fourth level.

The keyboard keys are linked together in an X-Y matrix, except for the second function, repeat, shift, and shift lock keys. Each key station has an X and a Y line associated with it. The keyboard encoder is constantly scanning these lines for key closures, and once one is found the keyboard encoder signals the CPU to interrupt Level 2.

The shift and second function keys, at the time of key closure, determine the level of the depressed key. With the key position and its level, the keyboard encoder outputs an eight bit ASCII Type code and a strobe pulse. The strobe pulse controls onboard logic to provide the system with an interrupt. When the system receives the interrupt, the DSR software reads the eight data bits from the keyboard CRU input port beginning the the CRU address of 0200. See Section 3.2.1 for a full definition. The system next resets the interrupt by setting the KYBICLR* CRU bit to zero, and then back to one. Figure 3.7.6 shows a basic flow chart of the keyboard interrupt service routine.

The repeat key enables the user to input repetitive key entries without subsequent key closures. In order to input repetitive entries, one depresses the repeat key, and then the desired repeated character. The repeated characters will occur at approximately a five hertz rate as long as the REPEAT key is held down.

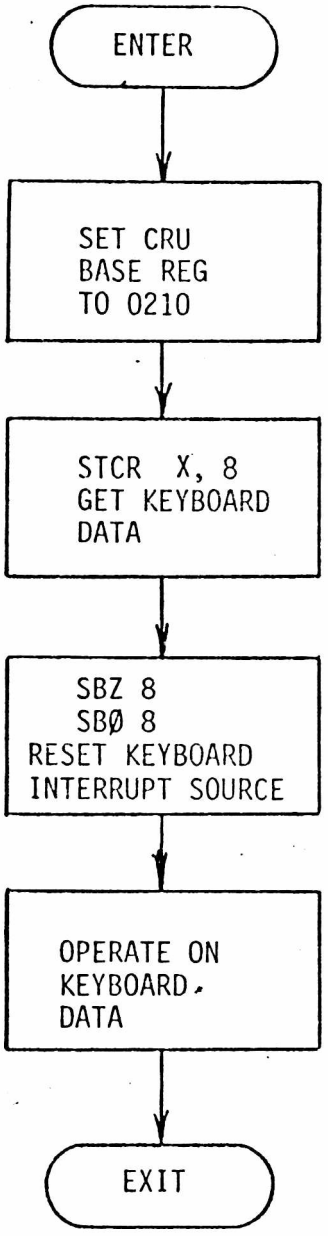


FIGURE 3.7.6
BASIC KEYBOARD INTERRUPT SERVICE
FLOW CHART

3.8 Thermal Printer

The thermal printer is one of the internal SR-70 peripherals which is controlled by the mainframe via an interface on MLB2.

3.8.1 Printer Basic Block Diagram

Figure 3.8.1 shows the basic characteristics of the thermal printer as five basic blocks.

3.8.2 Printer Functional Characteristics

The printer is to be a TMS9940, based module which accepts 16 bit control/data words via its CRU port from the CPU in the mainframe. The MSBY of this word will be a control character, and the LSBY will be data (if required by the control byte). Table 3.8.1 lists these commands.

MSBY	LSBY	FUNCTION
00	X	NOP, no interrupt response
10	data	First character in buffer (left to right build)
11	data	character for buffer anywhere after the first character
01	X	"Reset thyself"
02	X	Run checksum on ROM
03	X	Print RAM
04	MSBY, As^2	Print ROM
05	Hex data	Print Rom Address data
13	# of lines	Advance paper command
06	Don't Care	Test Mode #1
07	Don't Care	Test Mode #3

Table 3.8.1 Printer Command Definition

The handshake between the mainframe and the printer control is on an interrupt basis. The CPU will be interrupted on level 8, and the TMS9940 will utilize its Level 3 interrupt.

The loading of the forementioned CRU register by the mainframe will be done on a base of E20 in the mainframe CRU address space. The control necessary to create an interrupt in the TMS9940 will also utilize a pair of its CRU lines to effectively control its part of the interrupt logic.

One TMS9940 CRU out line (normally high) will be utilized to create a mainframe interrupt by performing a SBZ/SBO sequence to create a clocking pulse. The second line (normally high) will be utilized to reset a mainframe initiated interrupt to the TMS9940 by performing the same SBZ/SBO sequence. The same line function will be utilized by the mainframe in its interrupt control. See Section 3.2.1 for mainframe CRU definition.

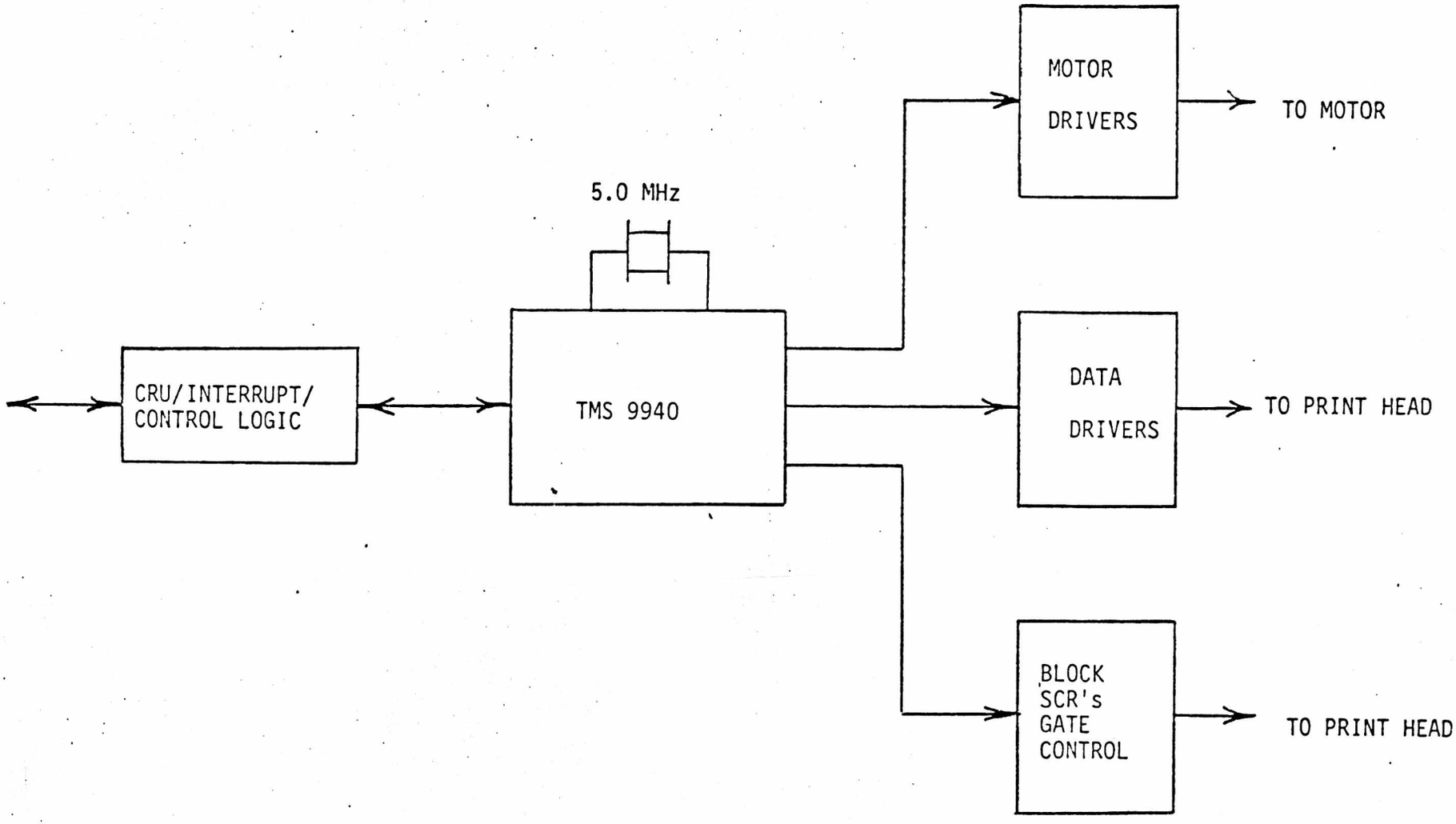


FIGURE 3.8.1 PRINTER BASIC BLOCK DIAGRAM

The mainframe supplies a low true "RESET" line to the TMS9940 that is a CRU output bit displaced from the E00 base by 2 as also were the two interrupt control lines.

In summary, there will be five control lines, adequately buffered at each end of the connecting cable, interfacing the printer module to the mainframe. There will be a mainframe E20 based CRUCLK, a CRUOUT bit, an interrupt source reset bit, an interrupt destination clock bit, and a TMS9940 Reset bit (the latter three originating at the MLB2 CRU control register).

The TMS9940 operates off of a 5MHz crystal to obtain a 2.5 MHz state time. The TMS9940 is responsible for generating all timing necessary to control the printer paper advance motor and the 5 ms printhead burn time.

The motor control is characterized by a quiescent "no drive" state. When told to print the TMS9940 advances the print motor four steps to produce a one line paper advance. The stepping sequence is as shown in Table 3.8.2 The motor step pulse width is 4 ms (16ms/line).

STEP #	A	A*	B	B*
1	ON	OFF	OFF	ON
2	ON	OFF	ON	OFF
3	OFF	ON	ON	OFF
4	OFF	ON	OFF	ON
STATIC	ON	ON	ON	ON

TABLE 3.8.2 Motor Stepping Sequence

After the last of the step pulses and an additional delay of 4ms, the print burn sequence is initiated. Each of the three heads is controlled in time sequence with the other two to limit the peak burn current to that of 16 elements (one burn element on each of 16 digits).

The 16 digit drivers will be turned either ON or OFF depending upon whether or not the element within that digit requires a burn. The state of the I/O line (high for SBO or low for SBZ) controlling the digit drivers for a burn will be determined in the design phase. The requirement that the removal of the TMS9940 or a prolonged system reset time NOT damage the printhead requires the I/O phase to be determined at this time. Once the digit drivers have been set up, the proper SCR (one out of five) is triggered to initiate the burn time. After a burn time of 5 ms the digit drivers must be set to the "No Burn" state to turn the SCR OFF.

The same sequence is followed for the other four elements in each digit.

Ideally, the element burn (5 elements per character) sequence probably should be 3,1,5,2,4 to more equally distribute the heat on the printhead.

After the element burn is complete for all three heads, a single line advance of the paper advance motor must be executed; then the other six lines must be burned exactly as the first line was. Following the last line burn will be two more paper advance lines.

As was previously mentioned, power must not be applied to the printhead if the TMS9940 is out of the socket or if the mainframe is reset. Any other reasonable precaution to protect the destruction of the burn elements must be applied (keep alive logic is acceptable). Digit drivers and/or SCR drivers must conform to this requirement. Since the SR-70 has a 3 printhead, 48 column printer, there are 3x5=15 element control SCR's. The control of these will be via the TMS9940 CRU port, and since there are 16 digits and 15 SCR controls, there are not enough CRU lines out of the TMS9940 to handle the motor, the printer, and the CRU/Interrupt interface. The 15 SCR lines must by nature be selected on a one out of 15 basis; therefore, they may be easily decoded.

The motor driver circuit should resemble those on mature CALD products utilizing the same motor. Reference CALD drawings 1031293 and 1030226.

A three pin test group shall be established to aid in factory/field testing.

3.8.3 Printer Module TMS 9940 Diagnostics

Upon command from the mainframe the TMS 9940 shall print a predefined group of characters to demonstrate head driver integrity (barber pole, etc). See Section 4.0 for further discussion. It must also be able to dump its ROM, RAM, and flags out its three pin test port, and do an internal ROM check sum check on command. The results of that test and any others may be tested by the mainframe on its Interrupt Level 8 port. Both the actual check sum and the comparison value supplied by the CPU shall be printed by the printer for visual display. Complete details of this will be worked out at a later date. Table 3.8.1 lists these commands as well as those for normal operation.

3.8.4 Thermal Printer Paper

Paper size will be 4.8" for all 48 characters plus margin dimensions. See CALD Dwg 1500506-4 for complete definition.

3.8.5 Print Head

The print head will be an EPN 3116S type from the EPN 3100 family. CALD Dwg 1018454 gives complete details of the EPN 3116S.

3.8.6 Font

The character font will be based on a 5 X 7 dot matrix.

3.9 Disk Drive Characteristics

3.9.1 Basic Mini Floppy Disk Characteristics

3.9.1.1 Number of Tracks

There shall be 35 tracks/side.

3.9.1.2 Sector Type

The Mini Floppy Disk shall be soft sectored.

3.9.1.3 Sector Size

Soft sectoring shall provide 256 bytes per sector.

3.9.1.4 Transfer Rate

The transfer rate is 250 KHz.

3.9.1.5 Average Access Time

The average access time is 657 ms.

3.9.1.6 Track Life

The Track Life is 3,000,000 "head loaded" passes for each track.

3.9.1.7 Disk Spin Speed

A rotation speed of 300 RPM +/- 5 RPM is provided.

3.9.1.8 Diskette Cartridge Size

The cartridge size is $5\frac{1}{4}$".

3.9.1.9 Power Requirements

+12 VDC +/- 5% @ 1.1A typ, 1.8 max
+5 VDC +/- 5% @ .5A typ, .7A max

3.9.4 Disk DSR Characteristics

Status and instructions are read from and written to the Floppy Disk Controller chip as if he Floppy Disk Controller were memory registers residing on the MSBY of the data bus.

The Floppy Disk Controller will execute all functions necessary for each of the eleven disk commands without system hardware or software intervention. Head stepping, track to track timing, verify operations, CRC generation and detection, serial to parallel, and parallel to serial data conversion are all executed internally to the FDC. Error detection in the form of a cyclic redundency check is the only means of insuring data integrity. After five software initiated retries after an error, the sector data is considered not recoverable; therefore, read after write procedures will improve the disk error rate.

The WD1781 is treated as a memory mapped peripheral with an address as noted in Section 3.1.1.

The DMA controller and data manager transfer data from memory to disk and from disk to memory in a byte mode. Prior to DMAC use the DMA address counter must be loader with the memory buffer start address. The DMAC and data manager must be controlled by the MLB2 CRU port. See Section 3.6.2.2.

The DMA address register resides at hex address F000. Since the transfer of data to or from the Floppy Disk Controller is achieved by DMA, the DMA controller must know at which RAM address to start the transfer. Before executing write track, write sector, read address, or read sector instruction, the DMA counter must be loaded with the buffer starting address. Note that the MSB of the data word is transferred first during the DMA transfers if the DMAC address register is set to an even address.

There are two CRU bits that control the DMA circuitry. The first bit, labelled ENADDR, enables the DMAC and Data Manager circuits to operate. On any operation that requires data transfers, this bit must be set to One. ENADDR is located at hex CRU address 0E00. The second bit is labelled RRDSK, and is located at 0E02 (displaced from 0E00 by 1). For any read operation requiring data transfers, this bit must be set to a One. For write operations, set this bit to Zero. Table 3.9.4.1 is a copy of a section of the Detailed Memory Map found in Section 3.1.1

Data transfers are defined as floppy disk commands that move blocks of data from or to system memory. These Floppy Disk Controller operations are read sector, write sector, read track, write track, and read address commands. Complete Western Digital FD1781 specs are found in Appendix H.

3.9.4 Disk DSR Characteristics (Continued)

ADDRESS	FUNCTION
9000 - 9FFF	Disk Control Address Space
9000	Command Register (write only address)
9002	Track Register (write)
9004	Sector Register (write)
9006	Data Register (write)
9008	Status Register (read only address)
900A	Track Register (read)
900C	Sector Register (read)
900E	Status Register (read)

To access the registers, the Floppy Disk Controller page select CRU bit (@ EOA) must be set to a logical one.

Data loaded into these registers must be located in the most significant byte of the data word that is moved to the hex address location above.

Table 3.9.4.1 Floppy Disk Controller Register Memory Space Definition

There are four registers within the WD1781. They include the Status/Command, Track, Sector, and Data registers. Note that CPU byte data transfered and received from the FDC is located in the most significant byte of the data word. Before accessing the registers, the DISKPG CRU bit (0E0A) must be set to a One. This bit prevents accidental access to the FDC registers. Once the register is accessed, set the DISKPG bit to Zero to safe guard the register contents.

When reading the Status register, one obtains the status of a pending or previous operation. When writing to the Command register, data is assumed to be a command, and its execution begins immediately.

The Track register holds the present track position of the drive being used since the controller can only keep track of one drive head at a time. When selecting Drive 0, the software DSR must store Drive 1's present position and restore Drive 0's position to the Track Register. Before issuing a Seek command, the desired track must be entered into the Floppy Disk Controller. It is not loaded into the Track register, but rather into the Data register. The Floppy Disk Controller then compares the contents of the Data register to the Track register, and steps accordingly.

The Sector register is used only for the purpose of holding the target sector to be read/written. The Sector register must be loaded before loading the command into the Command Register.

The Data register holds the send data for write operations and receive data for read operations.

Tables 3.9.4.2, 3.9.4.3, 3.9.4.4, 3.9.4.5, and 3.9.4.6 define the status bits for the various Floppy Disk Controller commands. In the listings of Status and Command bytes S7 and C7 are the most significant bits. In that the Floppy Disk Controller uses the MSB of the Data Bus, S7 and C7 correspond to the data bit zero (DB0) of the 9900 Data lines; i.e., S7 = D0, S6 = D1,... and S0 = D7.

TYPE	COMMAND	MSB 7	6	5	4	3	2	1	0	REQ'D DATA BYTE TO CHIP
I	RESTORE	0	0	0	0	h	V	r1	r0	0F
I	SEEK	0	0	0	1	h	V	r1	r0	1F
I	STEP	0	0	1	u	h	V	r1	r0	33
I	STEP IN	0	1	0	u	h	V	r1	r0	5F-53
I	STEP OUT	0	1	1	u	h	V	r1	r0	7F-73
II	READ COMMAND	1	0	0	m	b	e	0	0	8C
II	WRITE COMMAND	1	0	1	m	b	e	a1	a0	AC
III	READ ADDRESS	1	1	0	0	0	1	0	0	C4
III	READ TRACK	1	1	1	0	0	1	0	S	E4
III	WRITE TRACK	1	1	1	1	0	1	0	0	F4
IV	FORCE INTERRUPT	1	1	0	1	I3	I2	I1	I0	D8

The parameters h, V, r1, r0, m, b, e, a1, a0, I3, I2, I1, and I0 are defined as variables of the Command bytes.

TABLE 3.9.4.2 COMMAND SUMMARY

3.9.4 Disk DSR Characteristics (Continued)

TYPE I COMMAND SUGGESTED PARAMETERS

h=1	*Head load at the beginning
V=1	*Verify position at final track
r1, r0=11	*40 ms head stepping time
u=1	*TO update the track register

TYPE II COMMAND SUGGESTED PARAMETERS

m=0	*No multiple record operations
b=1	*256 byte format
a1, a0=00	*FB data address mark
e=1	*Enable 75 ms head load time

TYPE III COMMAND SUGGESTED PARAMETERS

s=0	*Sync to address mark

TABLE 3.9.4.3 COMMAND SUGGESTED PARAMETERS

BIT	TYPE I COMMAND
S7 (MSB)	NOT READY WHEN SET TO ONE
S6	WRITE PROTECTED WHEN SET
S5	HEAD ENGAGED WHEN SET
S4	SEEK ERROR WHEN SET
S3	CRC ERROR WHEN SET
S2	AT TRACK 00 WHEN SET
S1	WHEN SET INDEX PULSE WAS ACTIVE
S0	BUSY WHEN SET

FIGURE 3.9.4.4 TYPE I COMMAND STATUS BIT DEFINITIONS

BIT	READ ADDRESS COMMAND	READ COMMAND	READ TRACK COMMAND
S7 (MSB)	NOT READY	NOT READY	NOT READY
S6	0	RECORD TYPE (See Appendix H)	0
S5	0	RECORD TYPE	0
S4	ID NOT FOUND	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	0
S2	LOST DATA	LOST DATA	LOST DATA
S1	DRQ[1]	DRQ[1]	DRQ
S0	BUSY	BUSY	BUSY

Note 1 DRQ is a Data Request signal utilized by the DMAC to receive data from or to send data to the FD 1781 chip. It is invisible to the programmer.

FIGURE 3.9.4.5 READ CLASS COMMAND STATUS BIT DEFINITIONS

BIT	WRITE COMMAND	WRITE TRACK COMMAND
S7 (MSB)	NOT READY	NOT READY
S6	WRITE PROTECT	WRITE PROTECT
S5	WRITE FAULT	WRITE FAULT
S4	RECORD NOT FOUND	0
S3	CRC ERROR	0
S2	LOST DATA	LOST DATA
S1	DRQ	DRQ
S0	BUSY	BUSY

FIGURE 3.9.4.6 WRITE CLASS COMMAND STATUS BIT DEFINITIONS

Commands for the FDC are separated into four categories,and Type I commands are step commands. These commands move the disk head over the surface of the diskette. Type II commands are read and write sector operations. The third type involves track and header commands, while the force interrupt command comprises the fourth category.

The Type I step commands are sub-divided into single step and seek operations. The step, stepin and stepout commands are single step operations. In outlining a step operation, one must first verify that the Floppy Disk Controller is enabled, and that the drive motor is on. One must never step the disk head over the media unless the motor is on for deformation and scratching of the media and/or head may occur which results in ruined media and/or head.

Next, set the DISKPG CRU bit to a one, load the appropriate command into the Floppy Disk Controller, and reset the DISKPG CRU bit. A step pulse will be issued by the Floppy Disk Controller, and forty milliseconds later the Floppy Disk Controller will generate an interrupt to signal command completion. The interrupt is reset by reading the status byte. The 40 milliseconds is derived from the R1,R0 field of the command byte, and is the programmed track to track step time of the minifloppy disk.

The seek type commands are similar except that a destination is desired. The restore command brings the head to the home position, and is used for recalibration. If a seek error is suspected, the restore command may be used. The seek command is used in stepping the head in normal disk operation. Before using verify theFloppy Disk Controller is enabled, and that the motor is on. Set the DISKPG CRU bit to a one, load the desired track into the data register, load the seek command, reset the DISKPG CRU bit, and then wait for the interrrupt. Upon receiving the interrupt, set the DISKPG bit to one, read the status register, and then reset the DISKPG bit. If status bit four (S4) is set to one, the Floppy Disk Controller could not verify that the track reached was the desired track. The procedure at this point is to set up the head once in the previous direction of travel, and then return the head to the unverified track. If the track is still not verified, restore the drives to the home position, and use the seek command once more.

Type two commands consist of read and write sector operations. To outline a Type II write sector operation, the head is assumed to be at the correct track, and the motor is on. First, load the DMA address counters with the sector buffer start address. Next, enable the DMAC (ENADDR) and data flow direction (RRDSK) bits and, set the DISKPG CRU bit to a One. The desired sector must then be written into the sector reister. At this time the command is written into Command Register and the search begins. Then reset the DISKPG bit, and wait for the disk interrupt to signal that the operation has ended. The sector must be found within three revolutions of the diskette, or a "record-not-found" status bit will be set, and the operation will be ended. Once the sector is found, the DRQ line is set to request the first byte (invisible to the Programmer). In turn, the data manager writes the first

byte to the Data Register, and the DRQ line is reset (this is transparent to the programmer). The operation is repeated for each of the 256 data bytes. The FDC then appends two CRC bytes to the data. The operation is now completed, and the INTRQ line is activated to cause a Level 5 interrupt in the CPU. The actual sector search, data transfer, CRC generation, and CRC verifying are transparent to the host system and user.

The Read cycle follows the same logical pattern except that the data flow is in the opposite direction.

In the case that data is not transferred in time during the Floppy Disk Controller to processor transfer, the data lost bit of the Status Register is set and the transfer operation continues. If a Write operation was in progress, a byte of 00 will be written on the Disk in place of the data that didn't get there.

Note that the Floppy Disk Controller has complete control of the head loading. The Floppy Disk Controller will unload the head if no additional command is issued within three diskette revolutions. Head Load time is 75 ms. Any seek, step, read type, or write type command will cause the head to be automatically loaded.

The Type III write track command finds its basic use in the format diskette operation. In order to execute the command, a 3K byte memory buffer is necessary to hold the required track data. The buffer must also hold all gaps, data, and special marks to be written on the diskette. Only the defined format should be followed for workability and compatibility.

Initially the disk motor must be on, and the Floppy Disk Controller must be enabled. Load the DMA address register with the memory buffer starting address, enable the DMA controller by setting ENADDR CRU bit to One, and set the CRU data transfer flow bit RRDSK to Zero. Then set the DISPG CRU bit to one, and load the command byte. Finally, reset the DISKPG bit, and wait for the Level 5 disk interrupt. The FDC will synchoronize to the diskette index pulse, and then write out all address marks and CRC bytes. The data is then transferred in the same manner as the read or write sector commands. Upon receiving the next index pulse, the Floppy Disk Controller will have written a complete track, and will issue a Level 5 interrupt to signal a task completion. A Read Track operation will follow the same procedure as that for a Write Track operation except that the data flow will be in the opposite direction.

The Read Address command will pass the six bytes of the address mark via the DMAC to system RAM. The six bytes include, track number, sector number, and two CRC bytes. This command is executed utilizing the same procedure as for the Read Track command. Note that only six bytes are transferred instead of the 3K byte track contents, and that the DMAC address register still must be set up.

The Force Interrupt command and its four forms make up the Type IV commands. Only two of the four forms will be discussed here. The first is the force interrupt immediately command. When parameter I3 is set to a one, and all other parameters to zero, the command will cause the Floppy Disk Controller to abort the present operation, and issue an interrupt. This command is useful in terminating any operation prematurely or for Floppy Disk Controller testing. The second form is the "force interrupt on index pulse" command. Setting parameter I2 to a one, and all other parameters to zero will cause an interrupt to be generated on the next index pulse.

In verifying that the disk motor is up to speed, one may use the "force interrupt on index pulse" command. Two of these interrupts will be required. On the first interrupt, an event counter must be loaded with a 200 ms count. Next, issue another force interrupt on index pulse. If the disk interrupt occurs at a nominal time bracketing the 200 ms period (+/- 5%), the disk motor is running and rotating at the proper speed.

Special disk operations and characteristics are discussed next. On system Power-Up, one must insure that both drives are at the home position. Therefore, execute the Restore Drive command once for each disk drive.

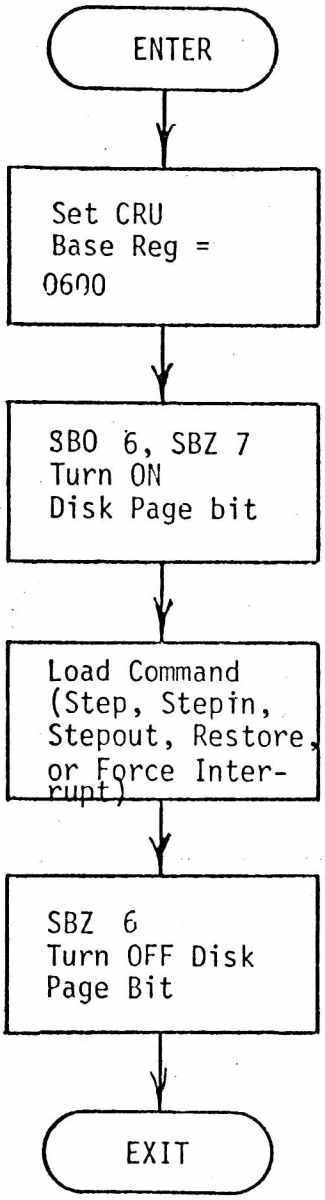
When turning a drive motor on, wait two seconds before executing any read or write command to allow the diskette to come up to the proper speed.

When using the FDC, the chip should be enabled at all times. Even though the motor undergoes a duty cycle, the chip should normally not be reset (the CRU bit 0E0C must normally be a One).

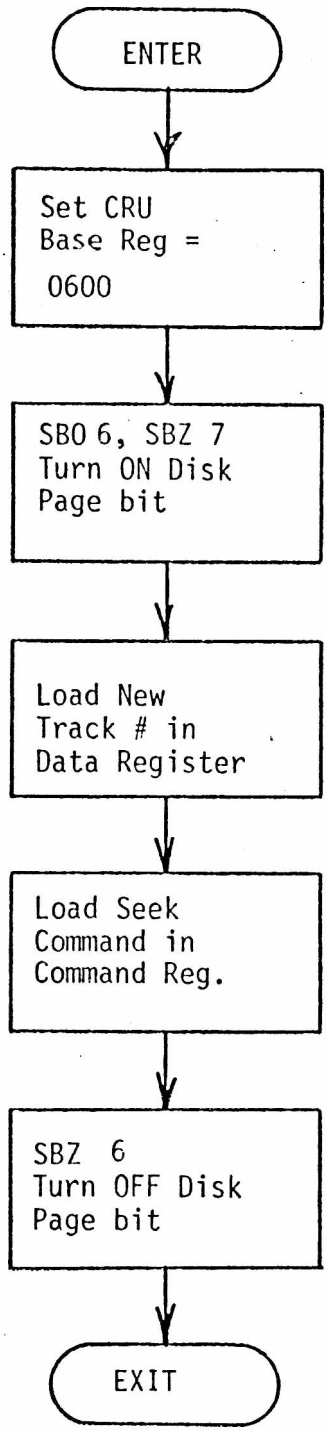
The disk drive motors and side select lines are independently operable even though only one CRU bit exists for both drives. In order to turn Drive 0 motor on, set the DISK0/1 CRU Bit to a Zero. Next, set the motor on CRU bit (0E10) to a One to turn on the motor. The drive 0 motor will stay on until reset by once again selecting Drive 0 (set CRU bit at 0E08 to Zero) and then setting the Motor On bit at 0E10 to Zero.

Although the FD 1781 controlls the head loading, it does not comprehend head settling time. "Head settle" is the time required for the disk head to stabilize at a track after a stepping operation. Track to track step time is 40 ms per track, and is comprehended by the Floppy Disk Controller. Once the head reaches the desired track an additional 10 ms is necessary for the head to come to rest. Head settle time therefore becomes a software responsibility.

Floppy disks do not have a separate erase pass before executing a write. Once the disk is formatted, only one pass is needed to accomplish a modification.



(A)



(B)

Figure 3.9.4.7 Basic Flow Chart of Issuing Types I and IV Commands

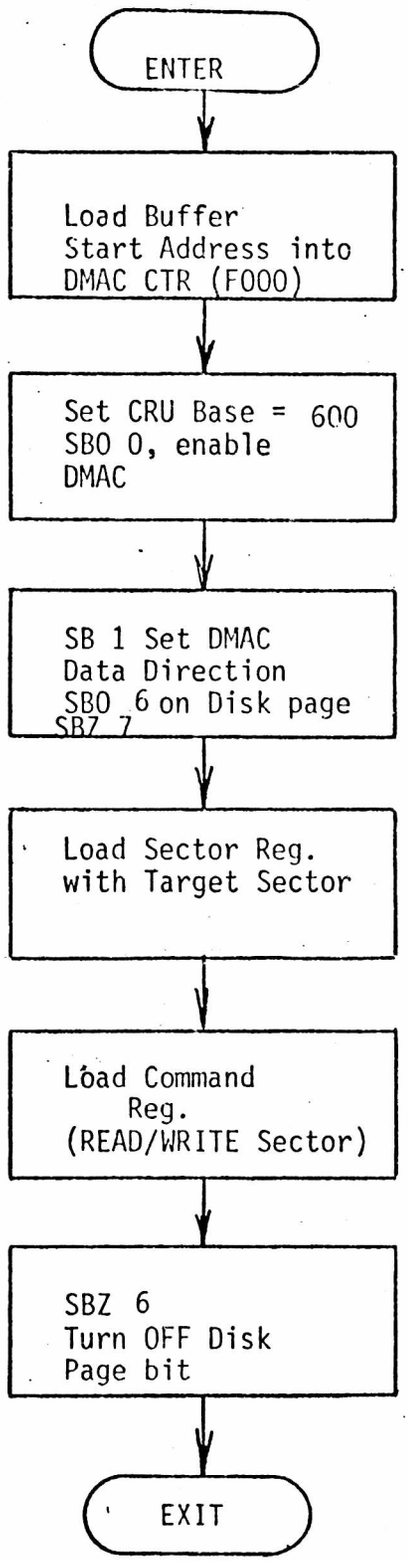


Figure 3.9.4.8 Basic Flow Chart of Issuing Type II Commands.

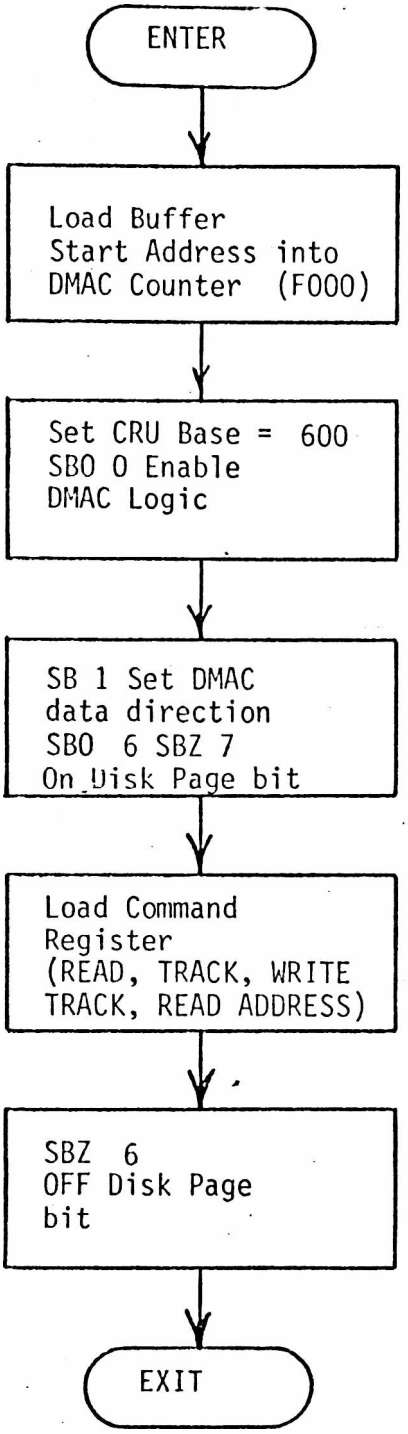


Figure 3.9.4.9 Basic Flow Chart on Initiating a Type III Command

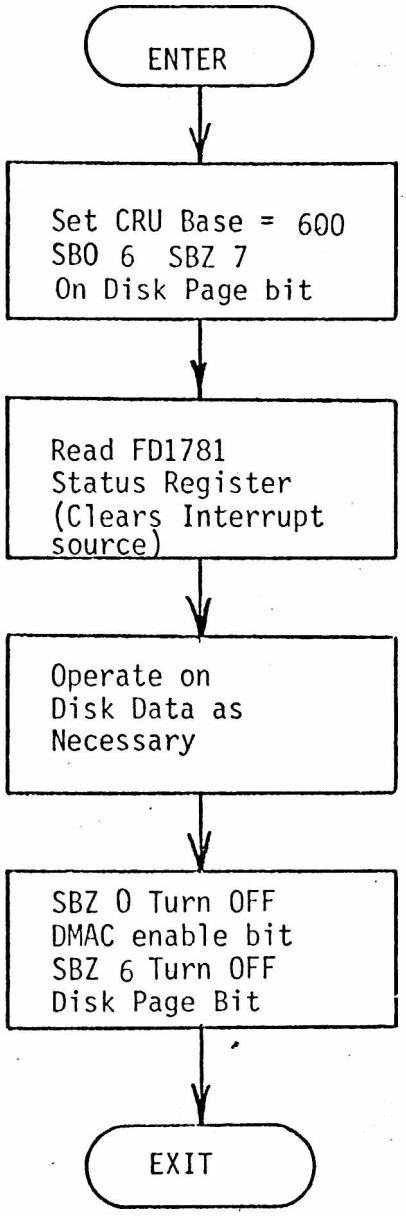


Figure 3.9.4.10 Basic Flow Chart of Disk Interrupt Service

3.10 Power Supply

The power supply must supply six output voltages at an output power of 160 watts, and occupy a reasonably small area inside the SR-70. All of the output voltages track off of the +5 V output.

3.10.1 Input

3.10.1.1 Unites States (Model 1)

120/127 VAC +/- 15%
47 - 63 Hz
UL, CSA Approved

3.10.1.2 Foreign, Model 2

220/240 VAC +/- 15%
47 - 63 Hz
VDE Approved

3.10.1.3 Foreign, Model 3 (To Be Considered)

100/200/250 VAC
47 - 63 Hz

3.10.2 Output

	Nominal Voltage	Regulation	Max Current	Max Power
1	+5V[1]	+6% - 3%	6.75A	33.5
2	-5V	+6% - 3%	.45A	2.25
3	+12V	+6% - 3%	3.2 A	38.4
4	-12V	+6% - 3%	.033A	.4
5	+20V[2]	+10%	3.33A RMS[3]	66.0
6	+15V[4]	+/- .2V	1.3 A	19.5

Notes:
1. Feedback sense voltage
2. The load current will be removed externally by PWRSTAB = 0.
3. This current - when not zero - follows a duty cycle of 10A for 1ms, 3.3A for 4 ms, and zero for the next 5 ms. The cycle then repeats.
4. TV monitor voltage is independently short circuit protected.

Output voltages are collectively adjustable by a single multi-turn potentiometer to provide a +/- 10% range.

3.10.3 Ripple and Spikes

Less than 100 mV pk-pk on outputs 1-4; output 5 is 5% pk-pk max; and for output 6 100 mV pk-pk max synchronous with primary power and 10 mV pk-pk max asynchronous with primary power.

3.10.4 Load Regulation

The regulation of the output voltages in section 3.10.2 shall be met when all combinations of outputs 1 thru 4 and 6 are varied-20% from maximum except for output #5 which shall be varied by 100% at the duty cycle described by Note 3, Section 3.10.2. Line regulation, ripple and spikes, load transient response, turn on/off overshoot, and line regulation for outputs 1 thru 6 must be included with load regulation to meet the regulation of section 3.10.2. Regulation for output 6 does does not include ripple and spikes.

3.10.5 Temperature Rating

0 Deg C to +70 Deg C Ambient. Conduction and forced air cooling at four cubic feet per second. Derate upper limit 1 Deg C per 1000 feet above 6000 feet altitude.

3.10.6 Storage Temperature

-20 Deg C to +85 Deg C

3.10.7 Temperature Coefficients of Outputs

+5V is .03%/Dec C
All others are .06%/Deg C

3.10.8 Humidity

Non-condensing 0% to 85% @ 35 Deg C.

3.10.9 Altitude

12,000 Ft. (max) Operating
50,000 Ft. (max) Non-operating

3.10.10 AC Inrush Current

Inrush current shall be limited by series power thermistors or other means such that parts are not stressed beyond published safe operating limits.

3.10.11 Efficiency

The efficiency shall be greater than or equal to 65%.

3.10.12 Switching Frequency

The switching frequency shall be a nominal 20 KHz, but not audible.

3.10.13 Hold-up

With all outputs fully loaded, regulation shall be maintained on outputs 1 thru 3 for 28 ms from 115 VAC -10% (104 VAC) on Model 1 or 220 VAC -15% (187 VAC) on Model 2. This allows a one cycle (50 Hz) ride thru and a PWRSTAB signal 1 ms prior to loss of regulation on outputs 1 thru 3. See Figure 3.10.20.

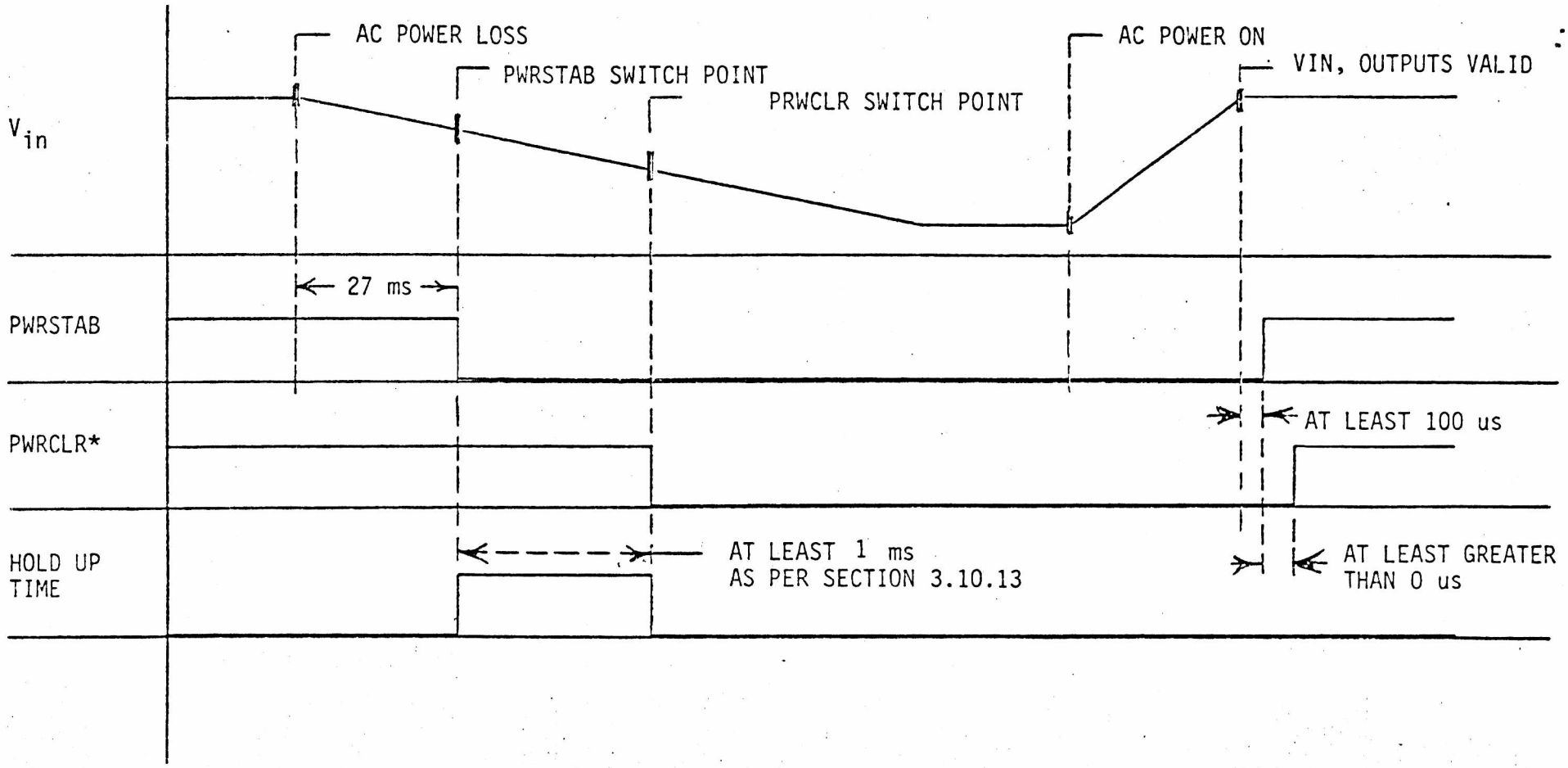


FIGURE 3.10.20 POWER SUPPLY POWER OFF/ON CHARACTERISTICS

3.10.14 Power Sequencing

The -5V output shall come on before, or less than 400 ms after, the +12V power comes up, and should never be more positive than signal ground when the +12V is powered up. During power down the +12V output must drop to 60% of its value before, or no greater than 400ms after the -5V output decays to 0 V.

3.10.15 Protection

Short circuit/overload protection shall be provided on all outputs to insure that published component safe operating limits are not exceeded during continuous overload or short circuit condition. Also to be provided are reverse-polarity protection (-1.0V, max), lightning transient protection, and RFI filtering (Model 2 only).

3.10.15.1 Over-voltage Protection

Vo	OVP Limits
+/-5V	7.0V max
+/-12V	15.0V max
+20V	28.0V max
+15V	20.0V max

3.10.16 EMI-RFI

MIL461A, BS800 Part 3, VDE 0875 Curve N as applicable for Model 2.

3.10.17 Isolation

3.10.17.1 United States (Model 1)

Must meet the UL and CSA requirements for office and business equipment (UL 748/CSA).

3.10.17.2 Foreign Model 2

Must meet the VDE requirements for office and business equipment (VDE 0730).

3.10.17.3 Foreign Model 3

Requirements not determined.

3.10.18 Testability

Test points shall be provided for all voltages, and will be accessible when the power supply is installed in the chassis. (Design Goal)

3.10.19 Power Stable Output

This open collector/drain output must go low when the line voltage goes lower than the limit specified in Section 3.10.1, and at least 1 ms prior to loss of regulated power on Outputs 1 thru 4. See Section 3.10.13. During power up PWRSTAB must remain low for at least 100 us after regulated power has been restored. Figure 3.10.20 shows the time/phase relationships of power down/up sense signals.

3.10.19 Power Stable Output (Continued)

The On voltage of the PWRSTAB open collector/drain signal must lie between OV (min.) and +.3V (max.) with a 5 ma sink current.

3.10.20 Power On Clear

The PWRCLR* output must go Low (.3V max, OV min) when any output from 1 thru 3 goes out of regulation, and must go to its high impedance state after PWRSTAB has gone high. The electrical characteristics are identical to those of PWRSTAB in Section 3.10.19, and a time/phase diagram involving PWRCLR* and others is shown in Figure 3.10.20.

3.10.21 Mean Time Between Failure

With nominal input voltage and an ambient temperature of 40 Deg C, the MTBF must be greater than or equal to 25,000 Hrs. as calculated by MIL-HDBK 217B.

3.10.22 PWB Marking

Shall have parts legend denoted on PWB.

3.10.23 Weight

Approximately 4 pounds.

3.10.24 Construction

Open frame may be used unless closed frame is required for RFI, EMI, approvals.

3.10.25 Certification As Office Equipment

3.10.25.1 United States (Model 1)

UL, CSA (Office Equipment)

3.10.25.2 Foreign Model 2

VDE (Office Equipment)

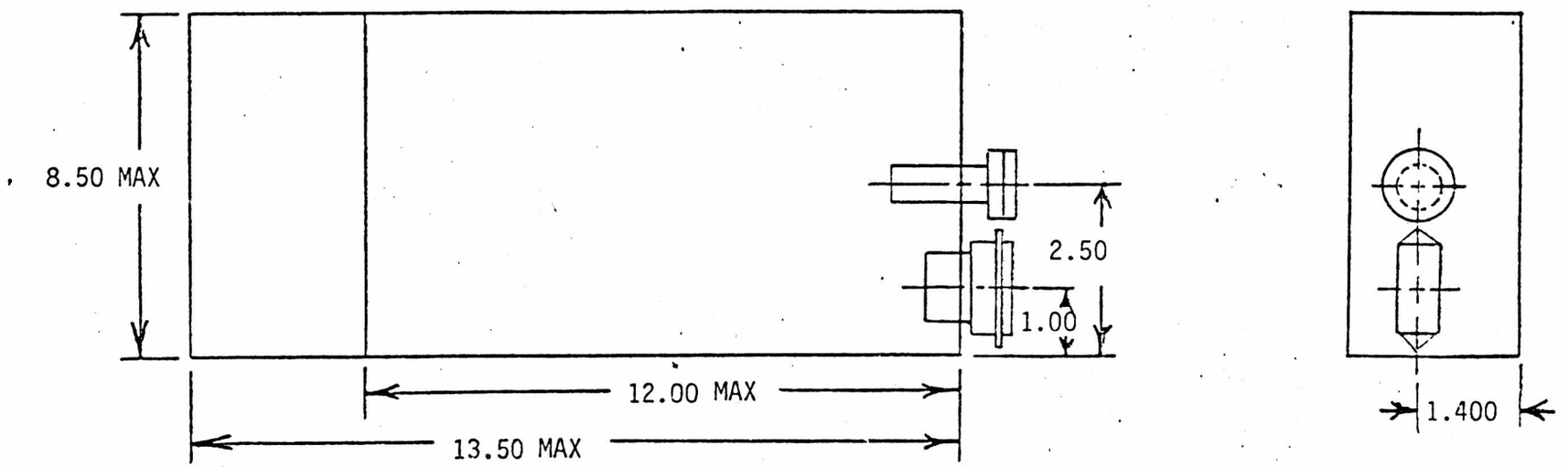
3.10.25.3 Foreign Model 3

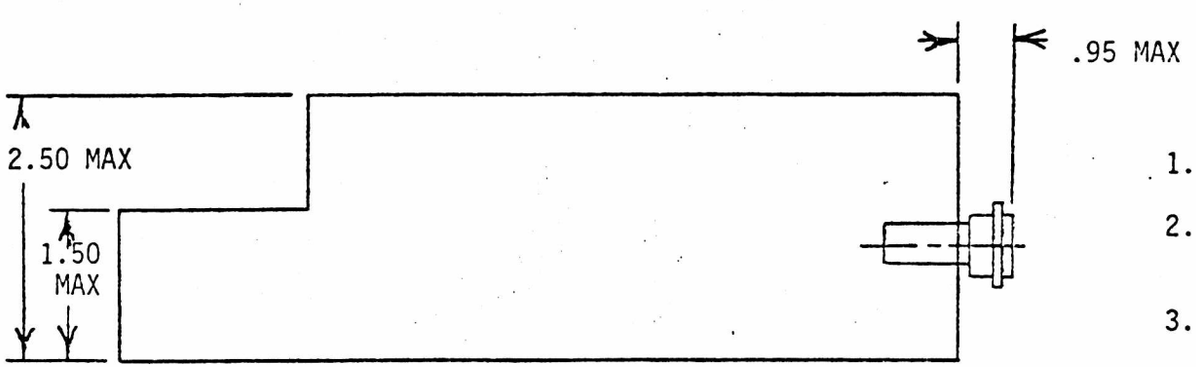
Not determined

3.10.26 Dimensions (max)

13.5" X 8.5" X 2.5". See Figure 3.10.26.

3.10.27 Environmental Testing (Vibration, Shock)





NOTES

1. MTG HOLES TO BE DETERMINED LATER
2. UNIT IS CONDUCTION COOLED THRU BOTTOM MOUNTING
3. FUSE HOLDER TO BE LITTLEFUSE 3AG SHOCK SAFE TYPE OR EQUIV.
4. INPUT POWER CORD RECEPTICAL TO BE AMP DATA SHEET 76-370 OR EQUIV.
5. OUTPUT CONNECTOR TYPE AND LOCATION NOT DETERMINED

FIGURE 3.10.26 CASE DIMENSIONS

3.10.27.1 Vibration In Shipping Container

Unit shall pass tests set out in MIL-STD-810B, Method 514.1, Procedure X per paragraph 4.5.1.3, cycling test using curve AY of Figure 5.14.1-VII, and time schedule Table 5.4.1-VII. Omit resonance search and Dwell. Test in three perpendicular planes from 5-200-5 Hz for one hour each time.

3.10.27.2 Bounce, Loose Cargo-In Shipping Container

Unit shall pass tests set out in MIL-STD-810B, Method 514.1, Procedure XI, Paragraphs 4.16.2, 4.16.2.3, and 4.16.2.4 except limit to .1 inch double amplitude sinusoidal vibration and 10 Hz.

3.10.27.3 Transient Drop Test - In Shipping Container

Unit shall pass tests set out in EIA-PEP-2. The packaged power supply shall be dropped from a height of four feet onto a concrete floor as follows: one flat drop on an end, a side, and the bottom, one corner drop on the bottom corner common to the end side used on the FLAT DROP Test; and one edge drop on the bottom edges of the same side and end previously used.

3.10.27.4 Mechanical Shock-Bench Handling

Unit shall pass the tests set out as follows: place the unpackaged power supply on a standard bench top surface; raise the front edge of the power supply six inches off the bench top surface, and allow the power supply to drop. Repeat the sequence for the back edge. Verify that the power supply will properly function after each drop.

3.11 Internal Connection Plan

Internal connections to the various SR-70 subassemblies shall be done in such a manner to provide both quick disconnect and reliable connections. The cables will be as short as practical.

3.11.1 Mechanical Concept

Mainframe to disks, printer, and keyboard will be via ribbon cable from the I/O back plane to the peripheral involved. Exact details will be determined later.

3.11.2 Connector Pin Definitions

3.11.2.1 Keyboard

To be determined later.

3.11.2.2 Thermal Printer

To be determined later.

3.11.2.3 Power Supply

To be determined later.

3.11.2.4 MFM Disk Drives

There will be unique cable for each disk drive (star connection). The pin outs for each disk are identical and listed in Table 3.11.2.4.

PIN #	Function
1 thru 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 34	Logic Ground
8	Index/Sector*
10	Drive select - 1*
16	Motor ON*
18	Direct Select*
20	Step*
22	Write Data*
24	Write Gate*
26	Track 00* indicator
28	Write Protect*
30	Read Data
32	Side Select

3.11.3 Power Distribution

All +/-5, +12, and Ground will be fed from the power supply to the Main Frame I/O backplane. Other peripherals will be fed these voltages from this point to shorten ground return paths. Exact details of this will be worked out later.

3.12 Outside World Interface

There shall be five basic connections from the SR-70 to external functions. Only two are required for SR-70 operation - the AC line cord, and the Monitor cable.

3.12.1 RS-232-C Port Definition

The RS-232-C Port shall interface directly to either a TI 810 Printer, TI 820 printer, or a Silent 700 Series with no special cables. This implies that the SR-70 will provide a female 25 pin "D" connector for RS-232-C connection. Table 3.12.1 gives pin definitions for the RS-232-C port. Figure 3.6.3.4 is a basic flow chart of the TMS 9902 DSR. The RS-232-C port shall function as a Data Set, and software will be written to service this port.

3.12.2 CRU Port Definition

The CRU Port provides the user with expansion capabilities, and it is the user's responsibility to program the SR-70 to comprehend any functions connected to it. Since one of the five interrupts capable of originating from the CRU port has a higher priority than some of the SR-70 internal peripherals (see Section 3.3), and since the user can lock out an interrupt from these lower levels, there can be no guarantee that the SR-70 will run according to specifications when the user programs this port. Appropriate guide lines in the software section will direct the user in the use of the CRU port.

The CRU port shall be designed to support at the end of an 8 foot long cable TMS 9900 series parts that will cycle at 400 ns or faster. 74LS series Line Drivers shall drive all lines leaving the SR-70 CRU port, and all lines received by this port shall be terminated with an impedance of not less than 290 ohms.

Signals comprehended by the CRU port are outlined in Section 3.6.3.3, and Table 3.12.2 provides the CRU Port pin definitions.

The least significant 4 address bits, the 3 bit CRU bus, System Reset, Phase 3 clock, and the Port CRU space select bit shall individually be guarded by Logic Ground when connected to a flat ribbon cable.

The connector shall be a 37 pin female "D" type.

3.12.3 Monitor Port Definition

The Monitor Port provides a path from the SR-70 to the monitor for both power and the three signals described in Section 3.6.3.2.1. The Monitor power requirements are defined in Section 3.10.

The connector type will be a 9 pin remale "D" connector, and Table 3.12.3 details the pin assignments.

Table 3.12.1 RS-232-C Port Pin definitions

PIN #	Function
1	Protective Ground (jumpered with pin 7 on MLB3 RS-232-C connector)
2	Transmit Data-Transmit data stream from the RS-232-C port to the TMS 9902
3	Receive Data-data stream from the TMS 9902 to the RS-232-C port
4	Request to Send-tied to the +12 thru a 4.7K resistor
5	Clear to Send-tied to +12 thru a 4.7K resistor
6	Data Set Ready-tied to +12 thru a 4.7K resistor
7	Signal Ground tied to Logic Ground on MLB3 (pin 1 also jumpers to this pin)
8	Data Carrier Detect-derived from the TMS 9902 CTS*-RTS* connection point.
11	Assigned to be 810 Printer Busy. Sensed at 0040. High indicates the printer is BUSY, and Low indicates the printer is READY. Notice that this violates the RS-232-C definition for control signals.
20	Data Terminal Ready - Sensed at the TMS 9902 "DSR*" location (See Section 3.2.1 for TMS 9902 access).

NOTE: Any signal received on the CRU Input Register located on the 0040 base cannot cause an interrupt.

Table 3.12.2 CRU Port Pin Definition

Pin #	Function
1 thru 5	Logic Ground
6	System Address Bus bit 9, hi true
7	System Address Bus bit 7, hi true
8	System Address Bus bit 5, hi true
9 thru 17	Logic Ground
18	Interrupt I4 (CPU Level 12), lo true
19	Logic Ground
20	System Address Bus bit 14, hi true
21	System Address Bus bit 13, hi true
22	System Address Bus bit 12, hi true
23	System Address Bus bit 11, hi true
24	System Address Bus bit 10, hi true
25	System Address Bus bit 8, hi true
26	System Address Bus bit 6, hi true
27	System Address Bus bit 4, hi true
28	CRUIN Cru input data to CPU, hi true
29	CRUOUT CRU output data from CPU, hi true
30	CRUCLK CRU clock from CPU, hi true
31	System Reset, lo true
32	System Phase 3, lo true
33	Port space select, lo true
34	Interrupt I1 (CPU Level 6), lo true
35	Interrupt I2 (CPU Level 10), lo true
36	Interrupt I3 (CPU Level 1), lo true
37	Interrupt I5 (CPU Level 13), lo true

Pin numbers are for a 37 pin "D" connector

Table 3.12.3 Monitor Port Pin Definitions

PIN #	Function
1,2,3	Power/Signal Ground
4,5,9	+15 Power
6	Video
7	Vertical Drive
8	Horzontal Drive

Table 3.12.4 GPIB Pin Definitions

Pin #	Function
1	DIO 1 Data Line #1
2	DIO 2 Data Line #2
3	DIO 3 Data Line #3
4	DIO 4 Data Line #4
5	EIO Control Line
6	DAV Control Line
7	NRFD Control Line
8	NDAC Control Line
9	IFC Control Line
10	SRQ Control Line
11	ATN Control Line
12	Shield
13	DIO 5 Data Line #5
14	DIO 6 Data Line #6
15	DIO 7 Data Line #7
16	DIO 8 Data Line #8
17	REN Control Line
18	Ground Return for Pin 6
19	Ground Return for Pin 7
20	Ground Return for Pin 8
21	Ground Return for Pin 9
22	Ground Return for Pin 10
23	Ground Return for Pin 11
24	Logic Ground

The 24 pin connector shall be Amphenol or Cinch Series 57 or AMP "Champ" series.

3.12.4 GPIB Interface Option

The IEEE bus option will utilize the TMS9914 chip with suitable buffers on either side to interface to the system and to the outside world bus. It will probably be in the best interest of the system to receive the outside world bus on MLB2, and to interface data to the 8 bit DMAC bus. This would prohibit concurrent operation with the disks unless additional Data Bus isolationis provided. Table 3.12.4 gives I/O pin definitions. Complete details will be worked out at a later date.

3.12.5 AC Power

The male AC power receptical, the AC power switch, and the AC power fuse shall be hardwired to the power supply assembly, and shall easily attached to the case with screws, etc.

3.13 Monitor Characteristics

The SR-70 monitor shall have the following characteristics:

- accept TTL Level Horizontal drive,
- accept TTL Level Vertical drive,
- accept TTL Level Video,
- 12" screen
- use P-31 green phosphor
- function on +15V DC power (See Section 3.10 for ripple defunction) with a maximum current of 1.5A,
- equal to or greater than 10 MHz bandwidth,
- provide internal, adjustable controls for horizontal width, vertical height, linearity and brightness,
- provide an external contrast control, and
- have a MTBF (less picture tube) of equal to or greater than 10,000 hours.

4.0 System Level Diagnostics

The SR-70 will support three levels of diagnostics. The first two levels will be slanted towards system integrity verification rather than to provide insight into what may be wrong with a given block. The third level is of sufficient depth to provide adequate information to service personnel for their use. An ongoing effort will add other useful tests as they become apparent.

4.1 User Oriented Diagnostics

The first level of diagnostics will be used as a system wide performance assurance test similar to the Performance Demonstration Test (PDT) supplied with DSG products. The intent of these tests will be to assure the user of the integrity of all parts of the system. The total elapsed time for the test should be less than five minutes. The manual containing instructions for running this test will also include a checklist of user correctable subsystem malfunctions (out of paper, unplugged, etc.). The main design criteria for this level will be ease of use for the unsophisticated computer user. The tests will require little, if any, operator intervention while exercising each subsystem, and provide a visual indication of its workability. This diagnostic shall be stored in the BROM for immediate availability.

A second level of diagnostics will perform a more comprehensive test of selected subsystems, and will allow the user to further isolate problems on the more sophisticated peripheral devices. This level will require assistance from the user through simple question and answer dialogs. At present the disk subsystem seems to be the only one requiring a second level of diagnostic sophistication. As potential problem areas are identified for the various subassemblies, other devices and subassemblies may require Level 2 diagnostics also. These programs shall be stored in the BROM, and will be invoked from the same program as the Level 1 diagnostics.

4.2 Power Up Diagnostics

When coming up from the RESET mode (Power Up or Software Reset) a simple, short diagnostic will be run to verify mainframe integrity. This includes a DRAM test, a ROM checksum test, and a CRU echo test by controlling the output bit at 606 and sensing the result at 0048. The thermal printer will be the destination of any messages.

4.3 Maintenance Diagnostics

The Level 3 diagnostics exist for use by trained service personnel. They will use the first and second levels of diagnostics as a foundation, but with additional, more rigorous features. They will provide for repetitive exercising of subsystems or subsystem elements to facilitate isolation of dynamic problems. The creation of these diagnostics will require close cooperation between the hardware designer involved and the diagnostic programmer. Since one of the more important challenges of the SR-70 project will be to produce a system that can be easily repaired, a review of the repair diagnostics should be planned 3 to 6 months after delivery of the first units. An ongoing effort involving Engineering, Production, Field Service, and the user is mandatory.

4.4 Diagnostic Functional Requirements

4.4.1 Level 1 Diagnostics

List system version and revision date. Report system resources. Perform CPU and Memory test. Exercise peripheral devices: Barber pole on printer(s) and monitor, Scroll monitor, Write, seek, and read both disks, Request and display keyboard input. Report missing disks, overdue interrupts, etc.

4.4.2 Level 2 Diagnostics

Disk performance test. Verify a user diskette (read only). Verify disk drive functionality. Initialize a diskette. Sequential write-read check. Random write-read check.

4.4.3 Level 3 Diagnostics

4.4.3.1 All Subsystems

Iterative testing (dynamic problems). Output fixed and user supplied patterns. Move data into external buffers (if applicable). Get data from external buffers (monitor). Selected portions of general diagnostics.

4.4.3.2 CPU

Execute each instruction form. Test ALU.

4.4.3.3 Memory

Exhaustive general memory test. Test for memory loss after extended time period. Identify bad chips with pattern tests.

4.4.3.4 Thermal Printer

Print barber pole and single character rows. Diagnostic programmes inside TMS 9940 will be an option if TMS 9940 ROM space exist.

4:4.3.5 Monitor

Initialize TV chip (SMC CRT5027)and blank the screen. Output barber pole pattern. Read contents of external buffer. Scroll monitor at both slow and fast rate.

4.4.3.6 Keyboard

Echo input characters on monitor. Request specific characters. Request all characters in a specific order.

4.4.3.7 RS-232-C Port

Black box. Output characters. Check for interrupt. Read characters. Perform TMS 9902 test with self test mode in the TMS 9902.

4.4.3.8 CRU Port

Black box. Output data. Check for interrupt. Read data.

4.4.3.9 Outboard Devices

Support 820 printer only. Built-in diagnostic. Similar to thermal printer.

4.4.3.10 Disks

Dumps as requested via the keyboard to the monitor will be utilized to observe various data patterns from the disk in question.

5.0 Software Characteristics

See SR-70 Operating System Specification (not released).

6.0 Electrical Test Plan

The basic test plan for the SR-70 is conceived to insure a producible product; therefore, it must comprehend all phases of the production cycle. The same emphesis is put on field service.

6.1 Component Level Testing

All components which do not have proven reliability records will be 100% tested prior to their populating an SR-70 subassembly. This includes an "Etch Test" of each bare PCB. Table 6.1 lists the known devices that will require 100% prescreening.

6.2 PWB Testing

A finished PWB will be given a functional test by an "In-House" designed test system. If good manufacturing practices are utilized a larger than 80% yield will be experienced; therefore, tieing up an expensive Fault Isolation system to pass these boards is not economical. This functional tester will be designed around the SC Division's "EVM" TMS9900 based system, and can easily produce a data base that may be utilized for line yields, etc. (Management Systems use).

6.3 Power Supply

Each power supply will be tested over its input voltage range with the output loading such that it resembles the actual mainframe/peripheral load. This includes a simulated (or actual) thermal printer load.

6.4 Disk Drives

Disk drives whether they be Mini Floppy DIsks or ADD's will be 100% functionally tested prior to their being installed on the SR-70 by a thorough READ/WRITE exercise operation. The same program to do this may be modified to fit the final system level verification test, and used there.

6.5 Keyboard

The keyboard will pass the "standard rake" test. It will be desirable to have Test Equipment build a solenoid/plunger test system for future use as time/loading permits.

6.6 Thermal Printer

The printer will be tested only by a character dump to all 48 columns such that all elements are exercised. The results of this test must be "eyeballed" by the operator; so a format must be chosen to facilitate this.

6.7 Internal Peripheral/Mainframe Cables

All cables will be continuity tested prior to their being installed on an SR-70. The PCB etch test system could easily be fixture adapted to do this.

Table 6.1 Devices Which Require 100% Preassembly Testing

ITEM	#/SR-70	DESCRIPTION
TMS 9900	1	Microprocessor
TMS 9901	1	Programmable Systems Interface
TMS 9902	1	Asynchronous Communication Controller
SN74LS362/TIM9904	1	Four Phase CLock Generator
TMS 4116-25	16	16K X 1 Dynamic RAM
CRT 5027	1	SMC TV Controller Chip
TMS 9940	1	Microcomputer
ULN2003A	8	Darlington Transistor Arrays
TMS 40L45-45	4	1K X 4 Static RAM
TMC 0350	32	BROMS

6.8 Monitor

The incoming TV monitor must be checked similar to the printer mainly for full screen coverage since MLB3 furnishes the characters for display.

6.9 System Level (Burn In Also)

The system level test will be comprehensive enough to insure that the system leaving the test station (Burn In Rack) will perform to its advertised specification. The SR-70 under test will be connected back to an "EVM" custom built monitor (something like that described in Section 6.2) that feeds data to the SR-70, and then checks the return data against a known set. Each monitor could quite will service up to 32 SR-70's on a time sliced basis. The complete details will be worked out later. Notice that here also the terminal printer and the video display must be "eye ball" checked.

7.0 Environmental

The SR-70 will operate under the environmental conditions described in CALD Specification 1500001.

7.1 Temperature

a)	Operating:	0 Deg C to 45 Deg C
b)	Storage:	-40 Deg C to 70 Deg C
c)	Shock	Unit operates in a 25^{0}C 50% R.H. environment within 30 minutes after being stored for two hours at -30 Deg C C at 50% R.H. must must be dry throughout.

7.2 Humidity

a)	Operating:	85% at 35 Deg C
b)	Storage:	95% at 53 Deg C

7.3 Shock

Drop from 10 inch height on all four sides and bottom.

7.4 Vibration

One hour of 5-200-5Hz at 0.8g maximum in each of 3 perpendicular planes.

7.5 Safety

The SR-70 will meet or exceed the consumer safety requirements described in 1500001 and applicable portions of UL478. In addition, the safety requirements of VDE 08680H (Germany) will be a design goal.

7.6 Noise

The principal noise sources in the SR-70 will be the fan and the printer. The total nosie emission of these will be maximum of 65 DBA.

8.0 Reliability

The SR-70 will have a MTBF goal of 8700 hours based on a 33% overall duty cycle (8/24 hours) and a 50% operating duty cycle of the ADD drives and the thermal printer. Selection and screening of the ciritical MOS parts, combined with burn-in at the system levels, will be utilized to achieve this goal.

9.0 Maintainability

The software diagnostics are key to user maintainability and failure verification. The diagnostics are discussed in Section 4.0.

The SR-70 upper case will be removed by removing four screws, thus exposing all subassemblies and test points for test equipment access. Changeout of modules will be facilitated by use of connectors rather than soldered joints. The four large circuit boards are removed by toggle levers on zero insertion force connectors.

A filter is located outboard of the fan to reduce the probability of contamination reaching the ADD drive head-survace interface. This filter will be replaceable by the user.

APPENDIX D

System Backplane Pin Definition

Pin #	Definition	MLB1	MLB2	MLB3	MLB4
1	Logic Ground	I	I	I	I
2	Logic Ground	I	I	I	I
3	Logic Ground	I	I	I	I
4	Logic Ground	I	I	I	I
5	Logic Ground	I	I	I	I
6	Logic Ground	I	I	I	I
7	System Data Bus, Bit 15 Hi True	T	T	T	T
8	System Data Bus, Bit 07 "	T	T	T	T
9	System Data Bus, Bit 14 "	T	T	T	T
10	System Data Bus, Bit 06 "	T	T	T	T
11	System Data Bus, Bit 13 "	T	T	T	T
12	System Data Bus, Bit 05 "	T	T	T	T
13	System Data Bus, Bit 12 "	T	T	T	T
14	System Data Bus, Bit 04 "	T	T	T	T
15	System Data Bus, Bit 11 "	T	T	T	T
16	System Data Bus, Bit 03 "	T	T	T	T
17	System Data Bus, Bit 10 "	T	T	T	T
18	System Data Bus, Bit 02 "	T	T	T	T
19	System Data Bus, Bit 09 "	T	T	T	T
20	System Data Bus, Bit 01 "	T	T	T	T
21	System Data Bus, Bit 08 "	T	T	T	T
22	System Data Bus, Bit 00 "	T	T	T	T
23	Guard Ground	NU	NU	NU	NU
24	Guard Ground	NU	NU	NU	NU
25	SPH1* Low True 3MHz System Clock	O	I	I	NU
26	SPH1* Low True 3MHz System Clock	O	I	I	NU
27	SPH2* Low True 3MHz System Clock	O	I	NU	NU
28	SPH2* Low True 3MHz System Clock	O	I	NU	NU
29	Guard Ground	NU	NU	NU	NU
30	Guard Ground	NU	NU	NU	NU
31	TVCLK 12MHz System Clock	O	I	NU	NU
32	TVCLK 12MHz System CLock	O	I	NU	NU
33	Guard Ground	NU	NU	NU	NU
34	Guarad Ground	NU	NU	NU	NU
35	SPH3* Low True 3MHz System Clock	O	I	NU	NU
36	SPH3* Low True 3MHz System Clock	O	I	NU	NU
37	SPH4* Low True 3MHz System Clock	O	I	NU	NU
38	SPH4* Low True 3MHz System Clock	O	I	NU	NU
39	Guard Ground	NU	NU	NU	NU
40	Guard Ground	NU	NU	NU	NU
41	System Address Bus AB08 Hi True	T	T	T	T
42	System Address Bus AB07 "	T	T	T	T
43	System Address Bus AB09 "	T	T	T	T
44	System Address Bus AB06 "	T	T	T	T
45	System Address Bus AB10 "	T	T	T	T
46	System Address Bus AB05 "	T	T	T	T
47	System Address Bus AB11 "	T	T	T	T
48	System Address Bus AB04 "	T	T	T	T
49	System Address Bus AB12 "	T	T	T	T
50	System Address Bus AB03 "	T	T	T	T

APPENDIX D

System Backplane Pin Definition

Pin #	Definition		MLB1	MLB2	MLB3	MLB4
51	System Address Bus AB13 Hi True		T	T	I	I
52	System Address Bus AB02 "		T	T	I	I
53	System Address Bus AB14 "		T	T	I	I
54	System Address Bus AB01 "		T	T	I	I
55	Write Cycle Enable WE* Lo True		T	T	NU	NU
56	System Address Bus AB00 Hi True		T	T	I	I
57	Guard Ground		NU	NU	NU	NU
58	Guard Ground		NU	NU	NU	NU
59	Data Bus Direction Hi = Read	DBIN	T	T	I	I
60	CRU Address Space Detect Hi True	CRUEN	S	I	I	NU
61	CPU Hold Acknowledge Hi True	HOLDA	S	I	NU	NU
62	CPU Hold Request Lo True	HOLD*	I	S	NU	NU
63	Interrupt Level 4, SPARE, Lo True		I	NU	NU	NU
64	CRU Port Interrupt #1 (L1)Lo True	BCRUFI1*	I	NU	S	NU
65	Guard Ground		NU	NU	NU	NU
66	Guard Ground		NU	NU	NU	NU
67	TMS9901 Chip Enable Lo True	N901CE*	I	S	NU	NU
68	Disk Interrupt (L5) Lo True	DSKI*	I	S	NU	NU
69	System CRU Clock Hi True	CRUCLK	O	I	I	I
70	System CRU INPUT Data Hi True	CRUIN	T	NU	T	T
71	System Reset Lo True	SRESET*	S	I	I	I
72	System CRU OUT Data Hi True	CRUOUT	S	I	I	I
73	Not Assigned					
74	Unsynchronized System Reset	URESET*	I	T	NU	NU
75	Ground Guard (Power-On-Clear)		NU	NU	NU	NU
76	Ground Guard		NU	NU	NU	NU
77	Not Assigned		NU	NU	NU	NU
78	TMS 9902 UART Inter. (L7) Lo True	EIAFI*	I	NU	S	NU
79	Interrupt Level 9, SPARE, Lo True		I	NU	NU	NU
80	Printer Interrupt (L8),	PTRI*	I	S	NU	NU
81	CRU Port Interrupt #3 (L11)Lo True	BCRUFI3*	I	NU	S	NU
82	CRU Port Interrupt #2 (L10)Lo True	BCRUFI2*	I	NU	S	NU
83	CRU Port Interrupt #5 (L13)Lo True	BCRUFI5*	I	NU	S	NU
84	CRU Port Interrupt #4 (L12)Lo True	BCRUFI4*	I	NU	S	NU
85	Guard Ground		NU	NU	NU	NU
86	Guard Ground		NU	NU	NU	NU
87	Not Assigned		NU	NU	NU	NU
88	Not Assigned		NU	NU	NU	NU
89	System Memory Request Lo True	MEMEN*	T	T	I	I
90	System Byte Pointer O=MSBY,1=LSBY	SPOINTM*	I	S	NU	NU
91	READY Control to CPU Hi True	XREADY	I	S	NU	NU
92	CPU WAIT Output Hi True	WAIT	S	I	NU	NU
93	Syst READY Fr Refsh Logic Hi True	SREADY	S	I	NU	NU
94	DMAC Cycle In Progress Lo True	DMCY*	I	S	NU	NU
95	Logic Ground		I	I	I	I
96	Logic Ground		I	I	I	I
97	Logic Ground		I	I	I	I
98	Logic Ground		I	I	I	I
99	Logic Ground		I	I	I	I
100	Logic Ground		I	I	I	I

APPENDIX E

I/O Backplane Pin Definition

Pin#	Definition	MLB1	MLB2	MLB3	MLB4
1	-5V Power	I	NU	NU	I
2	-5V Power	I	NU	NU	I
3	-5V Power	I	NU	NU	I
4	-5V Power	I	NU	NU	I
5	Logic Ground	I	I	I	I
6	Logic Ground	I	I	I	I
7	Logic Ground	I	I	I	I
8	Logic Ground	I	I	I	I
9	Logic Ground	I	I	I	I
10	Logic Ground	I	I	I	I
11	Logic Ground	I	I	I	I
12	Logic Ground	I	I	I	I
13	+12V Power	I	I	I	I
14	+12V Power	I	I	I	I
15	+12V Power	I	I	I	I
16	+12V Power	I	I	I	I
17	+5V Power	I	I	I	I
18	+5V Power	I	I	I	I
19	+5V Power	I	I	I	I
20	+5V Power	I	I	I	I
21	+5V Power	I	I	I	I
22	+5V Power	I	I	I	I
23	-12V Power	I	I	I	I
24	-12V Power	I	I	I	I
25	Not Assigned				
26	Not Assigned				
27	Not Assigned				
28	Not Assigned				
29	Not Assigned				
30	Not Assigned				
31	Not Assigned				
32	Not Assigned				
33	Not Assigned				
34	Not Assigned				
35	Not Assigned				
36	Not Assigned				
37	Not Assigned				
38	Not Assigned				
39	Not Assignew				
40	Not Assigned				
41	Not Assigned				
42	Not Assigned				
43	MLB1 Test Point # 3 TP3	I	NU	NU	NU
44	Reserved For Disk Drives	NU	I/O	NU	NU
45	Reserved For Disk Drives	NU	I/O	NU	NU
46	Reserved For Disk Drives	NU	I/O	NU	NU
47	Reserved For Disk Drives	NU	I/O	NU	NU
48	Reserved For Disk Drives	NU	I/O	NU	NU
49	Reserved For Disk Drives	NU	I/O	NU	NU
50	Reserved For Disk Drives	NU	I/O	NU	NU

APPENDIX E

I/O Backplane Pin Definition

Pin#	Definition	MLB1	MLB2	MLB3	MLB4
51	Reserved For Disk Drives	NU	I/O	NU	NU
52	Reserved For Disk Drives	NU	I/O	NU	NU
53	Reserved For Disk Drives	Nu	I/O	NU	NU
54	Reserved For Disk Drives	NU	I/O	NU	NU
55	Reserved For Disk Drives	NU	I/O	NU	NU
56	Reserved For Disk Drives	NU	I/O	NU	NU
57	Reserved For Disk Drives	NU	I/O	NU	NU
58	Reserved For Disk Drives	NU	I/O	NU	NU
59	Reserved For Disk Drives	NU	I/O	NU	NU
60	Reserved For Disk Drives	NU	I/O	NU	NU
61	MLB1 Test Point 0 TP0	I	NU	NU	NU
62	Reserved For Disk Drives	NU	I/O	NU	NU
63	Reserved For Disk Drives	NU	I/O	NU	NU
64	Reserved For Disk Drives	NU	I/O	NU	NU
65	Reserved For Disk Drives	NU	I/O	NU	NU
66	Reserved For Disk Drives	NU	I/O	NU	NU
67	Reserved For Disk Drives	NU	I/O	NU	NU
68	Reserved For Disk Drives	NU	I/O	NU	NU
69	Reserved For Disk Drives	NU	I/O	NU	NU
70	Reserved For Disk Drives	NU	I/O	NU	NU
71	MLB1 Test Point 1 TP1	I	NU	NU	NU
72					
73	MLB1 Test Point 2 TP2	I	NU	NU	NU
74	Reserved For Printer	NU	S	NU	NU
75	Reserved For Printer	NU	S	NU	NU
76	Reserved For Printer	NU	S	NU	NU
77	Reserved For Printer	NU	S	NU	NU
78	Reserved For Printer	NU	S	NU	NU
79	Guard Ground	NU	I	NU	NU
80	Guard Ground	NU	I	NU	NU
81	Keyboard Interrupt (L2) Lo True, KBI*	I	NU	NU	NU
82	Keyboard Data Bit 5 KB5	I	NU	NU	NU
83	Keyboard Data Bit 6 KB6	I	NU	NU	NU
84	Power Going Down Inter. (11)Lo True PGD*	I	NU	NU	NU
85	Keyboard Data Bit 4 KB4	I	NU	NU	NU
86	Keyboard Data Bit 3 KB3	I	NU	NU	NU
87	Keyboard Data Bit 7 (MSB) KB7	I	NU	NU	NU
88	Keyboard Data Bit 2 KB2	I	NU	NU	NU
89	Keyboard Data Bit 1 KB1	I	NU	NU	NU
90	Keyboard Interrupt Reset KBIRST*	S	NU	NU	NU
91	Not Assigned				
92	Keyboard Data Bit 0 (LSB) KB0	I	NU	NU	NU
93	+15V For Monitor	NU	NU	I	NU
94	+15V For Monitor	NU	NU	I	NU
95	+15V For Monitor	NU	NU	I	NU
96	+15V For Monitor	NU	NU	I	NU
97	Monitor Ground	NU	NU	I	NU
98	Monitor Ground	NU	NU	I	NU
99	Monitor Ground	NU	NU	I	NU
100	Monitor Ground	NU	NU	I	NU

KEYBOARD EN
99 KEYS, 4 MODES

APPENDIX F

MEMORY PRODUCTS

JUNE 1976

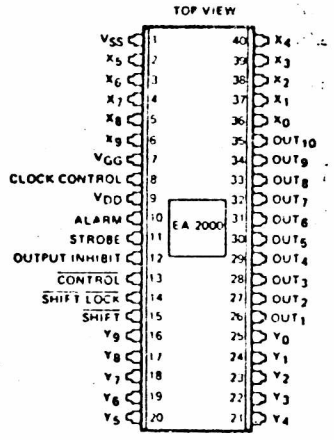
GENERAL DESCRIPTION

The EA 2000 is a monolithic keyboard encoder utilizing MOS P-channel integrated circuit technology. The EA 2000 encodes 99 keys, with four modes per key, allowing 396 different key codes. Each key code contains 10 parallel output bits. N-key rollover is provided together with automatic key bounce suppression, alarm signal for detection of simultaneous key depression, data ready strobe, electronic shift lock, and output inhibit features. The Shift Control and Output Inhibit inputs are all TTL compatible. All outputs are TTL compatible. Standard +5V and –12V supplies are used. Custom programming of the encoder matrix (4000 bits) is accomplished by the alteration of one mask used in the fabrication of the device. An internal clock generator is built into the device.

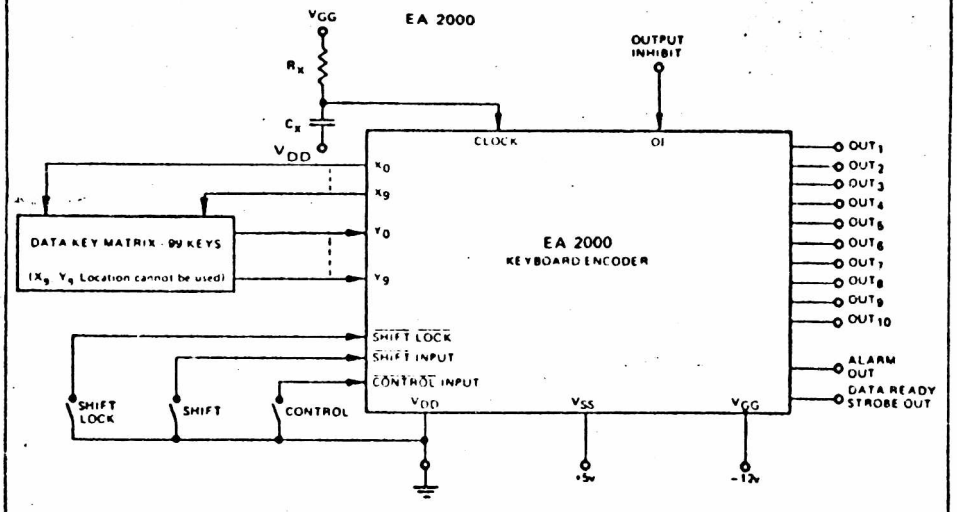
FEATURES

- 99 KEY, FOUR MODE OPERATION
- FULLY PROGRAMMABLE 10 BIT OUTPUT WORDS
- N-KEY ROLLOVER
- ERROR DETECTION FOR SIMULTANEOUS KEY DEPRESSIONS
- AUTOMATIC KEY BOUNCE PROTECTION
- ELECTRONIC SHIFT LOCK
- INTERNAL CLOCK GENERATOR
- TTL COMPATIBLE – 3-STATE OUTPUTS

CONNECTION DIAGRAM
40 LEAD DIP



SYSTEM DIAGRAM
EA 2000



ORDERING INFORMATION

	Temp. Range	Package
EA20XXCD	0°C to +70°C	Hermetic 40 Pin DIP
EA20XXCP	0°C to +70°C	Molded 40 Pin DIP

Custom bit patterns require a unique bit pattern number (XX) assigned by Electronic Arrays.

electronic arrays, inc.

550 east middlefield road, mountain view, california 94043 • telephone (415) 964-4321 • TWX 910-379-6985

ABSOLUTE MAXIMUM RATINGS

V_{DD} Supply Voltage (Relative to V_{SS})	+0.5V to -20V
V_{GG} Supply Voltage (Relative to V_{SS})	+0.5V to -20V
Operating Temperature Range (Ambient)	0°C to +70°C
Storage Temperature	-65°C to +150°C

Stresses more severe than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and operation of the device at any condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions unless otherwise noted. All voltages are referenced with respect to GND. Positive current is defined as flowing into the referenced pin.

$+4.75V \leqslant V_{SS} \leqslant +5.25V$ $-11.4V \geqslant V_{GG} \geqslant -12.6V$ $V_{DD} = GND$

$0°C \leqslant T_A \leqslant +70°C$ Output Load = 1 TTL Load

ELECTRICAL DRIVE REQUIREMENTS

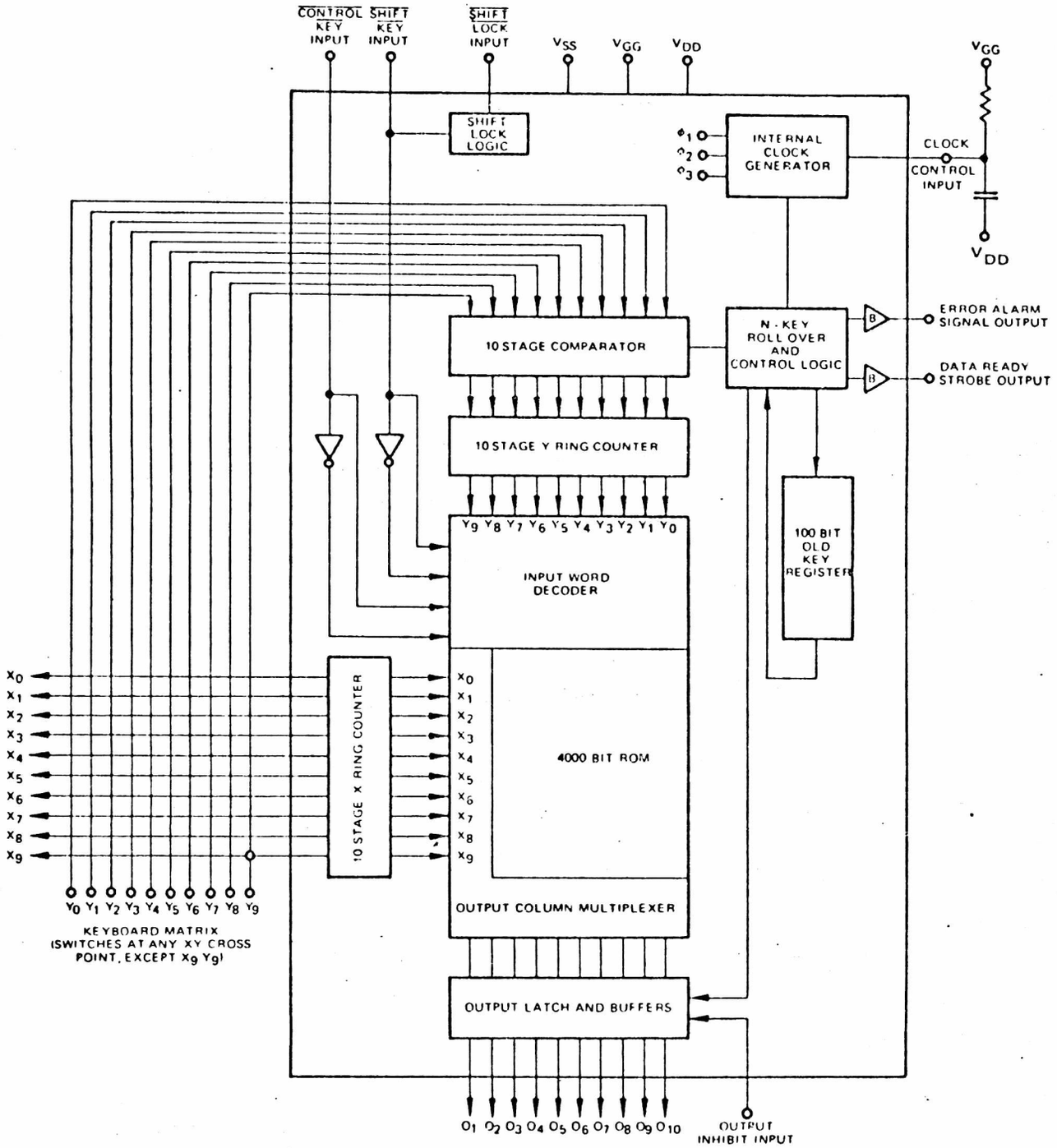
Parameter	Condition	Min.	Typ.	Max.	Units
Clock Frequency (Internal)	Under specified RC conditions(Note1)	40		125	KHz
Clock Frequency (External)	(Note 2)	80		250	KHz
INPUT LEVELS (Control, Shift, Shift Lock, and Output Inhibit)					
Logic "1"		2.8		V_{SS} +0.3	Volts
Logic "0"				+0.8	Volts
ALLOWABLE KEYSWITCH LOAD					
Series Contact Resistance				500	Ohms
Stray Capacitance	(Note 3)			200	pF
Forward Diode Voltage Drop				0.8	Volts

ELECTRICAL CHARACTERISTICS

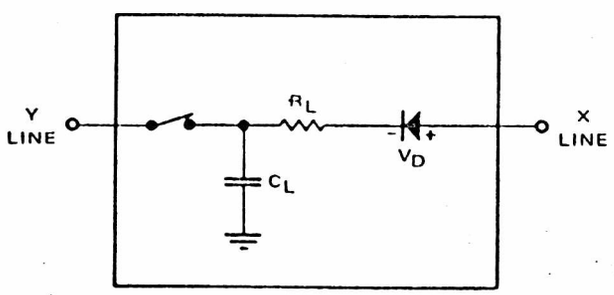
Parameter	Condition	Min.	Typ.	Max.	Units
DATA OUTPUTS					
Logic "0" Level	I = 1.6mA			0.4	Volts
Logic "1" Level	I = -100μA	4.0			Volts
INPUT CAPACITANCE (Control, Shift, Shift Lock, and Output Inhibit)	0 volt bias			5.0	pF
INPUT RESISTANCE (Control, Shift, Shift Lock, and Output Inhibit)	T_A = +25°C	3.0		10	Kohms
POWER SUPPLY CURRENT					
I_{SS} (note 4)	T_A = +25°C		19	24	mA
I_{GG}	T_A = +25°C		19	24	mA
OUTPUT CAPACITANCE				15	pF
OUTPUT LEAKAGE	Disabled $V_O = V_{SS}$			10	μA

NOTES:
1. For the internal frequency to fall within the spec range of 40 to 125 KHz use R_x = 180 Kohms and C_x = 33 pF. These values also assume a 2 pF stray capacitance. For other frequency, resistor, capacitor combinations see operating characteristic graph.
2. Due to a divider network in the internal clock, the external clock frequency at pin 8 is twice the required internal clock frequency.
3. Keyswitch capacitance is defined as the total capacitance between any X or Y line and ground.
4. Input and output interface current not included. Each TTL compatible input adds 1.75 mA maximum to I_{SS}.

BLOCK DIAGRAM



KEY SWITCH PARAMETER:



R_L max = 500 Ω
C_L max = 200 pF
V_D max = 0.8 V

1. KEYBOARD SCANNING

The EA 2000 automatically scans a 99-key keyboard, generating continuous sequential outputs on the X outputs and detecting key closures on the Y inputs.

The scanning circuitry consists of a 10-stage X ring counter, a 10-stage Y ring counter, and a 10-bit word comparator as shown in the block diagram.

Only one stage of a ring counter can be in the "one" state at any point in time. A "one" in the Y ring counter is shifted one position with each clock period. Every 10th clock period the Y ring counter generates a clock enable signal which gates the clock to the X ring counter. Thus, the Y ring counter controls the clocking to the X ring counter. The clock rate of the Y ring counter is ten times the clock rate of the X ring counter and a complete cycle of the X and Y ring counters requires 100 clock periods. The single ended outputs of the X ring counter drive the 10 rows of the key matrix. The Y ring counter outputs feed a 10-stage comparator which compares each Y ring counter output with a Y (column) line from the key matrix. The key matrix is limited to 99 keys since internal control logic is being reset at the time the 100th key is being scanned.

When a key is depressed, an X output line drives a Y line to a logic one. The word comparator generates a "one" level when the Y ring counter output and the Y line are both a logic one.

A load capacitance of 200 pF can be driven by the X lines. Also, a diode and a series resistance of 500 ohms can be placed between the X and Y lines. When a key is depressed, the Y line switches to a logic one which is a minimum voltage of +3 volts.

2. KEY VERIFICATION

A key depression will be considered verified after it is detected three times by the scanning matrix. When a key is detected the first time, an internal flip-flop will be set. If the key is again detected in the second and third scan cycle, an output code will be generated and will be available at the Output pins. At the beginning of the fourth scan cycle, Data Ready Strobe will become true (logic 1) indicating that valid data is available. This verification technique automatically accomplishes key bounce protection. A key will not be recognized unless it is detected through these successive scan cycles. Key bounce protection can be adjusted indirectly by modifying the clock frequency.

3. ENCODING ROM

The output code for each key depression is stored in 4000 bit ROM which is permanently programmed during the manufacture of the encoder. This ROM program is established by the user and transmitted to Electronic Arrays using either truth tables, paper tape or punched cards.

The 4000 bit ROM provides the user with complete flexibility for each of the 10-bit output words for each key depression and mode. Therefore, output data words are completely programmable with no restrictions.

4. ALARM SIGNAL

The Alarm output or error signal will become true (logic 1) whenever two new keys are detected as being closed during a verification cycle. A new key is defined as one for which valid data (indicated by a Data Ready Strobe) has not been outputed. The Alarm signal is reset or cleared by the occurrence of any of the following conditions:

a. The first end-of-scan after all keys have been released.

b. If one new key is detected after the alarm condition is cleared, but before the Alarm signal is cleared, the Alarm will clear at the beginning of the next scan cycle.

c. If an old key is still depressed (not one which caused the alarm condition), and one new key is detected after the alarm condition is cleared but before the Alarm is cleared, the Alarm signal will clear at the end-of-scan of the following cycle (one scan cycle before strobe).

5. ELECTRONIC SHIFT LOCK

The shift lock input will provide for sustained operation of the keyboard in the shift mode. Shift lock is enabled by applying an external logic "0" to the shift lock input pin. Reset of the shift lock operation occurs when a shift signal is applied. The shift lock lead will directly drive a transistor buffer which will provide current for an indicator lamp.

6. DATA READY SIGNAL

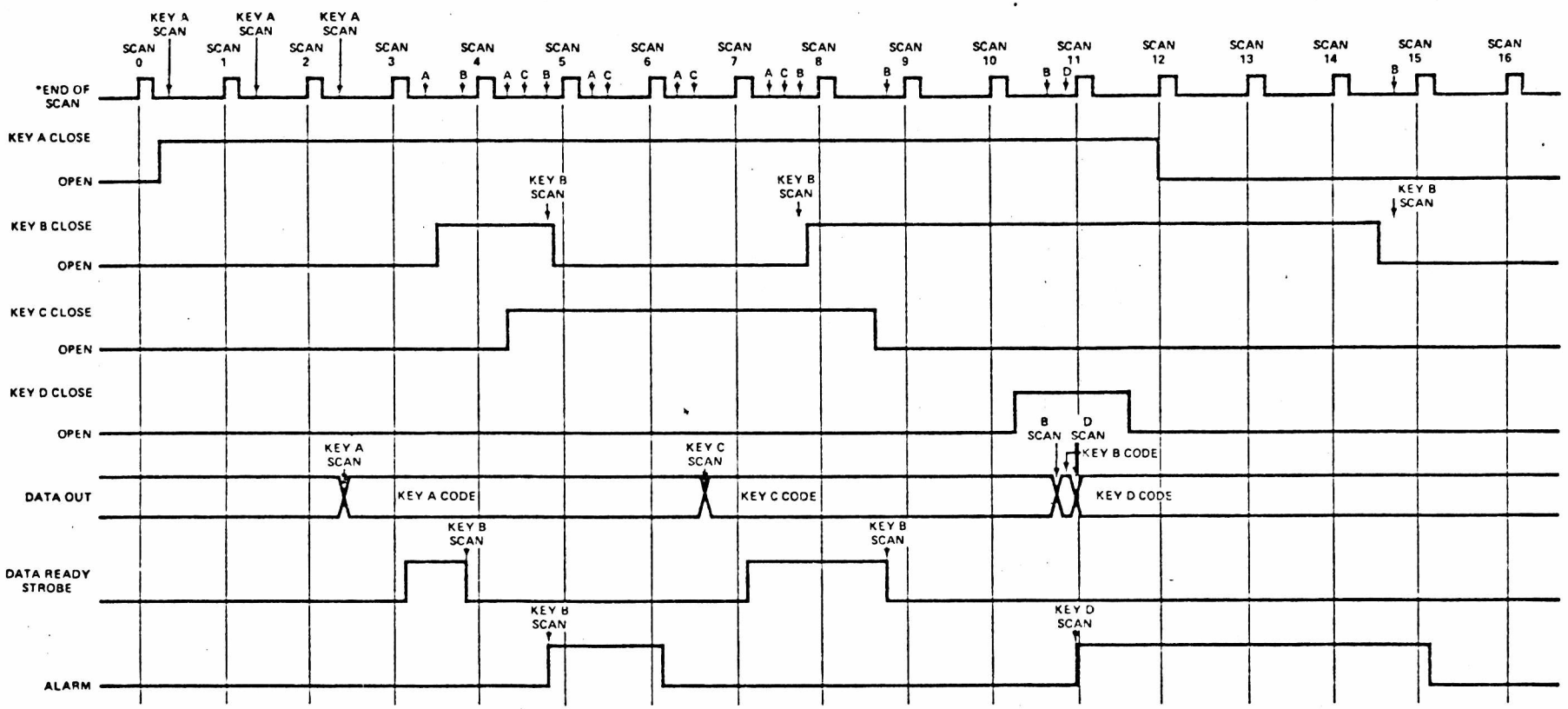
When a new key depression is verified and its output code has been generated, the Data Ready Strobe will switch to a logic 1 state at the beginning of the following scan cycle. The Data Ready Strobe then remains in the logic 1 state and is reset either the first time a new key is scanned, or the first end-of-scan after all keys are detected as released.

7. OUTPUT INHIBIT

A logic "1" applied to the output inhibit input causes the ten data output lines to remain in the high impedance state.

8. TTL INTERFACE

The Keyboard Encoder outputs will drive TTL directly without external resistors. The control, output inhibit, shift, and shift lock inputs have internal pull-up resistors so that no external resistors are required for direct TTL compatability on these inputs.



*DENOTES SIGNAL INTERNAL TO EA 2000.

1. End of scan is signal internal to the EA2000.
2. At a clock frequency of 100 KHz, each scan cycle is 1 msec in duration. During each scan cycle all 99 key locations are scanned.
3. If all keys are released, the data ready strobe returns to a logic "0" state, but the data output lines maintain the code of the last depressed key. If this condition is not desirable, the output inhibit can be used to float the data outputs.
4. At power up, the encoder outputs will assume an arbitrary key code until a key is depressed and detected. However, the data ready strobe will come on in the "zero" state.

Custom bit pattern information for the EA 2000 keyboard encoder can be supplied to Electronic Arrays either on standard 80 column computer cards or on the Keyboard Encoder Bit Pattern form. Either the forms or the computer cards will be used by Electronic Arrays' computer aided programming system to generate a printout for customer verification as well as the necessary tooling and test data to manufacture the custom device.

Keyboard Encoder Bit Pattern Form – When using the Keyboard Bit Pattern Form, it is necessary that the customer name, customer part number, Electronic Arrays' part number and date appear in the appropriate blocks at the top of the form. Each key is then listed in accordance with its X–Y matrix location. The appropriate one/zero bit pattern is then entered in the spaces provided for each of the four modes of operation. The keys need not be listed in numerical sequence and keys which are not used need not be listed. If fewer than ten output bits are used for any particular key mode, zeroes must be entered for the unused bits. The printout produced by our computer aided programming system will include a listing of all undefined keys. These will be programmed as logic "0's."

Computer Card Format – Custom bit pattern data may be supplied on standard 80 column computer cards. When using this media, a control card is required and it must be accompanied by an additional card for each programmed key. The control card format should be as follows:

Column	
1	Punch an asterisk.
2–25	Customer name.
26–40	Customer part number.
51–80	Optional.

Data Card Format

Column	
4	X key location.
5	Y key location.
6–7	Blank.
8–17	Output word for key location X, Y. Shift, logic 0; Control, logic 0 (output 10 in column 8, output 9 in column 9, etc.).
18–27	Output word for key location X, Y. Shift, logic 0; Control, logic 1 (output 10 in column 18, output 9 in column 19, etc.).
28–37	Output word for key location X, Y. Shift, logic 1; Control, logic 0 (output 10 in column 28, output 9 in column 29, etc.).
38–47	Output word for key location X, Y. Shift, logic 1; Control, logic 1 (output 10 in column 38, output 9 in column 39, etc.).
48–80	Optional.

Keyboard Encoder Bit Pattern Form

page ⌴ of ⌴

electronic arrays, inc.
501 ellis street, Mt. View, Calif.

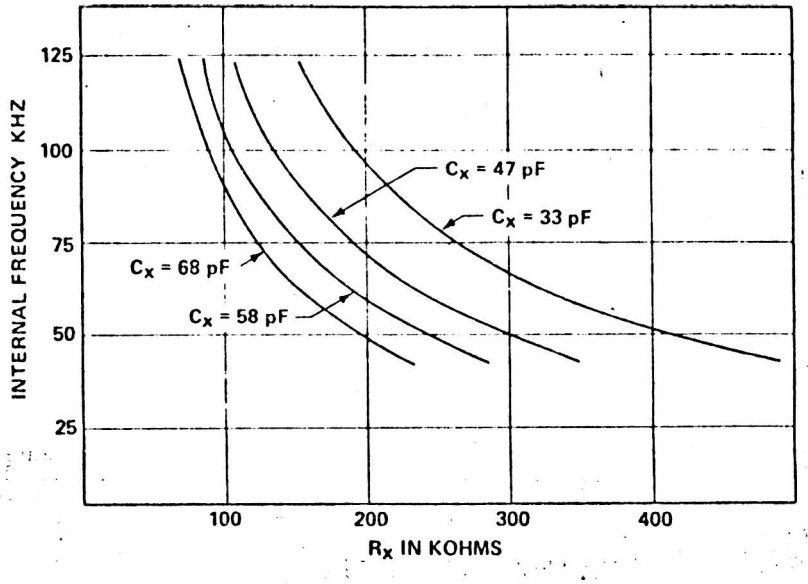
CUSTOMER NAME ⌴ PART NUMBER ⌴ REV. ⌴ authorized signature

program identification ⌴ identification code ⌴ number ⌴ rev. ⌴ DATE ⌴ month / ⌴ day / ⌴ year

KEY ADDRESS Matrix Location		CONTENTS			
		S,C=0,0	S,C=0,1	S,C=1,0	S,C=1,1
X	Y	OUTPUTS 10 9 8 7 6 5 4 3 2 1	OUTPUTS 10 9 8 7 6 5 4 3 2 1	OUTPUTS 10 9 8 7 6 5 4 3 2 1	OUTPUTS 10 9 8 7 6 5 4 3 2 1

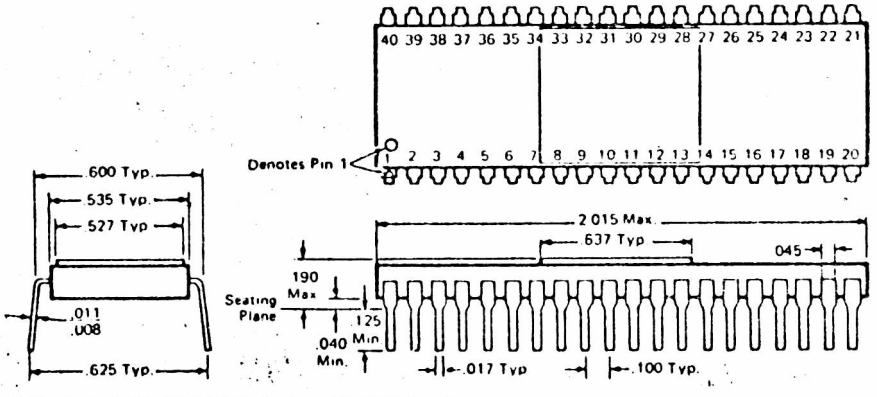
TYPICAL FREQUENCY RESISTOR, CAPACITOR VALUES

EA 2000

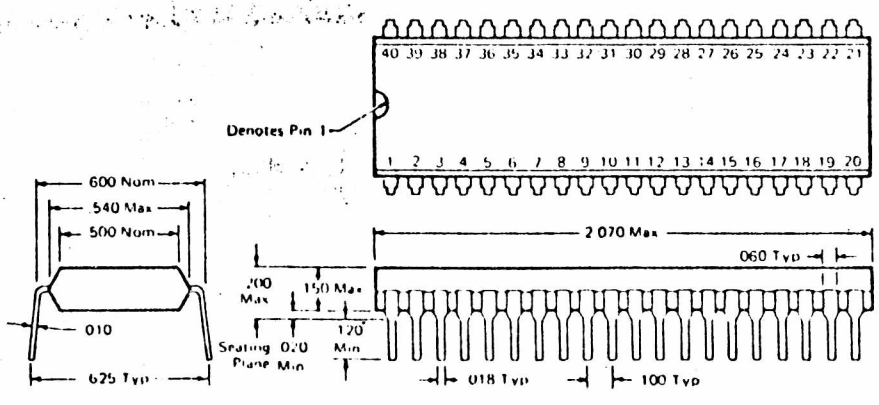


PHYSICAL DIMENSIONS

40 LEAD HERMETIC DIP



40 LEAD SILICONE DIP



Printed in U.S.A.

Electronic Arrays, Inc., 550 East Middlefield Road, Mountain View, CA 94043, telephone (415) 964-4321, TWX 910-379-6985

FLOPPY DISK FORMATTER/CONTROLLER

FEATURES

- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
- READ MODE
  - Single/Multiple Record Read with Automatic Sector Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Record
- WRITE MODE
  - Single/Multiple Record Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Selectable Head Settling and Head Engage Times
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-chip Track and Sector Registers Comprehensive Status Information

APPLICATIONS

FLOPPY DISK DRIVE INTERFACE
SINGLE OR MULTIPLE DRIVE CONTROLLER/FORMATTER
NEW MINI-FLOPPY CONTROLLER

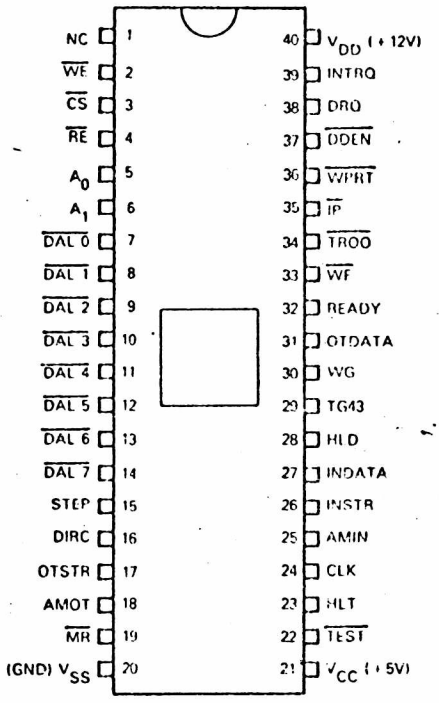
GENERAL DESCRIPTION

The FD1781 is a MOS/LSI device that performs the functions of a Floppy Disk Controller/Formatter. The device is designed to be included in the disk drive electronics, and contains a flexible interface organization that accommodates the interface signals from most drive manufactures. When in the single density mode the FD1781 is fully IBM-3740 compatible. In the double density mode, the type of encoding scheme is a function of the user's data recovery circuits. In this manner both M²FM or MFM is obtainable.

The processor interface consists of a 8-bit bi-directional bus for data, status, and control word transfers. The FD1781 is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD1781 is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs.

PIN CONNECTIONS



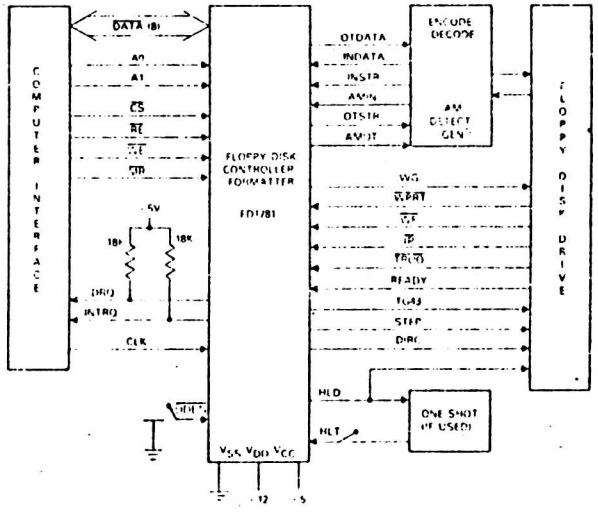
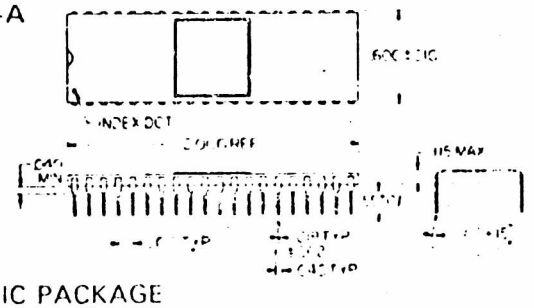


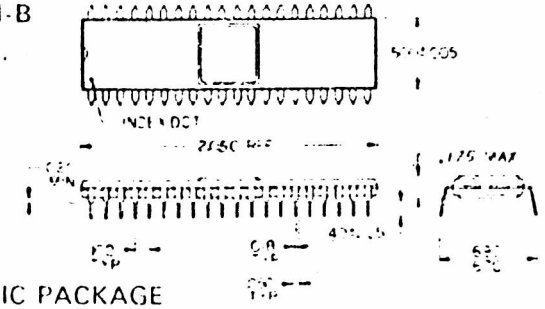
FIG. 1. 1781 SYSTEM BLOCK DIAGRAM

FD1781-A



CERAMIC PACKAGE

FD1781-B



PLASTIC PACKAGE

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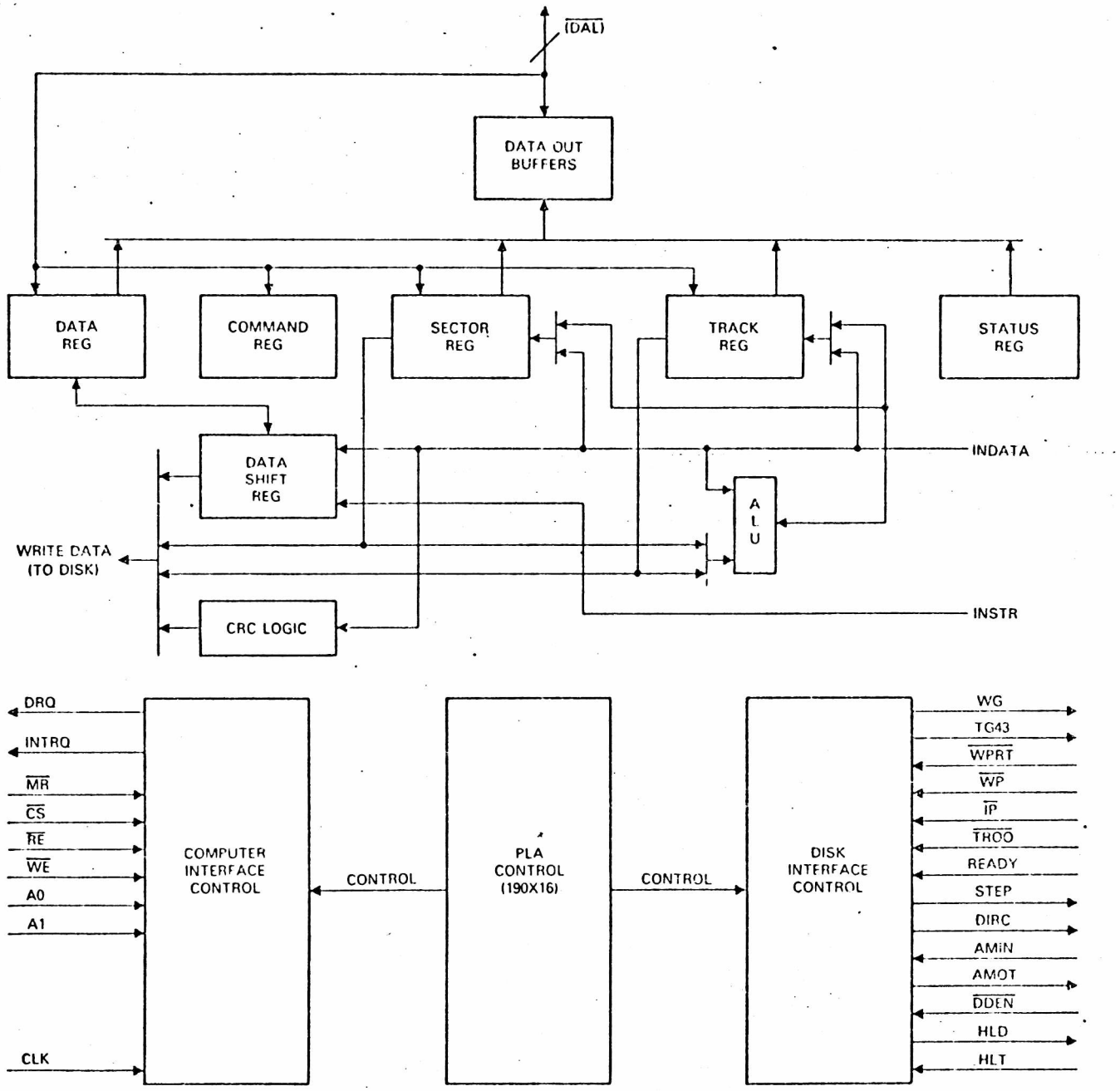

FIG. 3. FD1781 BLOCK DIAGRAM

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated above. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input (INDATA) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

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Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits are a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1781 has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double density is assumed. When $\overline{DDEN}$ = 1, single density is assumed. During disk read operations, the user must provide both data recovery and address mark detection circuits external to FD1781 in both single and double density modes. Thus for disk read operations, the user must provide as an input to the FD1781 Data (INDATA) a strobe to indicate when the data is valid (INSTR) and address mark detect (AMIN). During disk write operations and in the double density mode, the FD1781 provides as outputs Data (OTDATA), a strobe to indicate validity (OTSTR) and Address Mark Out (AMOT). During disk write operation and in the single density mode, OTSTR becomes Write Data (WD) which is exactly the same as in the FD1771.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD1781. The DAL are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The least-significant address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1-A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1781 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

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On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

The Lost Data bit and certain other bits in the Status Register will activate the interrupt request (INTRQ). The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The Floppy Disk interface consists of head positioning controls, write gate controls, and data transfers. The Clock (CLK) input is normally a free-running 2 MHz ±1% when in the double density mode and 1 MHz ±1% when in the single density mode. However when using a mini-floppy, the CLK is normally 1 MHz when in double density mode and 1/2 MHz when in the single density mode.

HEAD POSITIONING

Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 10 milliseconds of head settling time takes place. The four programmable stepping rates are tabulated below.

The rates (shown in Table 1) can be applied to a Step-Direction Motor through the device interface.

Step — A 2 μs pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC) — The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 10 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not made but the CRC checks, an interrupt is generated, the Seek Error status (Bit 4) is set and the Busy status bit is preset.

TABLE 1
STEPPING RATES

CLK	2 MHz	1 MHz	1 MHz	1/2 MHz	2 MHz	1 MHz
$\overline{DDEN}$	0	1	0	1		
R1 R0	$\overline{TEST}$ = 1	$\overline{TEST}$ = 1	$\overline{TEST}$ = 1	$\overline{TEST}$ = 1	$\overline{TEST}$ = 0	$\overline{TEST}$ = 0
0 0	3 ms	3 ms	6 ms	6 ms	Approx. 400 μs	Approx. 800 μs
0 1	6 ms	6 ms	12 ms	12 ms		
1 0	10 ms	10 ms	20 ms	20 ms		
1 1	20 ms	20 ms	40 ms	40 ms		

The Head Load (HDL) output controls the movement of the read/write head against the disk for data recording or retrieval. It is activated at the beginning of a Read, Write (E Flag On) or Verify Operation, or a Seek or Step operation with the head load bit, h, a logic one remains activated until the third index pulse following the last operation which uses the read/write head. Reading or Writing does not occur until a minimum of 10 msec delay after the HDL signal is made active. If executing the type 2 commands with the E flag off, there is no 10 msec delay and the head is assumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input every 10 msec. A high logic state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the disk. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic one. In a verify command the head is loaded after stepping to the destination track on the disk whenever the h bit is a logic zero.

DISK READ OPERATION

The normal sector length for Read or Write operations with the IBM 3740 format is 128 bytes. This format or binary multiples of 128 bytes will be adopted by setting a logic 1 in Bit 3 of the Read Track and Write Track commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the length of the sector. Variable sector lengths can

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be read or written in Read or Write commands respectively by setting a logic 0 in Bit of the command word. The sector length indicator specifies the number of 16 byte groups or 16 × N, where N is equal to 1 to 256 groups. An indicator of all zeroes is interpreted as 256 sixteen byte groups.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD1781 before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the $\overline{\text{Write Protect}}$ status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1781 terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the $\overline{\text{Write Gate}}$ output becomes inactive.

Whenever a Read or Write command is received the FD1781 samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the Ready input.

COMMAND DESCRIPTION

The FD1781 will accept and execute eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contain a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1, page four.

TABLE 2
COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	$\overline{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

TABLE 3
FLAG SUMMARY

TYPE I

h = Head Load Flag (Bit 3)

h = 1, Load head at beginning
h = 0, Do not load head at beginning

V = Verify flag (Bit 2)

V = 1, Verify on last track
V = 0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)

Refer to Table 1 for rate summary

u = Update flag (Bit 4)

u = 1, Update Track register
u = 0, No update

TABLE 4
FLAG SUMMARY

TYPE II

m = Multiple Record flag (Bit 4)

m = 0, Single Record
m = 1, Multiple Records

b = Block length flag (Bit 3)

b = 1, IBM format (128 to 1024 bytes)
b = 0, Non-IBM format (16 to 4096 bytes)

a_1a_0 = Data Address Mark (Bits 1-0)

a_1a_0 = 00, FB (Data Mark)
a_1a_0 = 01, FA (User defined)
a_1a_0 = 10, F9 (User defined)
a_1a_0 = 11, F8 (Deleted Data Mark)

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TABLE 5
FLAG SUMMARY

TYPE III
s = Synchronize flag (Bit 0)
$\overline{s}$ = 0, Synchronize to AM
$\overline{s}$ = 1, Do Not Synchronize to AM
TYPE IV
Ii = Interrupt Condition flags (Bits 3-0)
I0 = 1, Not Ready to Ready Transition
I1 = 1, Ready to Not Ready Transition
I2 = 1, Index Pulse
I3 = 1, Immediate interrupt
E = Enable HLD and 10 msec Delay
E = 1, Enable HLD, HLT and 10 msec Delay
E = 0, Head is assumed Engaged and there is no 10 msec Delay

The Type 1 Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command HLD output is made active). If h = 0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD1781 receives a command that specifically disengages the head. If the FD1781 does not receive any commands after two revolutions of the disk, the head will be automatically disengaged (HLD made inactive). The Head Load Timing Input is sampled after a 10 ms delay, when reading or writing on the disk is to occur.

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

During verification, the head is loaded and after an internal 10 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, the Seek Error status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the nex encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after two revolutions of the disk, the FD1781 terminates the operation and sends an interrupt, (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (U). When U = 1, the track register is updated by one for each step. When U = 0, the track register is not updated.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is samples. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 17) at a rate specified by the r_1r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the TR is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD1781 terminates operation, interrupts, and sets the Seek error status

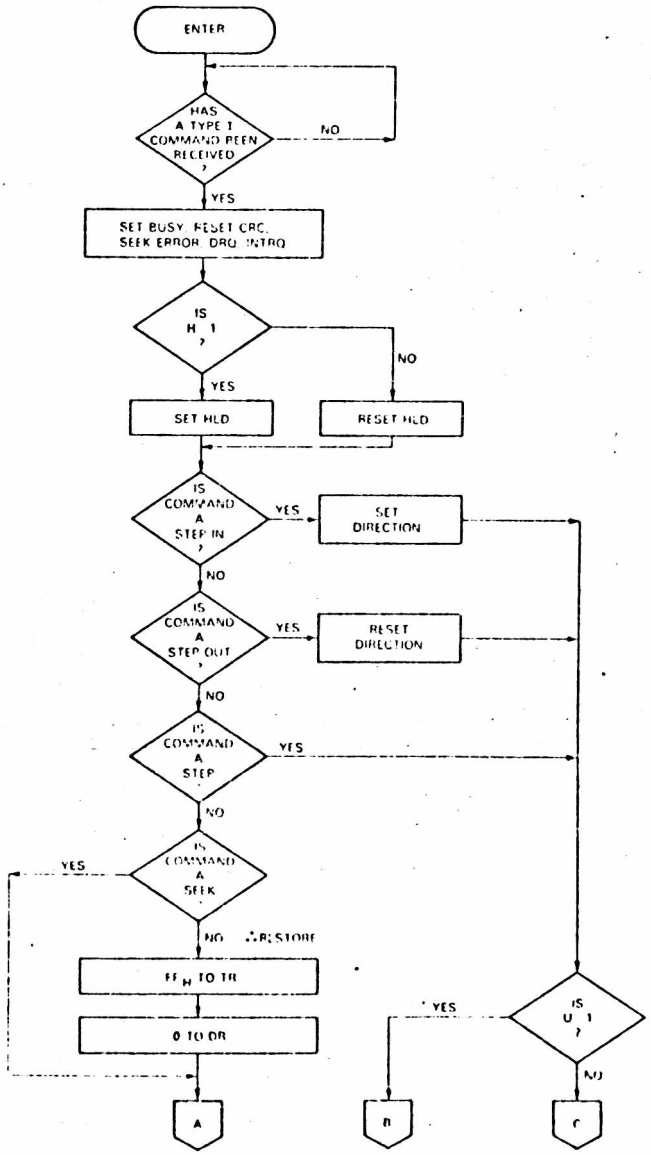

FIG. 4. TYPE I COMMAND FLOW

bit. Note that the Restore command is executed when MR goes from an active to an inactive state. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD1781 will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD1781 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD1781 issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

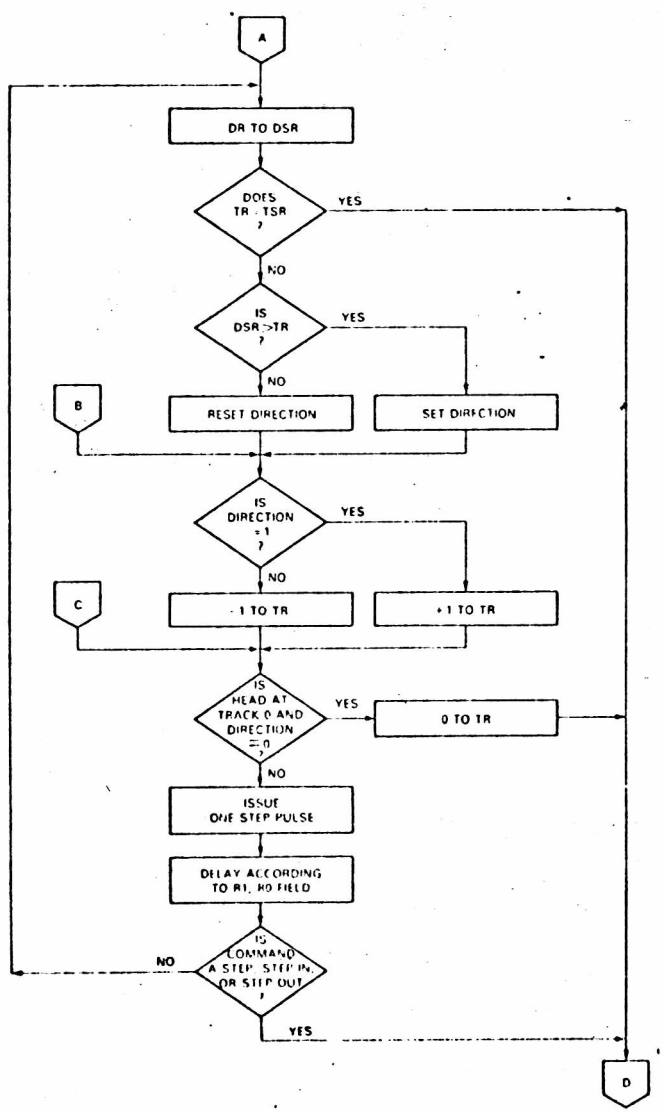

FIG. 5. TYPE I COMMAND FLOW

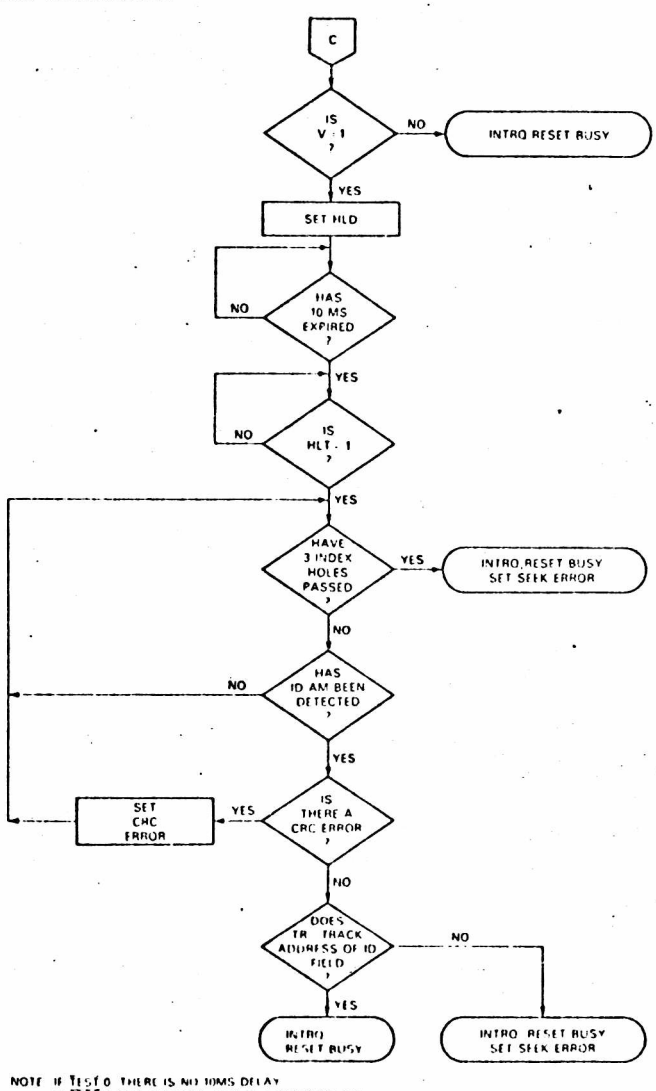

FIG. 6. TYPE I COMMAND FLOW

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STEP-OUT

Upon receipt of this command, the FD1781 issues one stepping pulse in the direction towards track 0. If the u flag is on, the TR is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands include the Read Sector (s) and Write Sector (s) commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II Command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 10 msec delay. If the E flag is 0, the head is assumed to be engaged and there is no 10 msec delay. The ID field and Data Field format are shown below:

When an ID field is located on the disk, the FD1781 compares the Track Number of the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD1781 must find an ID field with a Track number, Sector number, and CRC within two revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contain a (b) flag which in conjunction with the sector length field contents of the ID determines the length (number of characters) of the Data field.

For IBM 3740 compatibility, the b flag should equal 1. The numbers of bytes in the data field (sector) is then 128×2^n where n --0,1,2,3.

For b = 1

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below:

For b = 0

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
01	16
02	32
03	48
04	64
•	•
•	•
•	•
FF	4080
00	4096

Each of the Type II Commands also contain a (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0 a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD1781 will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminated the command and generates an interrupt.

READ COMMAND

Upon receipt of the Read command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 28 bytes of the corrected field; if not, the Record Not Found status bit is set and the operation is terminated.

GAP	ID AM	TRACK NUMBER	ZEROS	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP	DATA AM	DATA FIELD	1	2
ID FIELD									DATA FIELD			

IDAM = ID Address Mark — DATA = $(FE)_{16}$ CLK = $(C7)_{16}$
Data AM = Data Address Mark — DATA = (F8, F9, FA, or FB), CLK = $(C7)_{16}$

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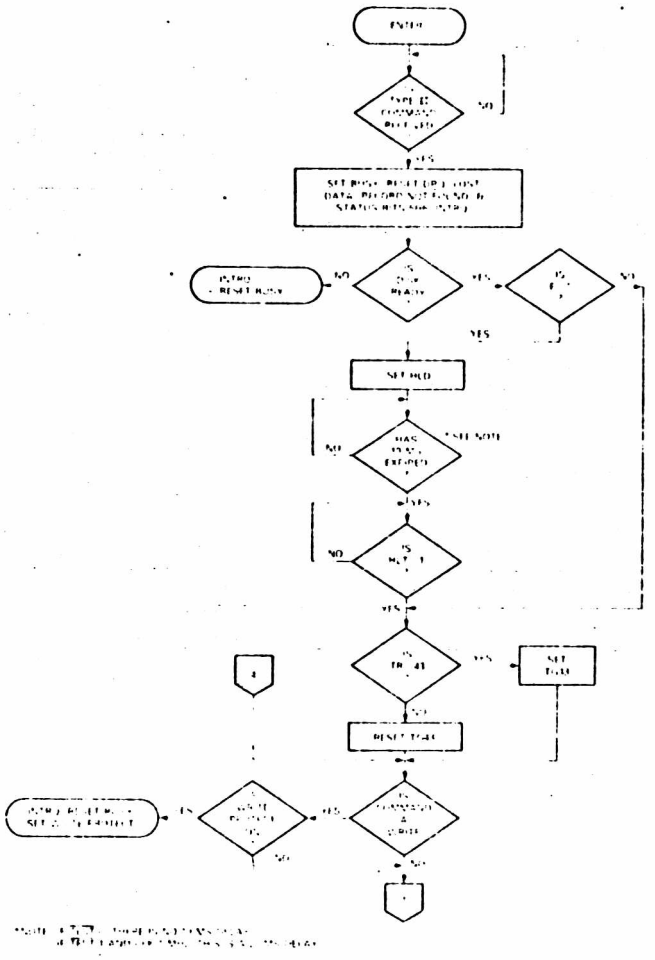

FIG. 7. TYPE II COMMAND

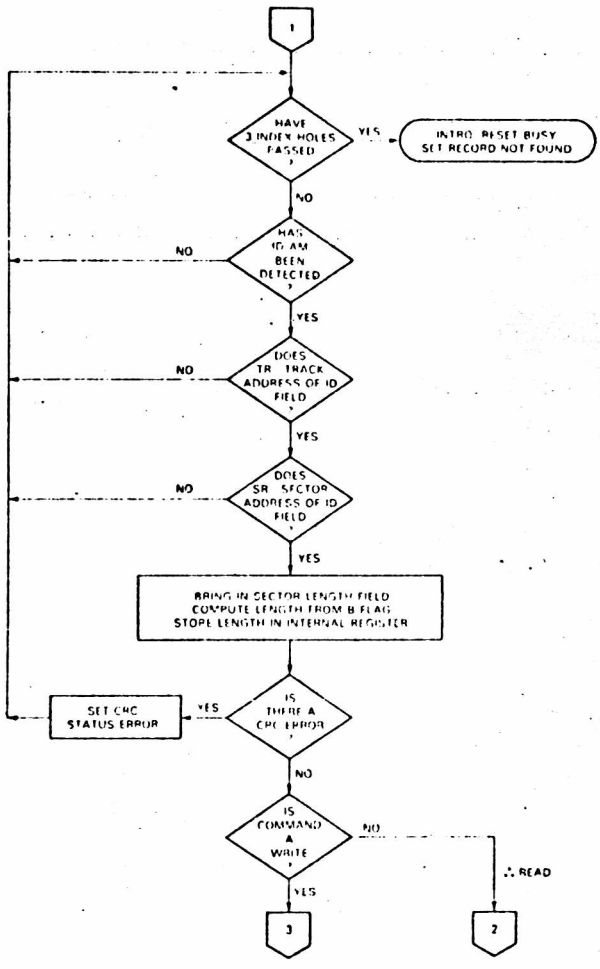

FIG. 8. TYPE II COMMAND

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bits 5 and 6) as shown below:

STATUS BIT 5	STATUS BIT 6	DATA 1	DATA 2	DATA 3
0	0	0	0	0
0	1	0	0	1
1	0	0	1	0
1	1	0	1	1

WRITE COMMAND

Upon receipt of the Write command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The FD1781 counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a^1a^0 field of the command as shown below:

a^1	a^0	DATA 1	DATA 2	DATA 3
0	0	0	0	0
0	1	0	0	0
1	0	1	1	0
1	1	0	1	1

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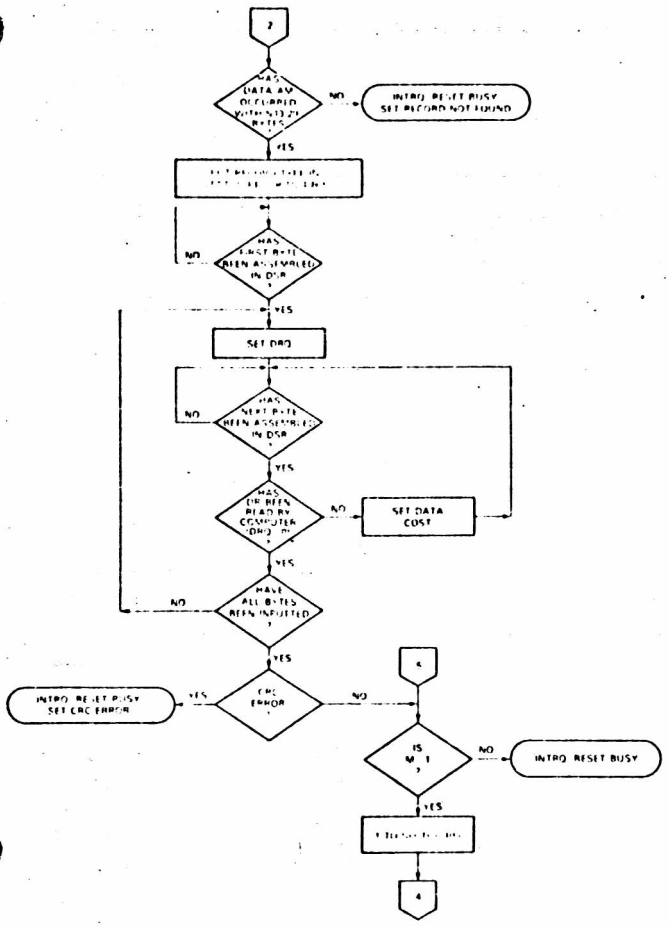

FIG. 9. TYPE II COMMAND

The FD1781 then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte gap of logic ones. The WG output is then deactivated.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	ZEROS	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

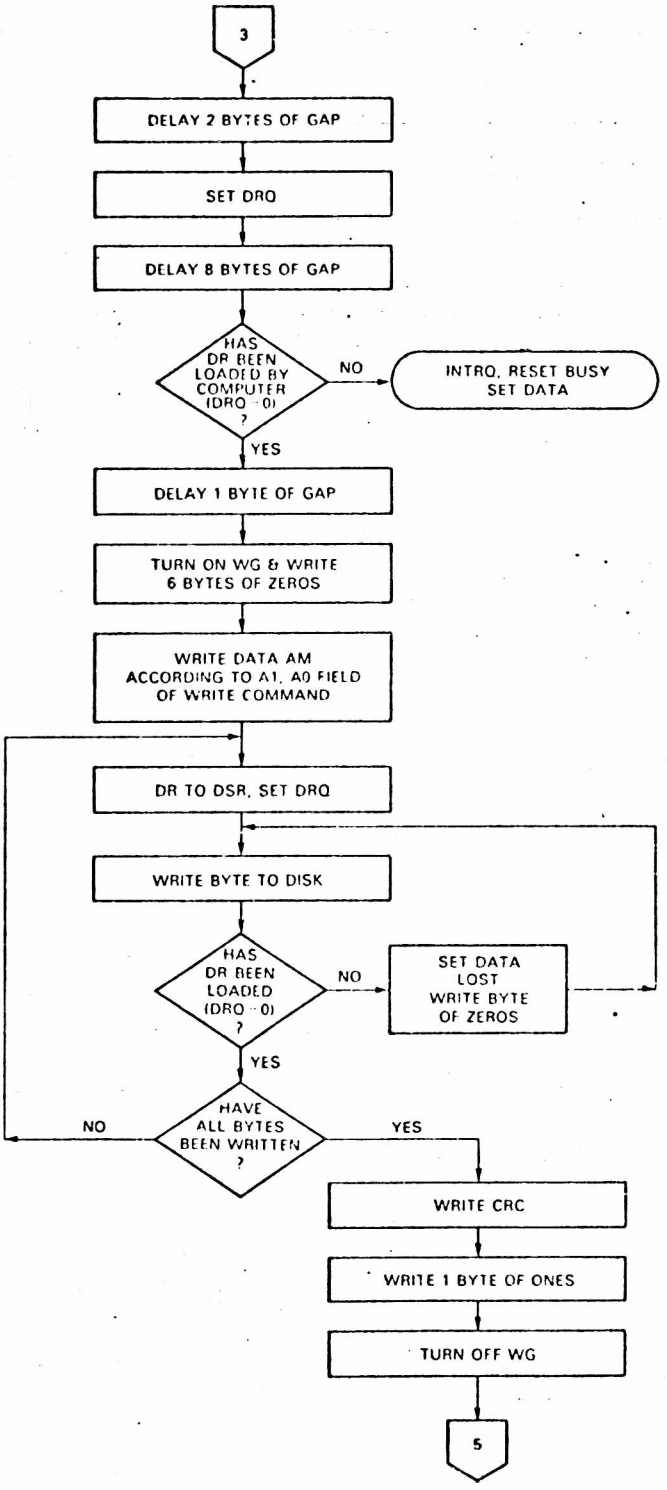

FIG. 10. TYPE II COMMAND

Although the CRC characters are transferred to the computer, the FD1781 checks for validity and the CRC error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

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READ TRACK

Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If bit 0 (S) of the command is a 0, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

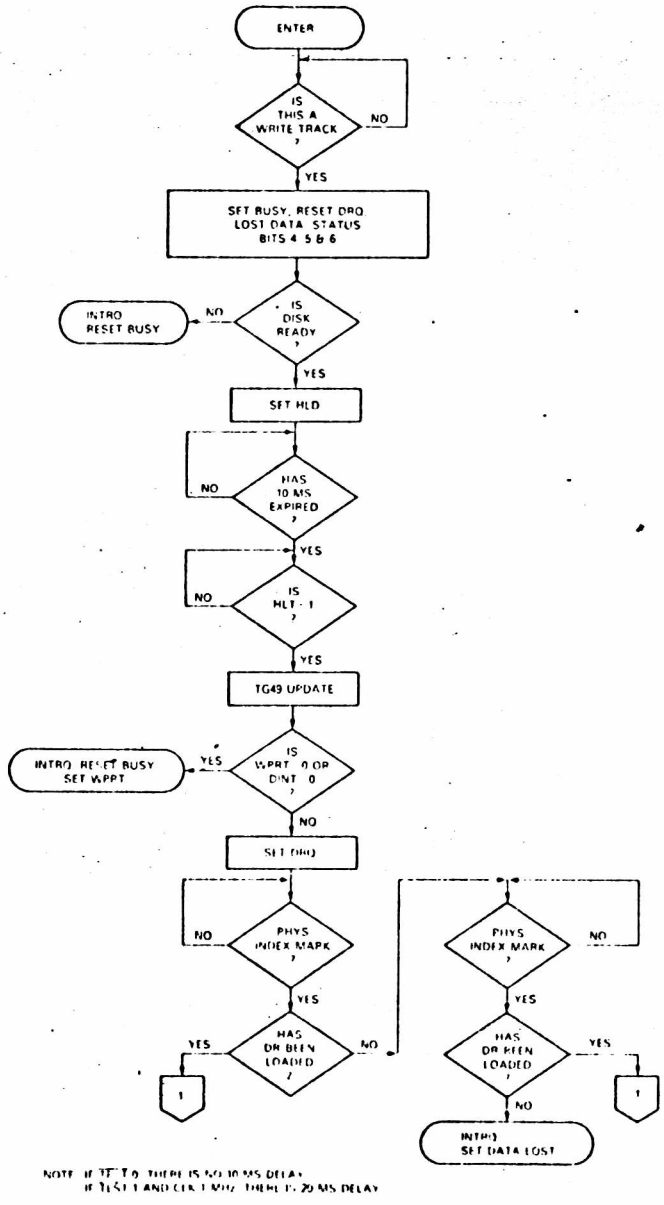

FIG. 11. TYPE III COMMAND WRITE TRACK

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR.

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK* (HEX)
F7	Write CRC Char.	FF
F8	Data Addr. Mark	C7
F9	Data Addr. Mark	C7
FA	Data Addr. Mark	C7
FB	Data Addr. Mark	C7
FC	Index Addr. Mark	D7
FD	Spare	
FE	ID Addr. Mark	C7

*Single density only

DATA 1	DATA 2	DATA 3	TYPE OF ADDRESS MARK
0	0	0	Deleted Data mark
0	0	1	Data Mark (user defined)
0	1	0	Data Mark (user defined)
0	1	1	Data Mark
1	0	0	Index Address Mark
1	0	1	Undefined
1	1	0	ID Address Mark
1	1	1	Undefined

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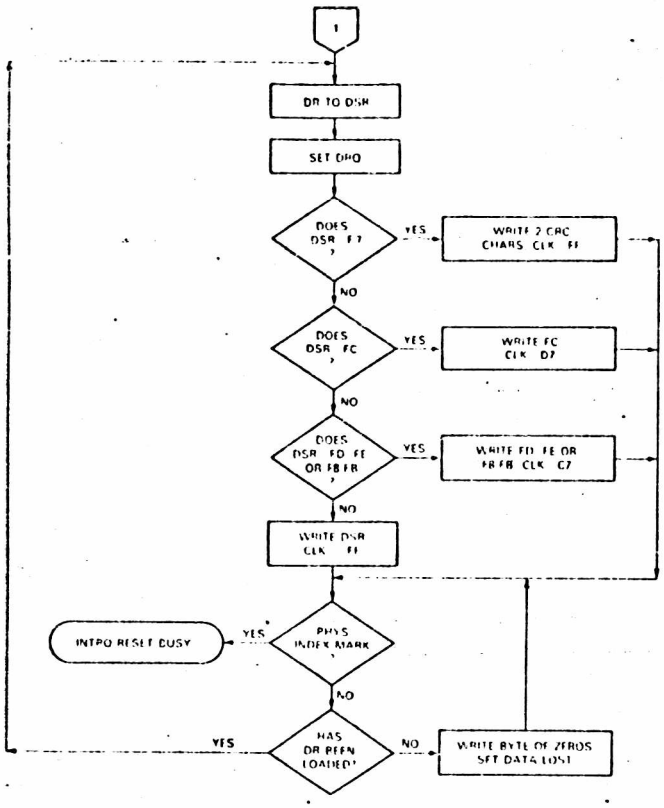

FIG. 12. TYPE III COMMAND WRITE TRACK

TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0 = Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

NOTE: If I_0-I_3 = 0, there is no interrupt generated but the current command is terminated and busy is reset.

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

(BITS)

7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

TABLE 6
STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

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STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 Not Ready	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 when updated.
S2 Track 00	When set, indicates Read Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TROO}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS BITS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 Not Ready	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 RECORD TYPE/ WRITE PROTECT	On read Record: In indicates the MSB of record-type code from data field address mark. On Read Track: Not Used. On any Write: It indicates a Write Fault. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the LSB of record-type code from data field address mark. On Read Track: Not Used. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

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FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD1781 raises the data request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a clock mark of $(FF)_{16}$. However, if the FD1781 detects a data pattern on F7 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters. As a consequence, the patterns F7 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by a F7 pattern.

Disks may be formatted in IBM 3740 formats with sector lengths of 128, 256, 512, or 1024 bytes, or may be formatted in non-IBM 3740 with sectors length of 16 to 4096 bytes in 16 byte increments. IBM 3740 at the present time only defines two formats. One format with 128 bytes/sector and the other with 256 bytes/sector. The next section deals with the IBM 3740 format with 128 bytes/sector and the following section details non-IBM formats.

IBM 3740 FORMATS—128 BYTES/SECTOR

Shown in Figure 13, is the IBM format with 128 bytes/sector. In order to format this format, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	00 or FF
6	00
1	FC (Index Mark)
26	00 or FF
6*	00
1	FE (ID Address Mark)
1	Track Number
1	00
1	Sector Number (1 thru 1A)
1	00
1	F7 (2 CRC's written)
11	00 or FF
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	00 or FF
247**	00 or FF

*Write bracketed field 26 times

**Continue writing until FD1781 interrupts out. Approx. 247 bytes.

NON-IBM FORMATS

Non-IBM formats are very similar to the IBM formats except a different algorithum is used to ascertain the sector length from the sector length byte in the ID field. This permits a wide range of sector lengths from 16 to 4096 bytes. Refer to Section V, Type II Commands with b flag equal to zero. Note that F7 thru FE must not appear in the sector length byte of the ID field.

In formatting the FD1781, only two requirements regarding GAP sizes must be met. GAP 2 (i.e., the gap between the ID field and data field must be 17 bytes of which the last 6 bytes must be zero and that every address mark be preceded by at least one byte of zeros. However, it is recommended that every GAP be at least 17 bytes long with 6 bytes of zeros. The FD1781 does not require the index address mark (i.e., DATA = FC, CLK = D7) and need not be present.

REFERENCES:

1. IBM Diskette OEM Information GA21-9190-1
2. SA900 IBM Compatibility Reference Manual — Shugart Associates.

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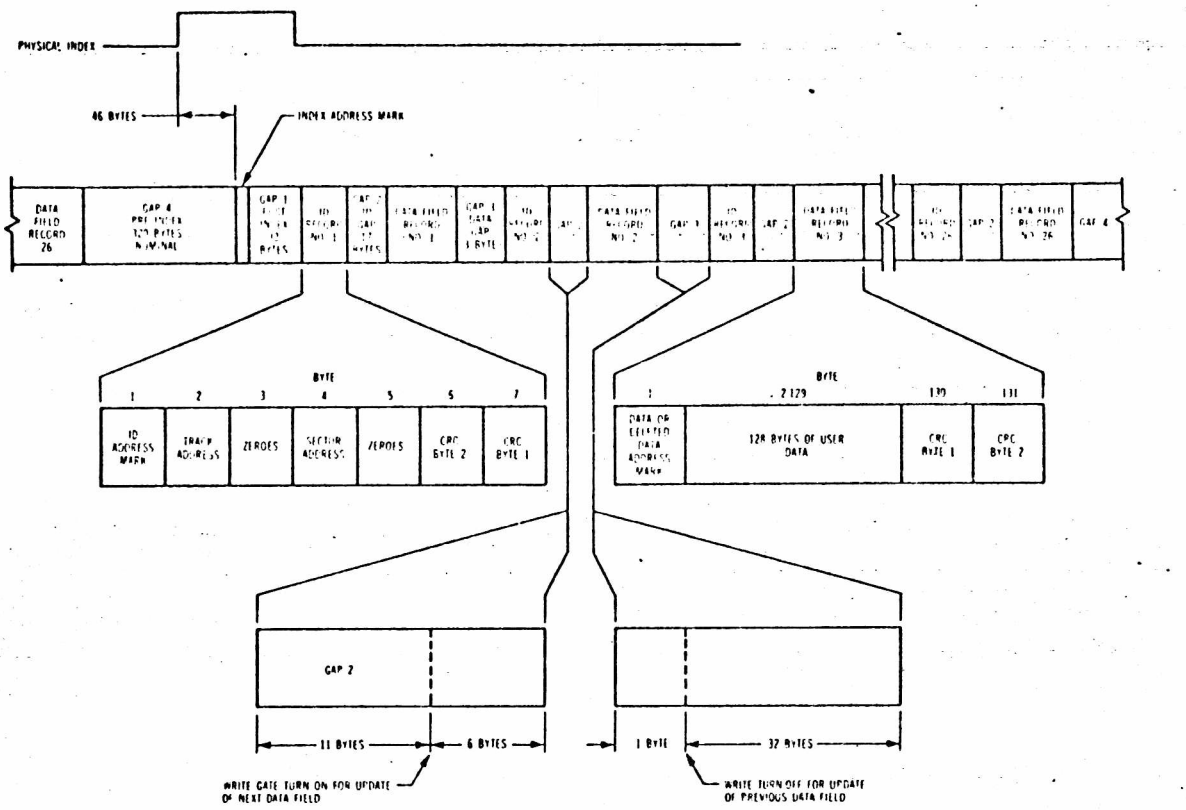

FIG. 13. TRACK FORMAT

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground)*	+15 to −0.3V
Max. Voltage to Any Input With Respect to V_{SS}	+15 to −0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	−55°C to +125°C

OPERATING CHARACTERISTICS (DC)

T_A = 0°C to 70°C, V_{DD} = +12.0V ±.6V, V_{SS} = 0V, V_{CC} = +5V ±.25V

V_{DD} = 10 ma Nominal, V_{CC} = 30 ma Nominal

SYMBOL	CHARACTERISTIC	MIN.	TYPE.	MAX.	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	A	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	A	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6			V	
V_{IL}	Input Low Voltage (All Inputs)			0.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = −100 μA
V_{OL}*	Output Low Voltage			0.45	V	I_O = 1.6 mA

NOTE: Vol ≤ .4V when interfacing with low Power Schottky parts (1_o < 1 ma)
*except WG, where V_{OL} ≤ .5 volts.

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TIMING CHARACTERISTICS

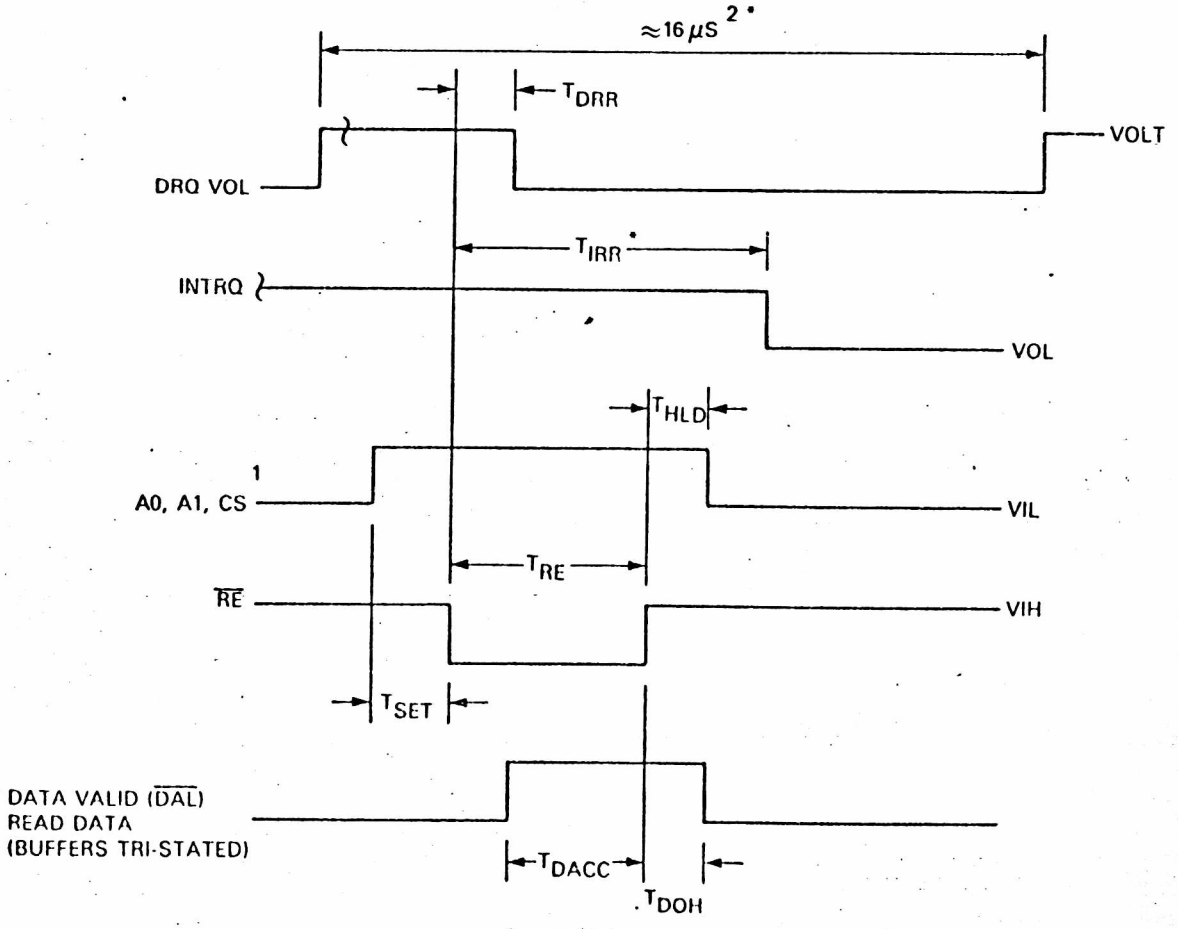
T_A = 0°C to 70°C, V_{DD} = +12V ±.6V, V_{SS} = 0V, V_{CC} = +5 ±.25V

NOTE: Timings are given for 2 MHz Clock. For those timings noted, values will double when chip is operated at 1 MHz.

READ OPERATIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	500			nsec	C_L = 25 pf
TDRR	DRQ Reset from $\overline{RE}$			500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L = 25 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 25 pf

READ ENABLE TIMING



NOTE: 1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED.
2. FOR READ TRACK COMMAND, THIS TIME MAY BE 12* TO 32* μSEC WHEN S·0.
*TIME DOUBLES WHEN CLK·1 MHz.

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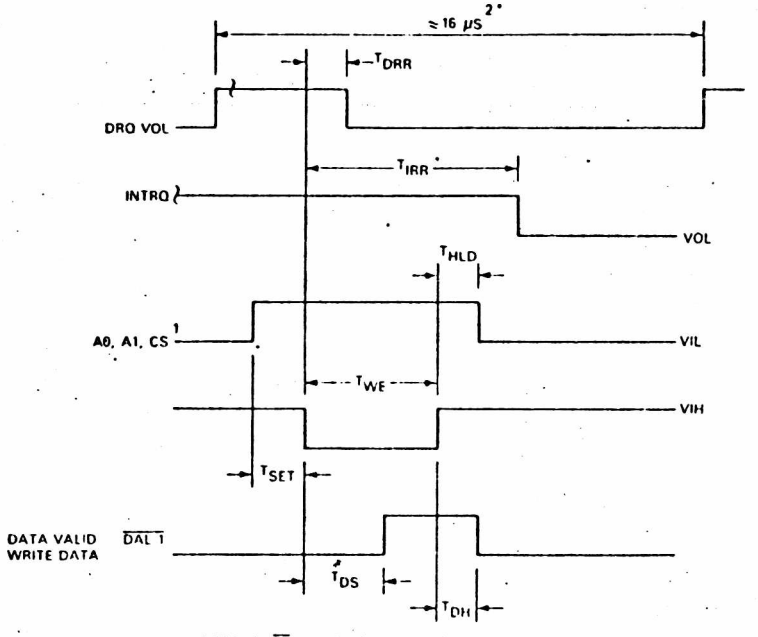
WRITE OPERATIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$			500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	20			nsec	

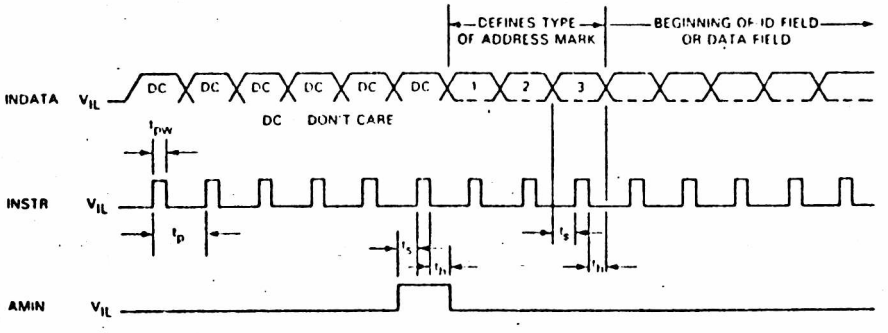
WRITE ENABLE TIMING



NOTE: 1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED.
2. WHEN WRITING DATA INTO SECTOR, TRACK, OR DATA REGISTER, USER CANNOT READ THIS REGISTER UNTIL AT LEAST 8 μSEC AFTER THE RISING EDGE OF WE WHEN WRITING INTO THE COMMAND REGISTER, STATUS IS NOT VALID UNTIL SOME 12 μSEC LATER. THESE TIMES ARE DOUBLED WHEN CLK 1 MHz.

*TIME DOUBLES WHEN CLOCK 1 MHz.

INPUT DATA TIMING



t_{pw} 500 ns ± 50 ns
$t_s \geq 100$ ns
$t_h \geq 300$ ns
$1.2\,\mu s < t_p < 5$ ms

NOTE: INSTR MUST BE FREE RUNNING AS INDICATED BY THE t_p SPECIFICATION. ALSO, THERE MUST BE AT LEAST 2 INSTR PULSES DURING MASTER RESET

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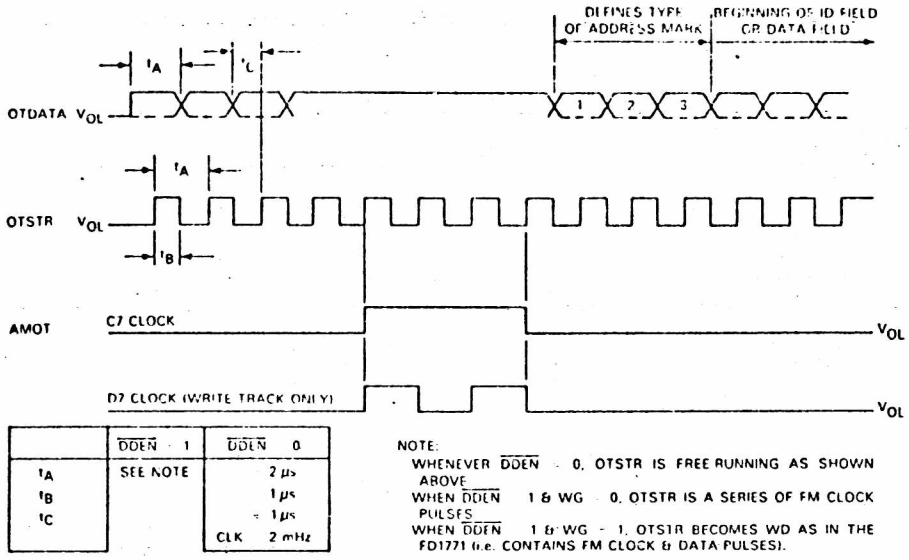
OUTPUT DATA TIMING



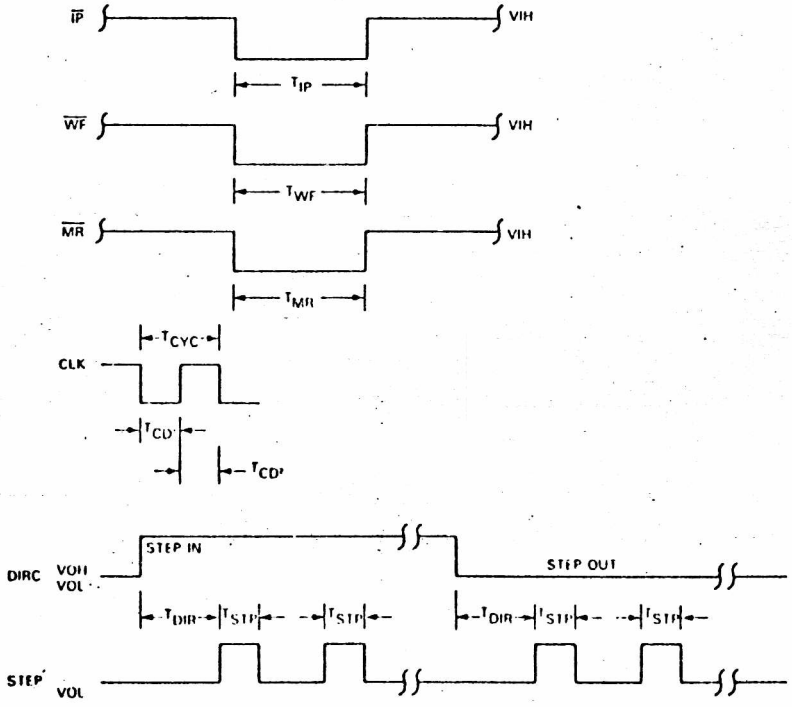
	DDEN = 1	DDEN = 0
t_A	SEE NOTE	2 µs
t_B		1 µs
t_C		1 µs
		CLK 2 mHz

NOTE:
WHENEVER $\overline{DDEN}$ = 0, OTSTR IS FREE RUNNING AS SHOWN ABOVE
WHEN $\overline{DDEN}$ = 1 & WG = 0, OTSTR IS A SERIES OF FM CLOCK PULSES
WHEN $\overline{DDEN}$ = 1 & WG = 1, OTSTR BECOMES WD AS IN THE FD1771 (i.e. CONTAINS FM CLOCK & DATA PULSES).

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty	175			nsec	2 MHz ±1% See Note
TCD_2	Clock Duty	210			nsec	
TSTP	Step Pulse Output	.2000			nsec	These times doubled when CLK = 1 MHz
TDIR	Dir Setup to Step	12			µsec	
TMR	Master Reset Pulse Width	5			µsec	
TIP	Index Pulse Width	5			µsec	
TWF	Write Fault Pulse Width	5			µsec	

MISCELLANEOUS TIMING



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PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V
40		V_{DD}	+12V
19	MASTER RESET	$\overline{MR}$	• A logic low on this input resets the device and clears the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a Restore Command is executed, regardless of the state of the Ready signal from the drive.
COMPUTER INTERFACE:			
7-14	DATA ACCESS LINES	$\overline{DAL0}$-$\overline{DAL7}$	• Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{WE}$ or a transmitter enabled by $\overline{RE}$.
3	CHIP SELECT	$\overline{CS}$	• A logic low on this input selects the chip and enables computer communication with the device.
5,6	REGISTER SELECT LINES	A0,A1	• These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control:

A1	A0	$\overline{RE}$	$\overline{WE}$
0	0	Status Reg	Command Reg
0	1	Track Reg	Track Reg
1	0	Sector Reg	Sector Reg
1	1	Data Reg	Data Reg

4	READ ENABLE	$\overline{RE}$	• A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
2	WRITE ENABLE	$\overline{WE}$	• A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
38	DATA REQUEST	DRQ	• This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	• This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register. Use 10K pull-up resistor to +5.
24	CLOCK	CLK	• This input requires a free-running square wave clock for internal timing reference.
FLOPPY DISK INTERFACE:			
25	ADDRESS MARK DETECT IN	AMIN	• Indicates to the FD1781 that an address mark has been detected. The FD1781 assumes the next three data bits defines the type of address mark encountered.
26	INPUT STROBE	INSTR	• Indicates that INDATA is VALID.
27	INPUT DATA	INDATA	The external data recovery circuits present INDATA as an input to the FD1781. INDATA must be valid when INSTR is active, see timing.
31	OUTPUT DATA	OTDATA	• The FD1781 presents output data and is valid when OTSTR is active.

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28 23	HEAD LOAD HEAD LOAD TIMING	HLD HLT	• The HLD output controls the loading of the Read-Write head against the media the HLT input is sampled every 10 nsec. When a logic high is sampled on the HLT input the head is assumed to be engaged.
15	STEP	STEP	• Step and direction motor control. The step output contains a 2 μsec high signal for each step and the direction output is active high when stepping; active low when stepping out.
16	DIRECTION	DIRC	
17	OUTPUT STROBE	OTSTR	• OTSTR when active indicates when the Output data is valid. The leading edge of OTSTR is centered about the data. (See timing) OTSTR becomes Write Data (WD) when DDEN = 1.
18	ADDRESS MARK OUT	AMOT	• AMOT when active informs the external data recovery circuits to write a unique data mark in double density mode. AMOT is valid for three data bits if CLK mark = C7.
29	TRACK GREATER THAN 43	TG43	• This output informs the drive that the Read-Write head is positioned between track 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	• This output is made valid when writing is to be performed on the diskette.
32	READY	READY	• This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$	$\overline{\text{WF}}$	• This input detects writing faults indications from the drive. When WG = 1 and WF goes low the current Write command is terminated and the Write Fault status bit is set. The WF input should be made inactive (high) when WG becomes inactive.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	• This input informs the FD1781 that the Read-Write head is positioned over Track 00 when a logic low.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	• Input, when low for a minimum of 10 μsec, informs the FD1781 when an index mark is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	• This input is sampled whenever a Write Command is received. A logic low terminated the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	• This pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	• This input is used for testing purposes only and should be tied to +5V or left open by the user.

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

WESTERN DIGITAL
3128 RED HILL AVENUE, BOX 2180
NEWPORT BEACH, CALIFORNIA 92663
(714) 557-3550 TWX 910-595-1139

SMC Microsystems Corporation
35 Marcus Boulevard
Hauppauge, New York 11787
(516) 273-3100
TWX: 510-227-8898

A Standard Microsystems Company

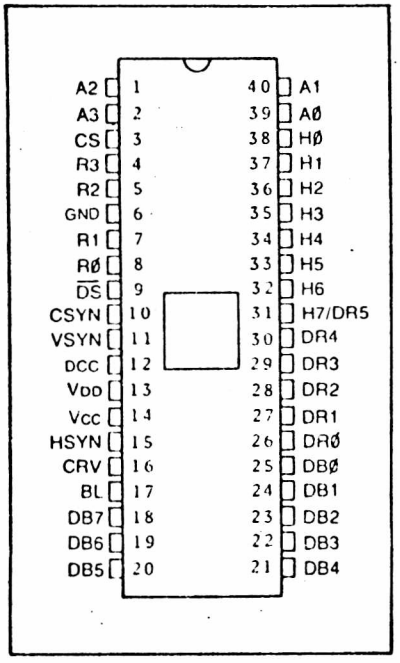
APPENDIX J

CRT Video Timer-Controller VTAC

FEATURES

- ☐ Fully Programmable Display Format
  - Characters per data row (1-200)
  - Data rows per frame (1-64)
  - Raster scans per data row (1-16)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (256-1023)
  - "Front Porch"
  - Sync Width
  - "Back Porch"
  - Interlace/Non-Interlace
  - Vertical Blanking
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync
  - Blanking
  - Cursor coincidence
- ☐ Programmed via:
  - Processor data bus
  - External PROM
  - Mask Option ROM
- ☐ Standard or Non-Standard CRT Monitor Compatible
- ☐ Refresh Rate: 60Hz, 50Hz,...
- ☐ Scrolling
  - Single Line
  - Multi-Line
- ☐ Cursor Position Registers
- ☐ Character Format: 5x7, 7x9,...
- ☐ Programmable Vertical Data Positioning

PIN CONFIGURATION



- ☐ Split-Screen Applications
  - Horizontal
  - Vertical
  - Programmable Wipes
- ☐ External Video Sync-Lock
- ☐ TTL Compatibility
- ☐ BUS Oriented
- ☐ High Speed Operation
- ☐ COPLAMOS® N-Channel Silicon Gate Technology

General Description

The CRT Video Timer-Controller Chip (VTAC) is a user programmable 40-pin COPLAMOS® n channel MOS/LSI device containing the logic functions required to generate all the timing signals for the presentation and formatting of interlaced and non-interlaced video data on a standard or non-standard CRT monitor.

With the exception of the dot counter, which may be clocked at a video frequency above 25 MHz and therefore not recommended for MOS implementation, all frame formatting, such as horizontal, vertical, and composite sync, characters per data row, data rows per frame, and raster scans per data row and per frame are totally user programmable. The data row counter has been designed to facilitate scrolling.

Programming is effected by loading seven 8 bit control registers directly off an 8 bit bidirectional data bus. Four register address lines and a chip select line provide complete microprocessor compatibility for program controlled set up. The device can be "self loaded" via an external PROM tied on the data bus as described in the OPERATION section. Formatting can also be programmed by a single mask option.

In addition to the seven control registers two additional registers are provided to store the cursor character and data row addresses for generation of the cursor video signal. The contents of these two registers can also be read out onto the bus for update by the program.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}= +5V±5%, V_{DD}= +12V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	Vcc−1.5		Vcc	V	
OUTPUT VOLTAGE LEVELS					
Low Level—V_{OL} for RØ-3			0.4	V	I_{OL} = 3.2ma
Low Level—V_{OL} all others			0.4	V	I_{OL} = 1.6ma
High Level—V_{OH} for RØ-3	2.4				I_{OH} = 80μa
High Level—V_{OH} all others	2.4				I_{OH} = 40μa
INPUT CURRENT					
Low Level, I_{IL}					
High Level, I_{IH}					
INPUT CAPACITANCE					
Data Bus, C_{IN}		10		pf	
Clock, C_{IN}		25		pf	
All other, C_{IN}		10		pf	
DATA BUS LEAKAGE in INPUT MODE					
I_{DB}					
I_{DB}					
POWER SUPPLY CURRENT					
I_{CC}		80		ma	
I_{DD}		40		ma	
A.C. CHARACTERISTICS					T_A = 25°C
DOT COUNTER CARRY					
frequency	0.2	4.0		MHz	Figure 1
PW_H	35			ns	Figure 1
PW_L	190			ns	Figure 1
t_r, t_f		10		ns	Figure 1
DATA STROBE					
$PW_{\overline{DS}}$		150		ns	Figure 2
ADDRESS, CHIP SELECT					
Set-up time		100		ns	Figure 2
Hold time		50		ns	Figure 2
DATA BUS—LOADING					
Set-up time		100		ns	Figure 2
Hold time		75		ns	Figure 2
DATA BUS—READING					
T_{DEL2}		100		ns	Figure 2, CL=50pf
OUTPUTS: HØ-7, HS, VS, BL, CRV, CS-T_{DEL1}		100		ns	Figure 1, CL=20pf
OUTPUTS: RØ-3, DRØ-5					
T_{DEL3}		1.0		μs	Figure 3, CL=20pf

Restrictions

1. Only one pin is available for strobing data into the device via the data bus. The cursor X and Y coordinates are therefore loaded into the chip by presenting one set of addresses and outputed by presenting a different set of addresses. Therefore the standard WRITE and READ control signals from most microprocessors must be "NORed" externally to present a single strobe ($\overline{DS}$) signal to the device.

2. An even number of scan lines per character row must be programmed in interlace mode. This is again due to pin count limitations which require that the least significant bit of the scan counter serve as the odd/even field indicator.

3. In interlaced mode the total number of character slots assigned to the horizontal scan must be even to insure that vertical sync occurs precisely between horizontal sync pulses.

Operation

The design philosophy employed was to allow the device to interface effectively with either a microprocessor based or hardwire logic system. The device is programmed by the user in one of two ways; via the processor data bus as part of the system initialization routine, or during power up via a PROM tied on the data bus and addressed directly by the Row Select outputs of the chip. (See figure 4). Seven 8 bit words are required to fully program the chip. Bit assignments for these words are shown in Table 1. The information contained in these seven words consists of the following:

Horizontal Formatting:

Characters/Data Row	A 3 bit code providing 8 mask programmable character lengths from 20 to 132. The standard device will be masked for the following character lengths; 20, 32, 40, 64, 72, 80, 96, and 132.
Horizontal Sync Delay	3 bits assigned providing up to 8 character times for generation of "front porch".
Horizontal Sync Width	4 bits assigned providing up to 16 character times for generation of horizontal sync width.
Horizontal Line Count	8 bits assigned providing up to 256 character times for total horizontal formatting.
Skew Bits	A 2 bit code providing from a 0 to 2 character skew (delay) between the horizontal address counter and the horizontal blank and sync signals to allow for retiming of video data prior to generation of composite video signal. The Cursor Video signal is also skewed as a function of this code.

Vertical Formatting:

Interlaced/Non-interlaced	This bit provides for data presentation with odd/even field formatting for interlaced systems. It modifies the vertical timing counters as described below. A logic 1 establishes the interlace mode.
Scans/Frame	8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. 1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields. Range = 513 to 1023 scans/frame, odd counts only. 2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011). Range = 256 to 766 scans/frame, even counts only. In either mode, vertical sync width is fixed at three horizontal scans (≡ 3H).
Vertical Data Start	8 bits defining the number of raster scans from the leading edge of vertical sync until the start of display data. At this raster scan the data row counter is set to the data row address at the top of the page.
Data Rows/Frame	6 bits assigned providing up to 64 data rows per frame.
Last Data Row	6 bits to allow up or down scrolling via a preload defining the count of the last displayed data row.
Scans/Data Row	4 bits assigned providing up to 16 scan lines per data row.

Additional Features

Device Initialization:

Under microprocessor control—The device can be reset under system or program control by presenting a 1Ø1Ø address on A3-Ø. The device will remain reset at the top of the even field page until a start command is executed by presenting a 111Ø address on A3-Ø.

Via "Self Loading"—In a non-processor environment, the self loading sequence is effected by presenting and holding the 1111 address on A3-Ø, and is initiated by the receipt of the strobe pulse ($\overline{DS}$). The 1111 address should be maintained long enough to insure that all seven registers have been loaded (in most applications under one millisecond). The timing sequence will begin one line scan after the 1111 address is removed. In processor based systems, self loading is initiated by presenting the Ø111 address to the device. Self loading is terminated by presenting the start command to the device which also initiates the timing chain.

Scrolling—In addition to the Register 6 storage of the last displayed data row a "scroll" command (address 1Ø11) presented to the device will increment the first displayed data row count to facilitate up scrolling in certain applications.

Description of Pin Functions

Pin No.	Symbol	Name	Input/ Output	Function
25-18	DBØ-7	Data Bus	I/O	Data bus. Input bus for control words from microprocessor or PROM. Bidirectional bus for cursor address.
3	CS	Chip Select	I	Signals chip that it is being addressed
39, 40, 1, 2	AØ-3	Register Address	I	Register address bits for selecting one of seven control registers or either of the cursor address registers
9	$\overline{DS}$	Data Strobe	I	Strobes DBØ-7 into the appropriate register or outputs the cursor character address or cursor line address onto the data bus
12	DCC	DOT Counter Carry	I	Carry from off chip dot counter establishing basic character clock rate. Character clock.
38-32	HØ-6	Character Counter Outputs	O	Character counter outputs.
7, 5, 4	R1-3	Scan Counter Outputs	O	Three most significant bits of the Scan Counter; row select inputs to character generator.
31	H7/DR5	H7/DR5	O	Pin definition is user programmable. Output is MSB of Character Counter if horizontal line count (REG.Ø) is ≥128; otherwise output is MSB of Data Row Counter.
8	RØ	Scan Counter LSB (Odd/Even Field)	O	Least significant bit of the scan counter. In interlaced mode this bit defines the odd or even field. in this way, odd scan lines of the character font are selected during the odd field and even scans during the even field.
26-30	DRØ-4	Data Row Counter Outputs	O	Data Row counter outputs.
17	BL	Blank	O	Defines non active portion of horizontal and vertical scans.
15	HSYN	Horizontal Sync	O	Initiates horizontal retrace.
11	VSYN	Vertical Sync	O	Initiates vertical retrace.
10	CSYN	Composite Sync	O	Active in non-interlaced mode only. Provides a true RS-170 composite sync waveform.
16	CRV	Cursor Video	O	Defines cursor location in data field.
14	Vcc	Power Supply	PS	+5 volt Power Supply
13	VDD	Power Supply	PS	+12 volt Power Supply

Timing Diagrams

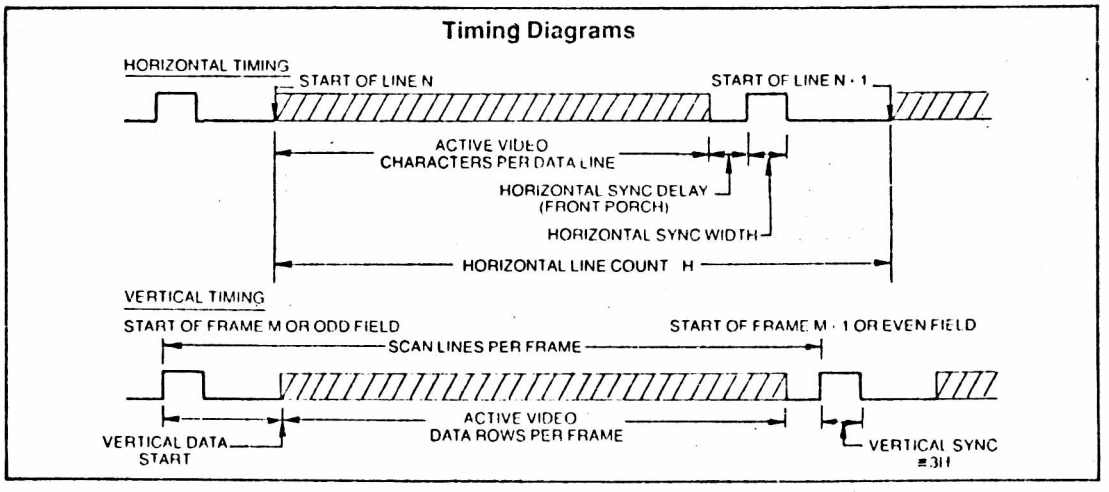
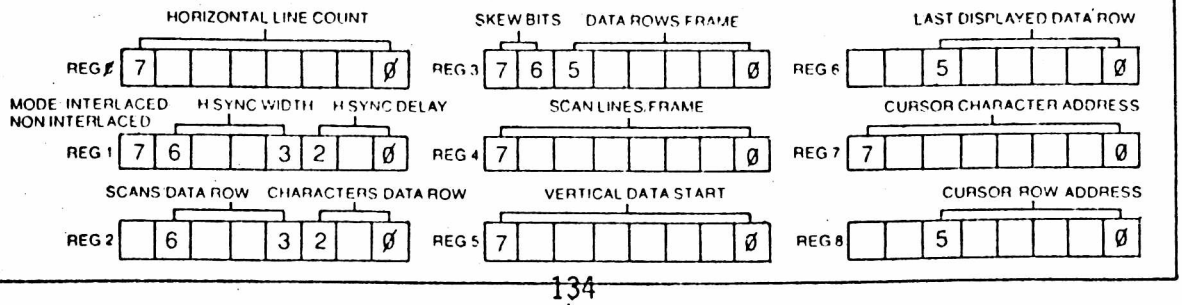


TABLE 1

BIT ASSIGNMENT CHART



Register Selects/Command Codes

A3	A2	A1	AØ	Select/Command	Description
0	0	0	0	Load Control Register Ø	See Table 1
0	0	0	1	Load Control Register 1	
0	0	1	0	Load Control Register 2	
0	0	1	1	Load Control Register 3	
0	1	0	0	Load Control Register 4	
0	1	0	1	Load Control Register 5	
0	1	1	0	Load Control Register 6	
0	1	1	1	Processor Self Load	Command from processor instructing CRT 5027 to enter Self Load Mode
1	0	0	0	Read Cursor Line Address	
1	0	0	1	Read Cursor Character Address	
1	0	1	0	Reset	Resets timing chain to top left of page. Reset is latched on chip by $\overline{DS}$ and counters are held until released by start command.
1	0	1	1	Up Scroll	Increments address of first displayed data row on page. ie; prior to receipt of scroll command—top line = 0, bottom line = 23. After receipt of Scroll Command—top line = 1, bottom line = 0.
1	1	0	0	Load Cursor Character Address*	
1	1	0	1	Load Cursor Line Address*	
1	1	1	0	Start Timing Chain	Receipt of this command after a Reset or Processor Self Load command will release the timing chain approximately one scan line later. In applications requiring synchronous operation of more than one CRT 5027 the dot counter carry should be held low during the $\overline{DS}$ for this command.
1	1	1	1	Non-Processor Self Load	Device will begin self load via PROM when $\overline{DS}$ goes low. The 1111 command should be maintained on A3-Ø long enough to guarantee self load. (Scan counter should cycle through at least once). Self load is automatically terminated and timing chain initiated when the all "1's" condition is removed, independent of $\overline{DS}$. For synchronous operation of more than one CRT 5027, the Dot Counter Carry should be held low when this command is removed.

*NOTE: During Self-Load, the Cursor Character Address Register (REG 7) and the Cursor Row Address Register (REG 8) are enabled during states Ø111 and 1ØØØ of the R3-RØ Scan Counter outputs respectively. Therefore, Cursor data in the PROM should be stored at these addresses.

FIGURE 1 VIDEO TIMING

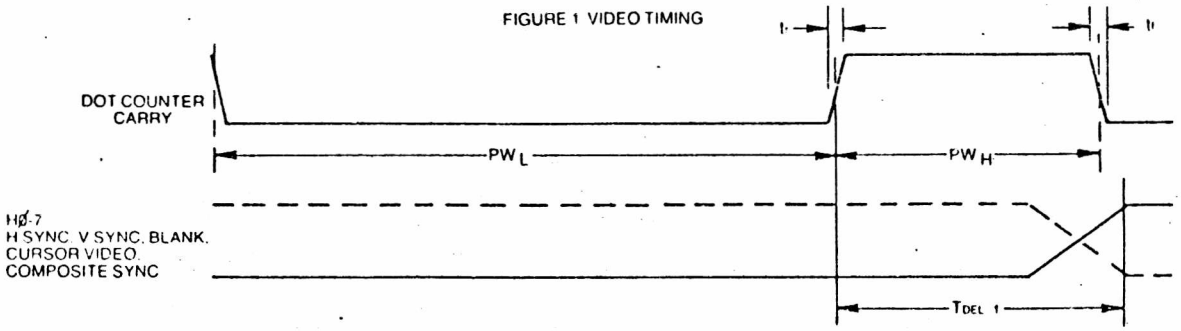


FIGURE 2 LOAD/READ TIMING

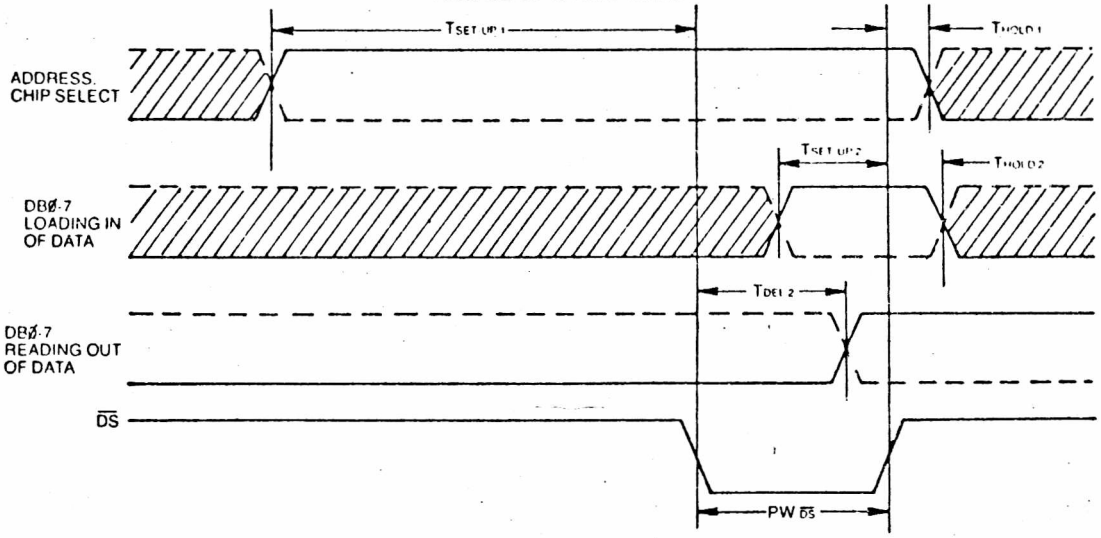


FIGURE 3 SCAN AND DATA ROW COUNTER TIMING

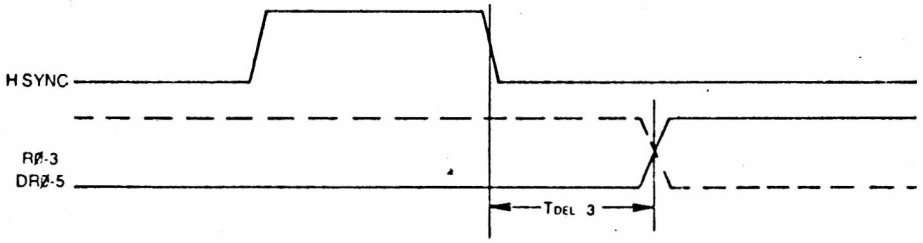
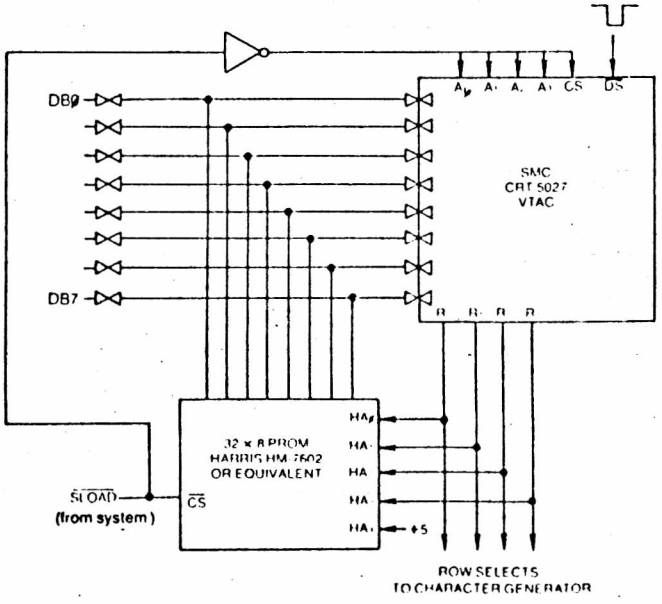
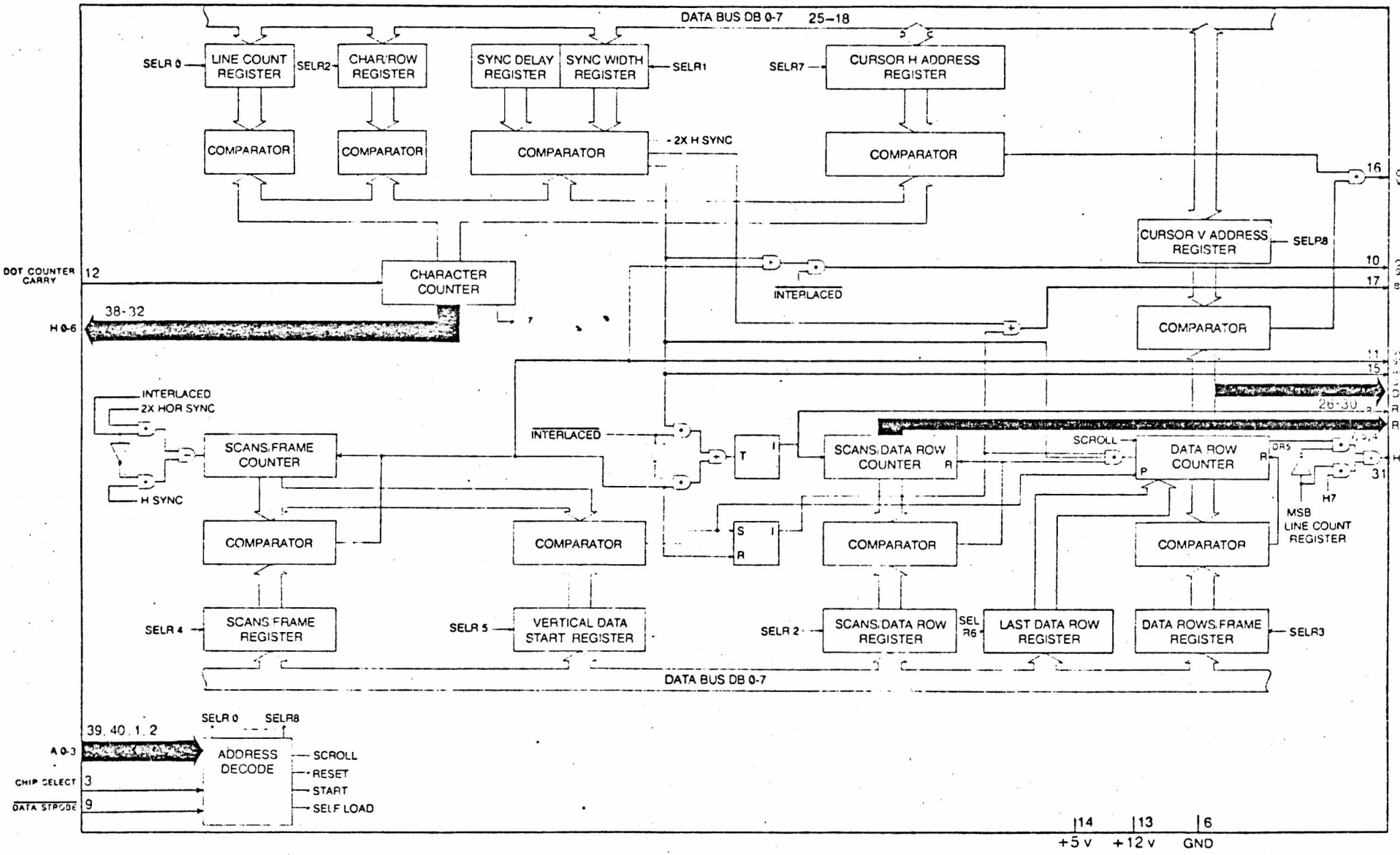


Figure 4. SELF LOADING SCHEME FOR CRT 5027 SET-UP





BLOCK DIAGRAM

CRT 5027 Control Registers Programming Chart

Horizontal Line Count: Tctal Characters/Line = N+1, N=0 to 255 (DBØ=LSB)

Characters/Data Row:

DB2	DB1	DBØ		
0	0	0	= 20	Active Characters/Data Row
0	0	1	= 32	
0	1	0	= 40	
0	1	1	= 64	
1	0	0	= 72	
1	0	1	= 80	
1	1	0	= 96	
1	1	1	= 132	

Horizontal Sync Delay: =N, from 1 to 7 character times (DBØ=LSB) (N=0 Disallowed)

Horizontal Sync Width: =N, from 1 to 15 character times (DB3=LSB) (N=0 Disallowed)

Skew Bits

DB6	DB7	Sync/Blank Delay (Character Times)	Cursor Delay
0	0	0	0
0	1	1	0
1	0	2	1
1	1	2	2

Scans/Frame

8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. (DBØ=LSB)

1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields.
Range = 513 to 1023 scans/frame, odd counts only.

2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011).
Range = 256 to 766 scans/frame, even counts only.

In either mode, vertical sync width is fixed at three horizontal scans (≡3H).

Vertical Data Start: N= number of raster lines delay after leading edge of vertical sync of vertical start position. (DBØ=LSB)

Data Rows/Frame: Number of data rows = N+1, N=0 to 63 (DBØ=LSB)

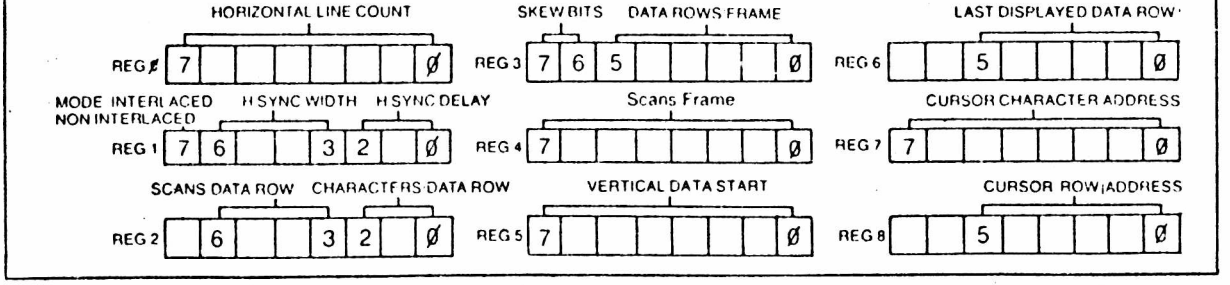
Last Data Row: N= Address of last displayed data row, N=0 to 63, ie; for 24 data rows, program N=23. (DBØ=LSB)

Scans/Data Row: =N+1, N=0 to 15 (DB3=LSB)

Mode: DB7=1 establishes interlace

TABLE 1

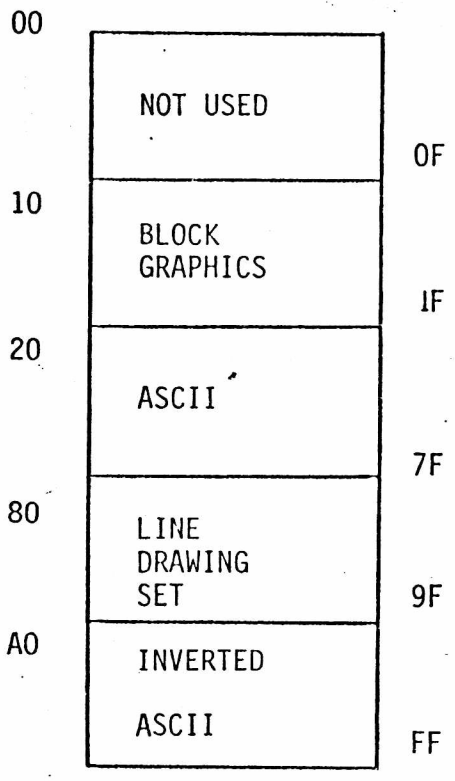
BIT ASSIGNMENT CHART



APPENDIX K

Video Code Definitions

The Video Character ROM is broken up into four basic areas: Block Graphics, Standard ASCII, a Line Drawing set, and Inverted ASCII. This is depicted with address boundaries.



Video ASCII Code Definitions

8 Bit	Code	Definition	8 Bit	Code	Definition
0000	0000	Not Used	0011	0000	0
0000	0001	Not Used	0011	0001	1
0000	0010	Not Used	0011	0010	2
0000	0011	Not Used	0011	0011	3
0000	0100	Not Used	0011	0100	4
0000	0101	Not Used	0011	0101	5
0000	0110	Not Used	0011	0111	7
0000	0111	Not Used	0011	1000	8
0000	1000	Not Used	0011	1001	9
0000	1001	Not Used	0011	1010	:
0000	1010	Not Used	0011	1011	;
0000	1011	Not Used	0011	1100	
0000	1100	Not Used	0011	1101	=
0000	1101	Not Used	0011	1110	
0000	1110	Not Used	0011	1111	?
0000	1111	Not Used	0011	0000	@
0001	0000	Block Graphics	0100	0000	A
0001	0001	Block Graphics	0100	0010	B
0001	0010	Block Graphics	0100	0011	C
0001	0011	Block Graphics	0100	0100	D
0001	0100	Block Graphics	0100	0101	E
0001	0101	Block Graphics	0100	0110	F
0001	0110	Block Graphics	0100	0111	G
0001	0111	Block Graphics	0100	1000	H
0001	1000	Block Graphics	0100	1001	I
0001	1001	Block Graphics	0100	1010	J
0001	1010	Block Graphics	0100	1011	K
0001	1011	Block Graphics	0100	1100	L
0001	1100	Block Graphics	0100	1101	M
0001	1101	Block Graphics	0100	1110	N
0001	1110	Block Graphics	0100	1111	O
0001	1111	Block Graphics	0101	0000	P
0010	0000	Space	0101	0001	Q
0010	0001	!	0101	0010	R
0010	0010	"	0101	0011	S
0010	0011	#	0101	0100	T
0010	0100	$	0101	0101	U
0010	0101	%	0101	0110	V
0010	0111	'	0101	0111	W
0010	1000	(	0101	1000	X
0100	1001	)	0101	1001	Y
0010	1010	*	0101	1010	Z
0010	1011	+	0101	1011	
0010	1100	,	0101	1100	
0010	1101	-	0101	1101	
0010	1110	.	0101	1110	
0010	1111	/	0101	1111	

Video ASCII Code Definitions

8 Bit	Code	Definition	8 Bit	Code	Definition
0110	0000	'	1011	0000	0
0110	0001	a	1011	0001	1
0110	0010	b	1011	0010	2
0110	0011	c	1011	0011	3
0110	0100	d	1011	0100	4
0110	0101	e	1011	0101	5
0110	0110	f	1011	0110	6
0110	1000	h	1011	0111	7
0101	1001	i	1011	1000	8
0101	1010	j	1011	1001	9
0101	1011	k	1011	1010	:
0110	1100	l	1011	1011	;
0110	1100	m	1011	1100	
0110	1110	n	1011	1101	=
0110	1111	o	1011	1110	
0111	0000	p	1011	1111	?
0111	0001	q	1100	0000	@
0111	0010	r	1100	0001	A
0111	0011	s	1100	0010	B
0111	0100	t	1100	0011	C
0111	0101	u	1100	0100	D
0111	0110	v	1100	0101	E
0111	0111	w	1100	0110	F
0111	1000	x	1100	0111	G
0111	1001	y	1100	1000	H
0111	1010	z	1100	1001	I
0111	1011		1100	1010	J
0111	1100		1100	1011	K
0111	1101		1100	1100	L
0111	1110		1100	1101	M
0111	1111	Space	1100	1110	N
1000	0000	Line Drawing Set	1100	1111	O
Thru			1101	0000	P
1001	1111	Line Drawing Set	1101	0001	Q
1010	0000	Space	1101	0010	R
1010	0001	!	1101	0011	S
1010	0010	"	1101	0100	T
1010	0011	#	1101	0101	U
1010	0100	$	1101	0110	V
1010	0101	%	1101	0111	W
1010	0110	&	1101	1000	X
1010	0111	'	1101	1001	Y
1010	1000	(	1101	1010	Z
1010	1001	)	1101	1011	
1010	1010	*	1101	1100	
1010	1011	1101	1101	1101	
1010	1100	,	1101	1110	
1010	1101	-	1101	1111	_
1010	1110	.			
1010	1111	/			

Video ASCII Code Definitions

8 Bit	Code	Definition	8 Bit	Code	Definition
1110	0000	'	1111	0000	p
1110	0001	a	1111	0001	q
1110	0010	b	1111	0010	r
1110	0011	c	1111	0011	s
1110	0100	d	1111	0100	t
1110	0101	e	1111	0101	u
1110	0110	f	1111	0110	v
1110	0111	g	1111	0111	w
1110	1000	h	1111	1000	x
1110	1001	i	1111	1001	y
1110	1010	j	1111	1010	z
1110	1011	k	1111	1011	
1110	1100	l	1111	1100	
1110	1101	m	1111	1101	
1110	1110	n	1111	1110	
1110	11111	o	1111	1111	Space

001 0000 

001 0001 

001 0010 

001 0011 

001 0100 

001 0101 

001 0110 

001 0111 

001 1000 

001 1001 

001 1010 

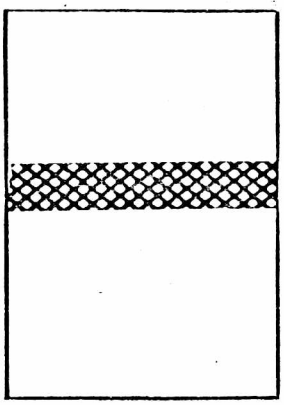
001 1011 

001 1100 

001 1101 

001 1110 

001 1111 



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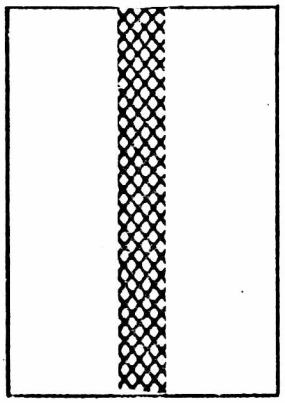

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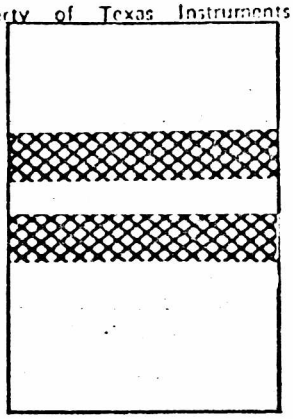

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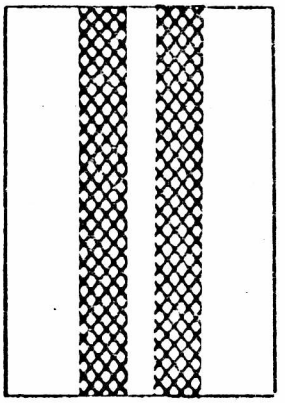

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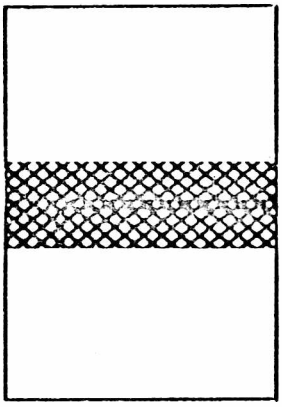

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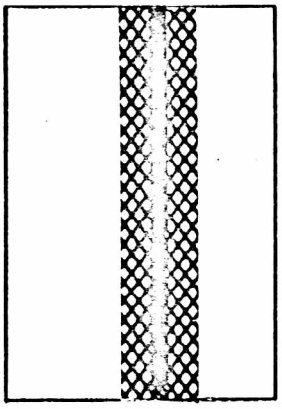

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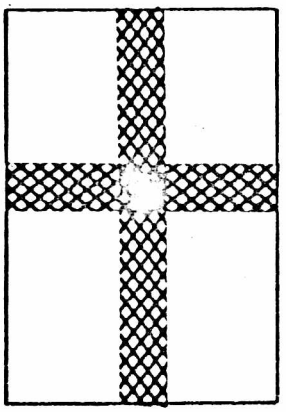

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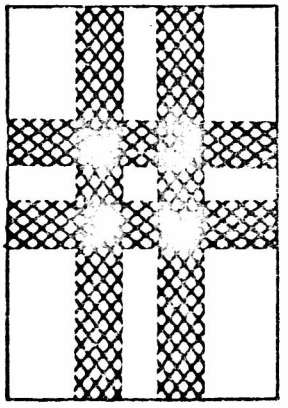

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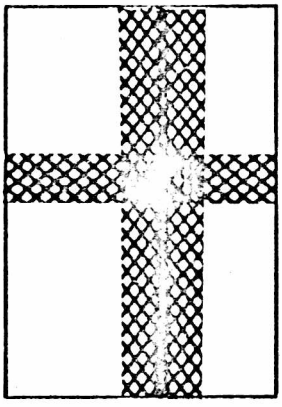

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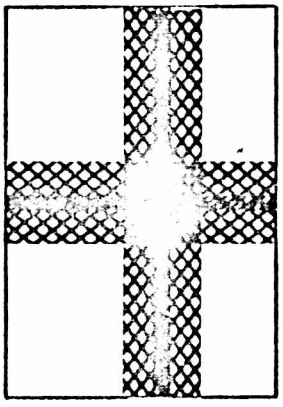

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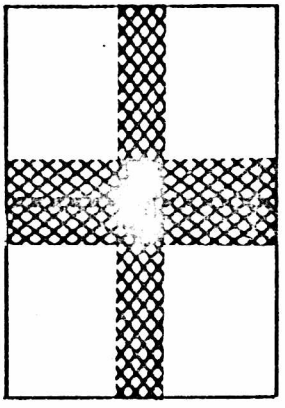

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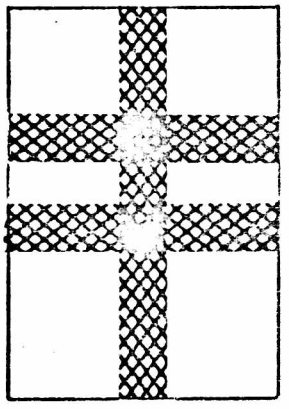

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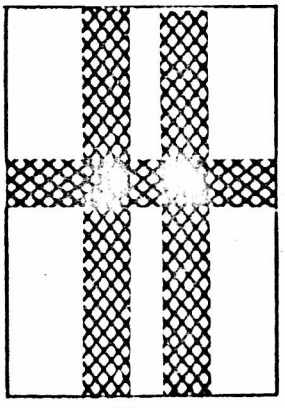

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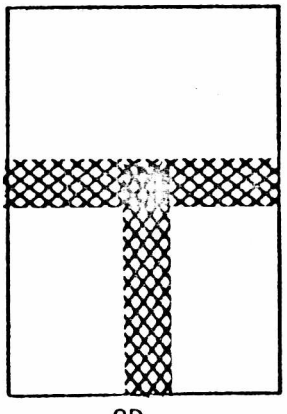

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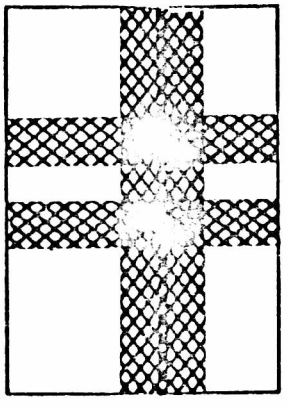

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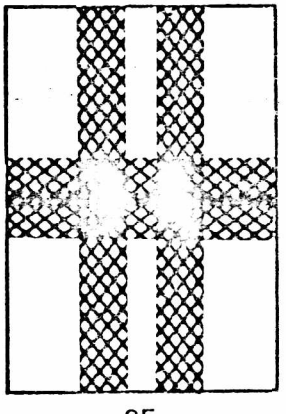

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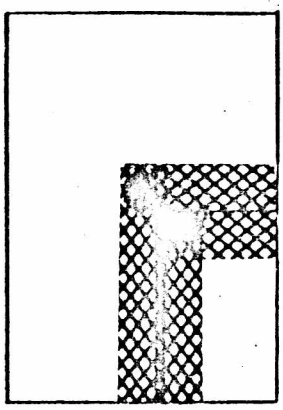

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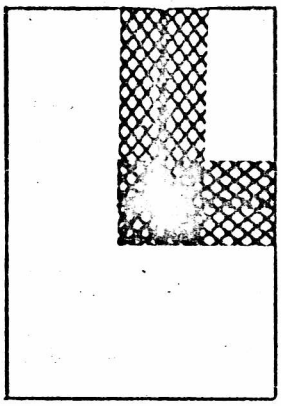

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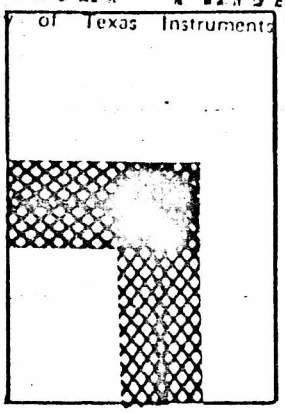

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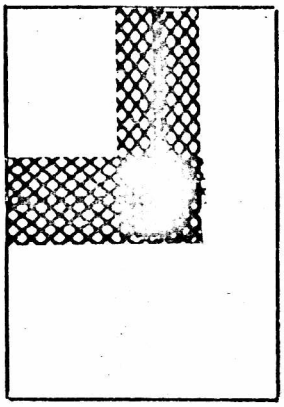

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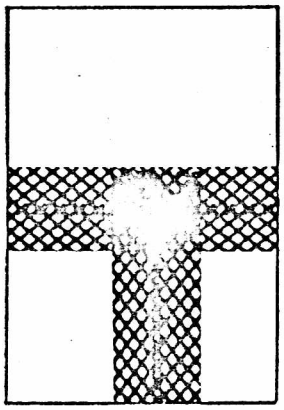

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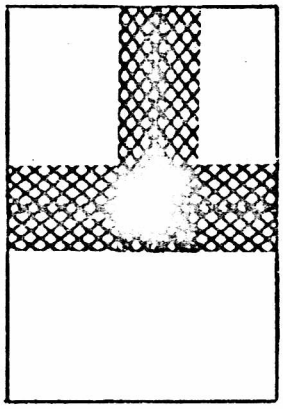

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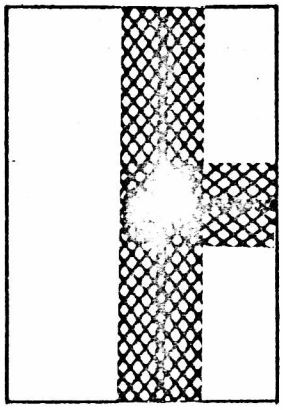

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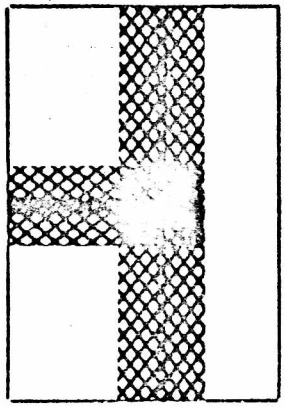

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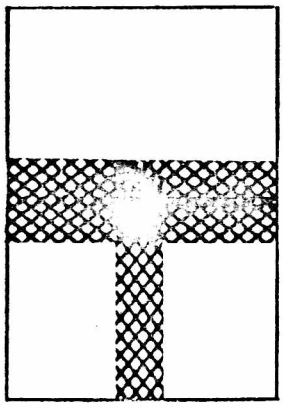

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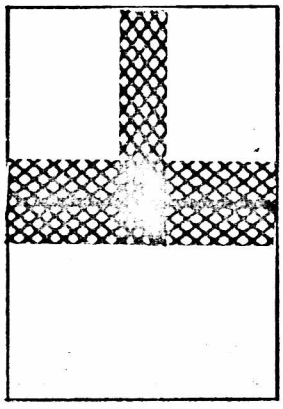

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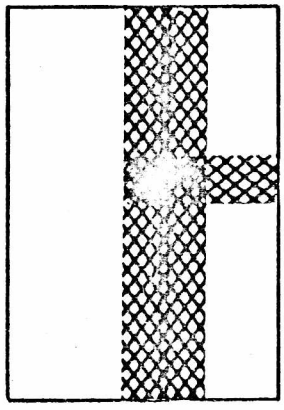

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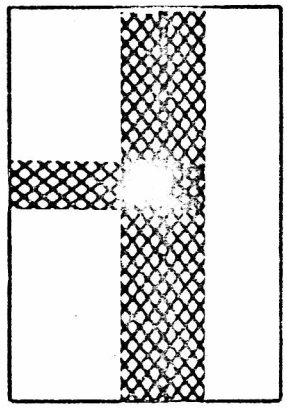

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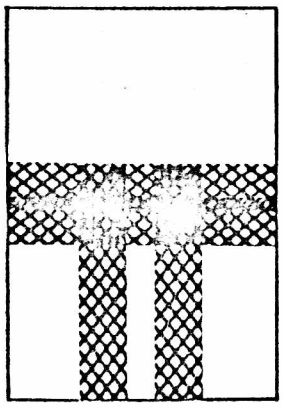

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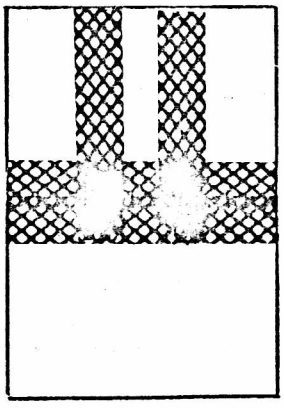

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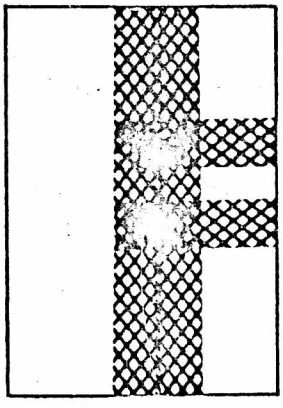

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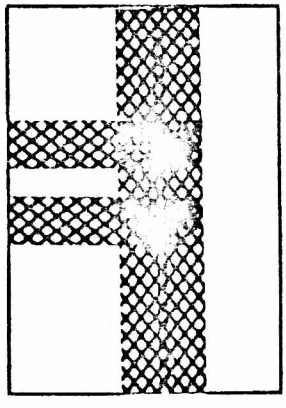

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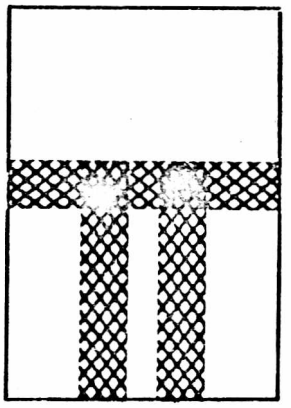

FF

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
	3-500				

APPENDIX L

TMC 0350

SERIALLY ACCESSED ROM

ELECTRICAL SPECIFICATION

SHEET																																	
REV STATUS OF SHEETS	REV																																
	SHEET	1	2	3																													

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ±1°
3 PLACE DECIMAL ± 010
2 PLACE DECIMAL ± 02

IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY

DWN Donna Justice DATE 12/05/77
CHK
ENGR 12-05-77
QA
MNFG
CONTR NO
DESIGN ACTIVITY RELEASE 12/5/77

TEXAS INSTRUMENTS
INCORPORATED
Dallas, Texas

TMC 0350
SERIALLY ACCESSED ROM
ELECTRICAL SPECIFICATION

12-5-77

SIZE		DRAWING NO
A		1501363
SCALE		SHEET 1 of 3

TI 21901

1.0 SCOPE:

THIS DOCUMENT SPECIFIES ELECTRICAL AND MECHANICAL REQUIREMENTS FOR A READ ONLY MEMORY INTEGRATED CIRCUIT DESIGNATED THE TMC 0350. IN CASE OF CONFLICT WITH CITED DOCUMENTS, THIS DOCUMENT PREVAILS.

2.0 APPLICABLE DOCUMENTS:

GENERAL REQUIREMENTS FOR MOS CALCULATOR INTEGRATED CIRCUITS	TI 1500005
TMC 0280 LPC SYNTHESIZER ELECTRICAL SPEC.	TI 1501364
TMC 0350, TMC 0270 LPC SYNTHESIZER/ROM FUNCTIONAL SPEC.	TI 1501362

3.0 PACKAGE:

THE TMC 0350 SHALL BE MOUNTED IN A 28 PIN DUAL IN LINE PLASTIC PACKAGE WITH 0.6" ROW SPACING AND 0.1" PIN CENTER SPACING PIN NAMES AND FUNCTIONS SHALL BE AS FOLLOWS:

PIN	NAME	DIRECTION	FUNCTION
1	V_{DD}	-	DRAIN SUPPLY (-10V NOM)
2	N.C.	-	
3	ADD1	I/O	ADDRESS/DATA 1
4	ADD2	I/O	ADDRESS/DATA 2
5	N.C.	-	
6	ADD4	I/O	ADDRESS/DATA 4
7	ADD8	I/O	ADDRESS/DATA 8
8	N.C.	-	
9	ROM CLK	I	200KHz CLOCK INPUT
10	I_0	I	COMMAND BIT 0
11	I_1	I	COMMAND BIT 1
12			
13	CS	I	SUBSTRATE SUPPLY
14	V_{SS}	-	CHIP SELECT
15-28	N.C.	-	

4.0 ELECTRICAL CHARACTERISTICS:

4.1 ABSOLUTE MAXIMUM RATINGS:

UNLESS OTHERWISE NOTED, ALL VOLTAGES ARE WITH RESPECT TO V_{SS}. EXCEEDING THE LIMITS GIVEN HERE MAY CAUSE PERMANENT DAMAGE TO THE CIRCUIT. THESE ARE STRESS LIMITS ONLY AND FUNCTIONAL OPERATION OF THE CIRCUIT AT THESE OR AT ANY OTHER CONDITION DIFFERENT FROM THESE GIVEN IN THE OPERATION SECTIONS OF THIS SPECIFICATION IS NOT IMPLIED.

	MIN	MAX
V_{DD}	-20V	+0.3V
ALL OTHER PINS APPLIED VOLTAGE	-20V	+0.3V
STORAGE TEMPERATURE		125°C
OPERATING TEMPERATURE		50°C

4.2 OPERATING CHARACTERISTICS AND REQUIREMENTS:

	MIN	MAX
INPUT PINS		
CS, ROM CLK, I_0, I_1, ADD1, 2, 4, 8		
ONE LEVEL	V_{SS}-0.6V	V_{SS}
ZERO LEVEL	V_{DD}	V_{SS}-4.5V
NO PULL DOWNS		
CAPACITANCE		12pf
POWER SUPPLIES		
V_{DD}	-11.0V	-9.0V
I_{DD} (V_{DD}= -10V)		10mA
ROM CLK INPUT (200KHz NOM)		
RISE TIME V_{DD} TO V_{SS}-0.6V;		0.5µs
FALL TIME V_{SS} TO V_{SS}-4.5V;		0.5µs
OUTPUTS		
ADD 1, 2, 4, 8, DATA, STATUS		
RISE TIME V_{DD} TO V_{SS}-0.6V; 240pf LOAD		2.0µs
FALL TIME V_{SS} TO V_{SS}-4.5V; 240pf LOAD		2.0µs
SINK CURRENT V_{OUT}=V_{SS}-4.2V	0.4mA	
SOURCE CURRENT V_{OUT}=V_{SS}-2.0V	100µA	

4.3 STATIC DISCHARGE PROTECTION:

THE INPUTS AND OUTPUTS SHALL BE GUARDED AGAINST ELECTROSTATIC DAMAGE BY STATE OF THE ART PROTECTION DEVICES INCORPORATED ON THE CHIP.

SIZE		DRAWING NO
A		1501363
SCALE	REV	SHEET 3 of 3

TI 22222

```
J=0:P=40
20 FOR I=1 TO 26
Z=I+J
IF Z>26 THEN Z=Z-26
Z=Z+P
!CHR$(Z)9
NEXT I
J=J+1
IF J>26 THEN J=0:P=100-P
GOTO 20
```

$40 = a(60) + b$
$-60 = -a(40) + b$

$-20 = 20a$

$a = -1$

$40 = -60 + b$

$b = 100$