SECTION 1

INTRODUCTION

1.1 PURPOSE

The purpose of these specifications is to document the I/O characteristics of the TI 99/8 Home Computer. These specs are technical in nature, and should allow one to design hardware to function connected to this port.

1.2 GENERAL CONSTRAINTS

The propogation delays inherent in the 99/8 Mapper chip limit the address access time of ROMs to 350 ns or less for modules in an expansion unit connected to the 99/8 by a 4' cable. As decoding is required for the memory chip select, the access time from CS active must be adjusted faster accordingly. The same is true for CRU based logic blocks (TMS9901, TMS2202, etc.) also.

The fundamental problem is that the Mapper chip skews PH3*, MEMEN*, PWE*, and the PAS Address bits with respect to the 99/8 uP CLKOUT. Data is taken on the falling edge of the second CLKOUT of the apparent 2 clock cycle I/O Port (99/8 Physical Address Space...PAS).

An additional constrain existed at an earlier date which required us to maintain a 99/4-99/8 compatible Expansion Box. With the demise of the 1982-82 Expansion Box, this restriction is not necessary, but THAT COMPATIBILITY ALREADY EXISTS IN THE MAPPER CHIP. Unless a Mapper chip revision is made (and none is currently planned), we will still be confined to these useless restrictions.

The full characteristics of the I/O Port will not be known until the Mapper chip is characterized to verify mathematical model values.

SECTION 2

99/8 CHARACTERISTICS

2.1 ADDRESS GENERATION

The 99/8 provides a 24-bit address on a 16-bit bus by multiplexing two 16-bit quantities. The format is as shown below.

```
|W X R O  O O O O  M M M M  M M M M|  (MSAST*)  Word #0
------------------------------------
  W = Write Protect, X = Execute Protect, O = LOW Level,
  R = Read Protect, M = Most Significant 8 Address bits


|L L L L  L L L L  L L L L  L L L L|   (MEMEN*)  Word #1
|----------------------------------|
```

In all probability only the Least significant 8 bits of Word #0 will be of interest to the Logic Designer. Of course, the designer could sense the protect bits, and control logic accordingly. At present, there are no plans in mind to use these bits other than at the chip test level.

Word #0 is guarenteed to be stable on the FALLING EDGE of MSAST*, and is stable such that setup and hold time requirements of a SN74LS273 are met when a SN74LS04 is used to invert MSAST* for clocking the '273. IT IS UP TO THE PERIPHERAL TO SAVE THIS DATA IF IT IS REQUIRED FOR ITS PAS DECODE.

With this scheme the 99/8 has 256 64K memory segments, and the 99/8 Mapper provides BYTE resolution within a segment. The 99/8 Mapper also provides for displacing from one 64K segment into another if desired.

The Least Significant 16 address bits are found in Word #1, and are stable at the time PMEMEN* goes active LOW. They will remain stable over most of the time PMEMEN* is active. What sort of "gap" at the end of PMEMEN* we will have will be determined when a Mapper chip is characterized. In any case, the LS 16 address lines will be stable when PWE* is active (LOW). See the Section on Timing Diagrams for more information.

2.2 SRAM CONTROL

It is highly recommended that the Logic Designer include the term (PDBIN + PWE) in his equations to chip select the SRAM, and to connect PWE* to the READ/WRITE* control of the SRAM. This is termed EARLY WRITE, and is the manner to eleminate data bus conflicts some logic designers perfer to design in.

As was with ROMs and CRU based devices, an address access of no slower than 350 ns should be used.

2.3 DRAM CONTROL

This is the stickiest controller of all, as one must provide for RAS* and CAS*, and then still return data to the 99/8 no later than 350 ns from the falling edge of PMEMEN* while ignoring any address decode glitches. The saving grace for this glitch problem is that if 64K BYTE or bigger increments of 64K BYTEs are used, the space decode will be on the MS 8 bits of the address (which occurs between 50 and 100 ns before PMEMEN* goes active.

It would be considered good design practice to latch the control signal to the W* input of the DRAMs for the entire duration of PMEMEN* for write glitch protection.

2.4 MEMORY ACCESS LENGTH

The 99/8 requires three clock cycles for every PAS access. The Mapper chip suppresses one of these clock cycles from the PAS by delaying PMEMEN* by one clock cycle. This allows for adder settling time, etc., within the Mapper, and for generating the control signal MSAST*. An inherent advantage of this delay is that there can be no successive (back-to-back) accesses, and DRAM refresh could occur in this time if desired.

The Mapper is timed with respect to the uP CLKOUT, and in turn generates a derivative of this (PH3*) as the PAS analog of CLKOUT. PH3* serves the TMS9901 within the 99/8 as well as the PAS peripherals, and was generated for 99/4 peripheral compatibility reasons.

SECTION 3

DEDICATED PAS SPACE

3.1 GENERAL

There are several PAS spaces already committed both within and outside of the 99/8 Console. Functions implemented inside of the 99/8 are not accessable from the 99/8 I/O Port. All are detailed in the following paragraphs.

3.2 99/8 INTERNAL 64K BYTE DRAM

The first 64K BYTE page (PAS = >000000) is decoded and implemented on the 99/8 itself. While this is good for the Console user, it falls well within the "not so very good" class for the peripheral designer if multiple 64K BYTE Blocks are implemented (128K/256K/512K, etc.). The space decode is considerably more tedious if this configuration exists.

If an interface PCB to the new???99/8 Expansion Box included a 64K BYTE DRAM, this problem would be minimized.

All spaces are contiguous in nature unless noted in the individual discussions.

3.3 99/8 COMMAND MODULE SPACE

A 16K BYTE space is decoded and based at >FF6000 on the 99/8 to be used for Solid State Software. As is with the on-board 64K BYTE DRAM, it is not accessable from the I/O Port Bus.

3.4 99/8 CONSOLE ROM SPACE

A 32K BYTE ROM is provided on the 99/8, and is partitioned to have 16K BYTEs in the PAS decoded and based at >FFA000. Two 8K segments are provided to be CRU paged, and to respond in the Peripheral space based at >FF4000. It is not accessable from the

I/O Port.

3.5 PERIPHERAL SPACE

An 8K BYTE block is reserved based at >FF4000 to be used in the paged mode with peripheral DSRs. The 99/8 uses CRU Paging to enable this block. There is no reason why a peripheral DSR could not based at another location that does not conflict with an internal 99/8 function. The 99/8 Operating System does expect RAM to be contiguous starting with the on-board 64K BYTEs.

3.6 INTERRUPT LEVEL SENSE

A two BYTE READ ONLY interrupt status bit sense is included in a 16 byte PAS based at >FFE000. This is to be implemented on the interface PCB that interfaces the Expansion Box with the 99/8. A word MOVE shall access both BYTEs.

This function was included to allow the 99/8 to easily discern which PCB function in the 99/4 Expansion Box was the interrupt source. It is of questionable value considering that we do not have a 99/8 Expansion Box defined at present.

SECTION 4

SIGNAL DEFINITIONS

4.1 GENERAL

The following text describes each signal in the 50 conductor I/O Port. Signals suffixed with "*" indicate an Active LOW state. Others are HIGH True.

"I" indicates an input to the 99/8, "O" indicates an output from the 99/8, and "B" indicates a bidirectional line.

Many signals may be futher clarified by reading the TI TMS9995 uP Data Manual.

4.2 UR5, I

This is the unregulated +5V bus in the 99/4 Expansion Box, and is used by the 99/4 cable to power logic at that end of the connecting cable.

The 99/8 uses this signal to indicate that a 99/4 Expansion Box is connected to it.

4.3 RESET*, B

This is a bidirectional system reset signal. It is driven by the 99/8 for Power Up, when a Command Module is just inserted, and for a Software Reset. It is active LOW. To insure that the 99/8 uP pulse duration is met, RESET* must be held LOW for at least three (3) PH3* clock cycles. It will be a good idea to drive RESET* as a function of the falling edge of PH3*.

This is a line that is pulled up within the 99/8, and drivers there must drive the minimal load within the 99/8 in addition to the cable to the 99/8 Expansion Box and the load in it (if they are connected).

4.4 EXTINT*, I

EXTINT* is an active LOW signal to interrupt the 99/8. Interrupt Level 1 in the 99/8 uP is driven.

4.5 A0 thru A14, O

These HIGH True signals form the Most Significant 15 bits of the 16-bit PAS Bus.

4.6 A15/COUT, O

This is the LSB of the 16-bit PAS Bus if a Memory Cycle is in progress (PMEMEN* is LOW). If PMEMEN* is HIGH, A15/COUT is the CRU Output Data bit.

4.7 PDBIN, O

This is the Data Bus direction indicator for the PAS. If it is HIGH, the data direction is from the I/O Port into the 99/8.

4.8 LOAD*, I

This input to the 99/8 drives a "LOAD" or "NMI" operation in the uP. If not inherently done so, it should be synchronized with respect to the falling edge of PH3*.

4.9 CRUCLK*, O

CRUCLK* is the separated CRU Clock of the 99/8 uP. It is separated as a function of MEMEN*, IAQ/HOLDA, and WE/CRUCLK*.

4.10 PH3*, O

This is the Mapper generated Active LOW Phase 3 Clock needed at one time to maintain 99/4A Peripheral compatibility. The falling edge of PH3* corresponds to the rising edge of the uP CLKOUT, but with Mapper introduced skew.

4.11 PWE*, O

This is the Active LOW Write Enable for the PAS. It is timed the same as that for the TMS9900 WE*, but is skewed by the Mapper chip.

4.12 PMEMEN*, O

PMEMEN* is memory cycle indicator for the PAS. It is LOW True, and is skewed by the Mapper chip from the 99/8 uP MEMEN*.

4.13 CRUIN, I

This signal is CRU Input Data. It is HIGH True.

This is a line that is pulled up within the 99/8, and drivers there must drive the minimal load within the 99/8 in addition to the cable to the 99/8 Expansion Box and the load in it (if they are connected).

4.14 DO thru D7, B

These 8 HIGH True Data lines feed the PAS.

4.15 SCLK, O

SCLK is the 10.7368+ MHz System clock. The falling edge of SCLK is phased to the 99/8 uP, but due to Mapper introduced skew, it is not dependably phased to PH3*.

4.16 IAQ/HDA, O

This is the buffered 99/8 uP IAQ/HOLDA signal.

4.17 MSAST*, O

The falling edge MSAST* indicates that the MS 16 bits of the Mapper are stable on the PAS Address Bus.

4.18 HOLD*, I

This active LOW status signal is used to put the 99/8 uP in the HOLD state. No internal function in the 99/8 is available at the I/O Port, though. It is for future Expansion Box Direct Memory Access use.

This is a line that is pulled up within the 99/8, and drivers there must drive the minimal load within the 99/8 in addition to the cable to the 99/8 Expansion Box and the load in it (if they are connected).

4.19 READY, I

READY is the system READY input to the 99/8. It must by synchronized with respect to the falling edge of PH3*, and due to delays in the Mapper chip, it must be stable one clock cycle before the 99/8 uP recognizes it. That is, it is syncronized on Clock Cycle n, and the uP recognizes it on Clock Cycle n+1.

This is a line that is pulled up within the 99/8, and drivers there must drive the minimal load within the 99/8 in addition to the cable to the 99/8 Expansion Box and the load in it (if they are connected).

4.20 GND

Logic Ground is this function. All due care must be used in connecting these signals to another system. Weak Grounds equate to low merit reviews.

4.21 RDBENA*, I

RDBENA* is a carryover from the 99/4 Expansion Box where it enabled a data bus driver in the 99/4 end of the Expansion Box Cable. It has questionable use at the present date.

4.22 AUDIO IN, B

This is the Audio input to the internal 99/8 Sound Generator chip.

SECTION 5

TIMING DIAGRAMS

5.1 MEMORY

Memory timing for the PAS was designed to emulate that of the TI TMS9900 for 99/4-99/8 compatibility with the same peripheral PCB. The Mapper chip considerably skews these signals, and the result is a considerably shortened actual cycle with respect to the apparent 2 PH3* clock cycle (745 ns base time, less prop and setup times) memory access. Worst case timing will be better known after the Mapper chip has been characterized.

```
Signal
------
         |------------------        ------------------------
MSAST*   |                  |_______|
         |
PAij     |-------------|_Stable--|---------------------------
PMEMEN*, |-----------------------------
PDBIN    |                             |___________________
----------------------------------------------------------------
                       !20ns!20ns! >!  !<  Greater than 0 ns

PMEMEN*, |-----                                    ---------
PDBIN    |     |______________Stable_______________|
         |
PAij     |       |____________Stable_____________|
----------------------------------------------------------------
              >! !<0 ns                          >! !< Unknown

PMEMEN*, |-----                                    ---------
PDBIN    |     |______________Stable_______________|
         |
         |-------------                   ----------------
PWE*     |             |___________________|
----------------------------------------------------------------
              >! 186 ns!<   IDEAL VALUES  >! 186 ns!
```

5.2 CRU

```
PAij     !       !____________Stable______________!
         !---------------                  -----------------
CRUCLK*  !             !____________________!
------------------------------------------------------------------
                >!     !< Unknown Values  >!      !<
```

SECTION 6

DMAC

6.1 GENERAL

Direct Memory Access shall be allowed within the 99/8 Expansion Box, but this concept will not allow an outside function to access data inside of the 99/8. If the 99/8 Expansion Box, when defined, accepts standard sized 99/4 Expansion Bsox PCBs, then the signal "AMB.A" shall be driven to affect a DMA condition to the Expansion Box Bus Drivers. It shall be the responsibility of DMA requestor to drive HOLD*, and sense IAQ/HDA and MEMEN*.