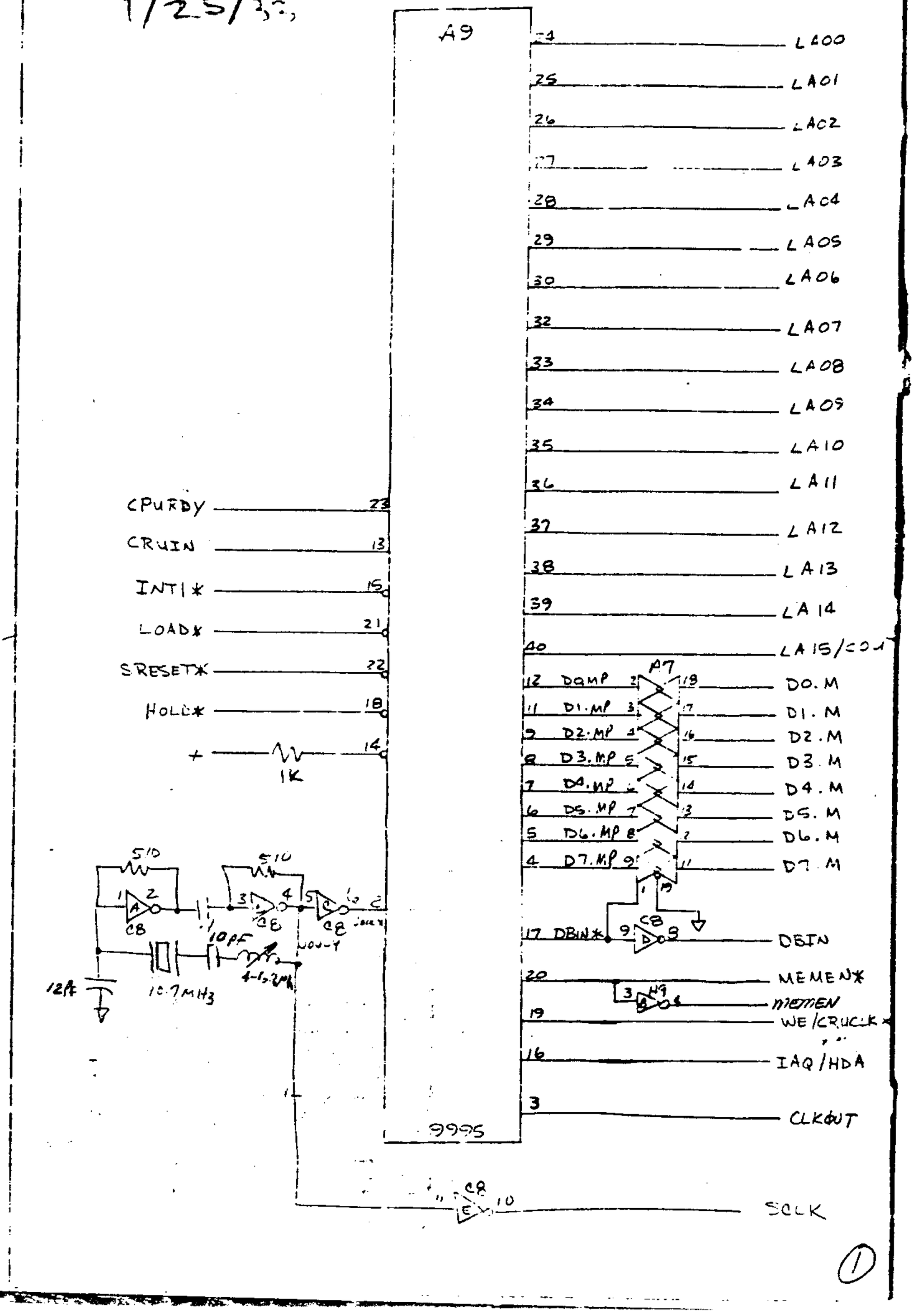
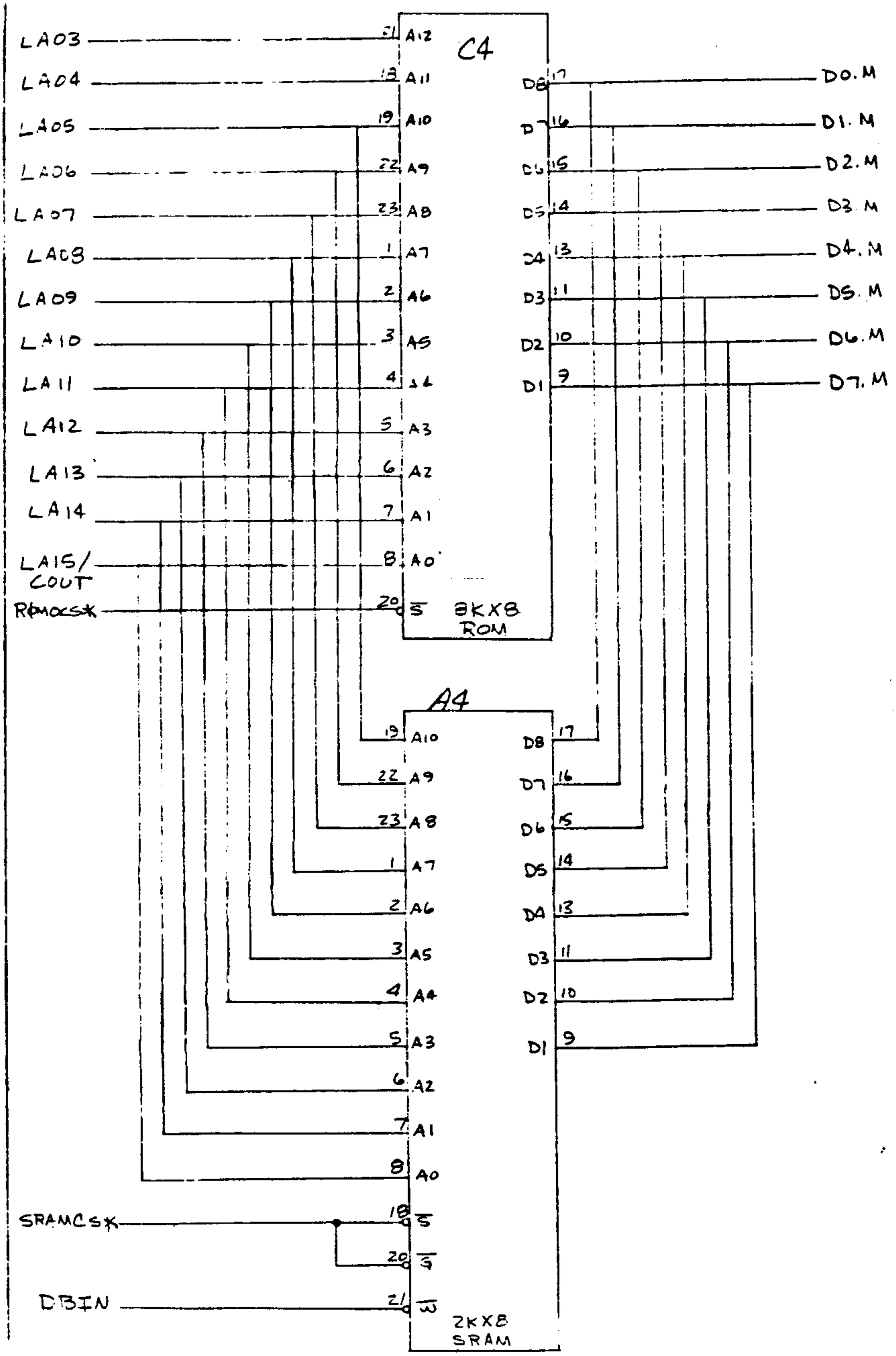
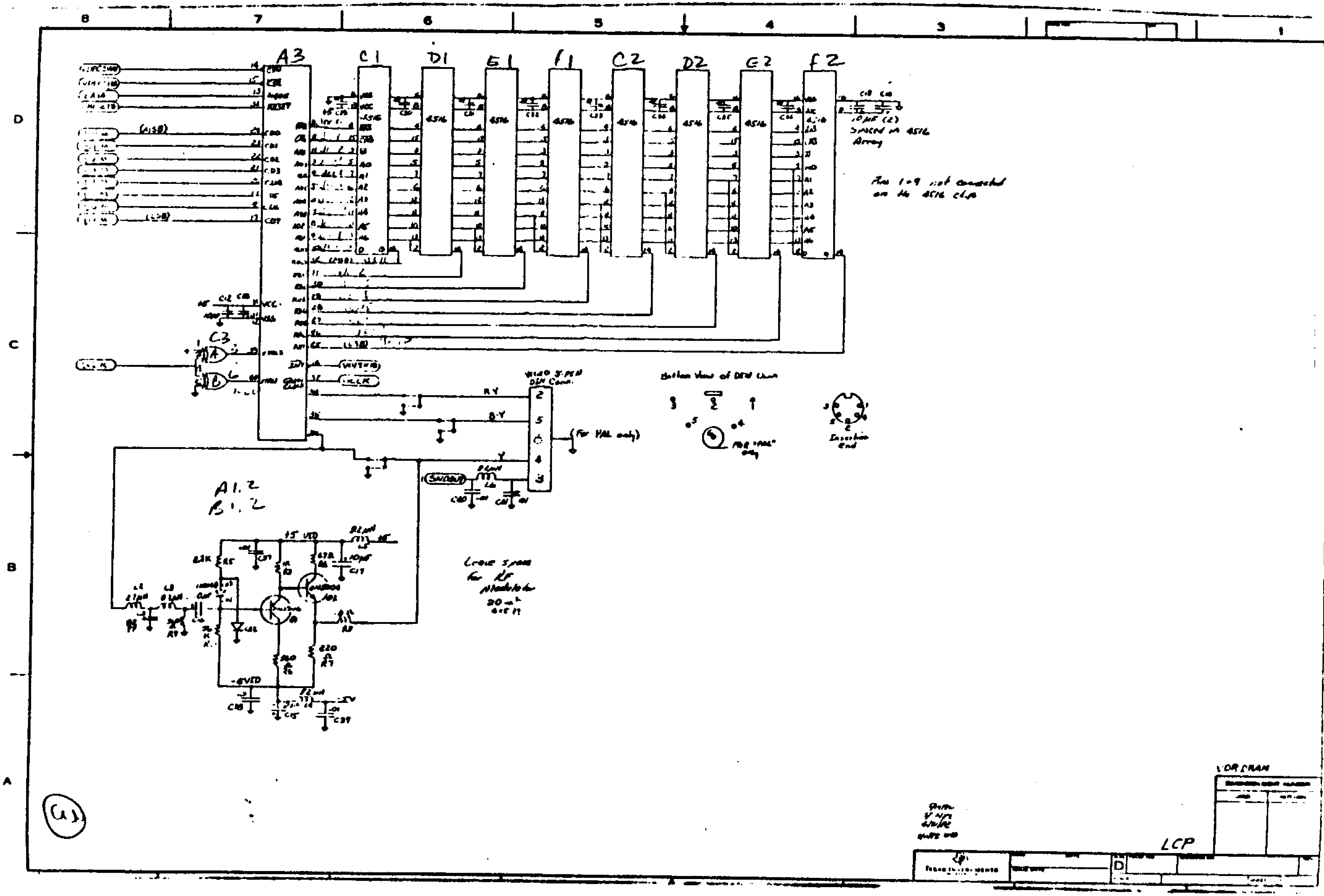
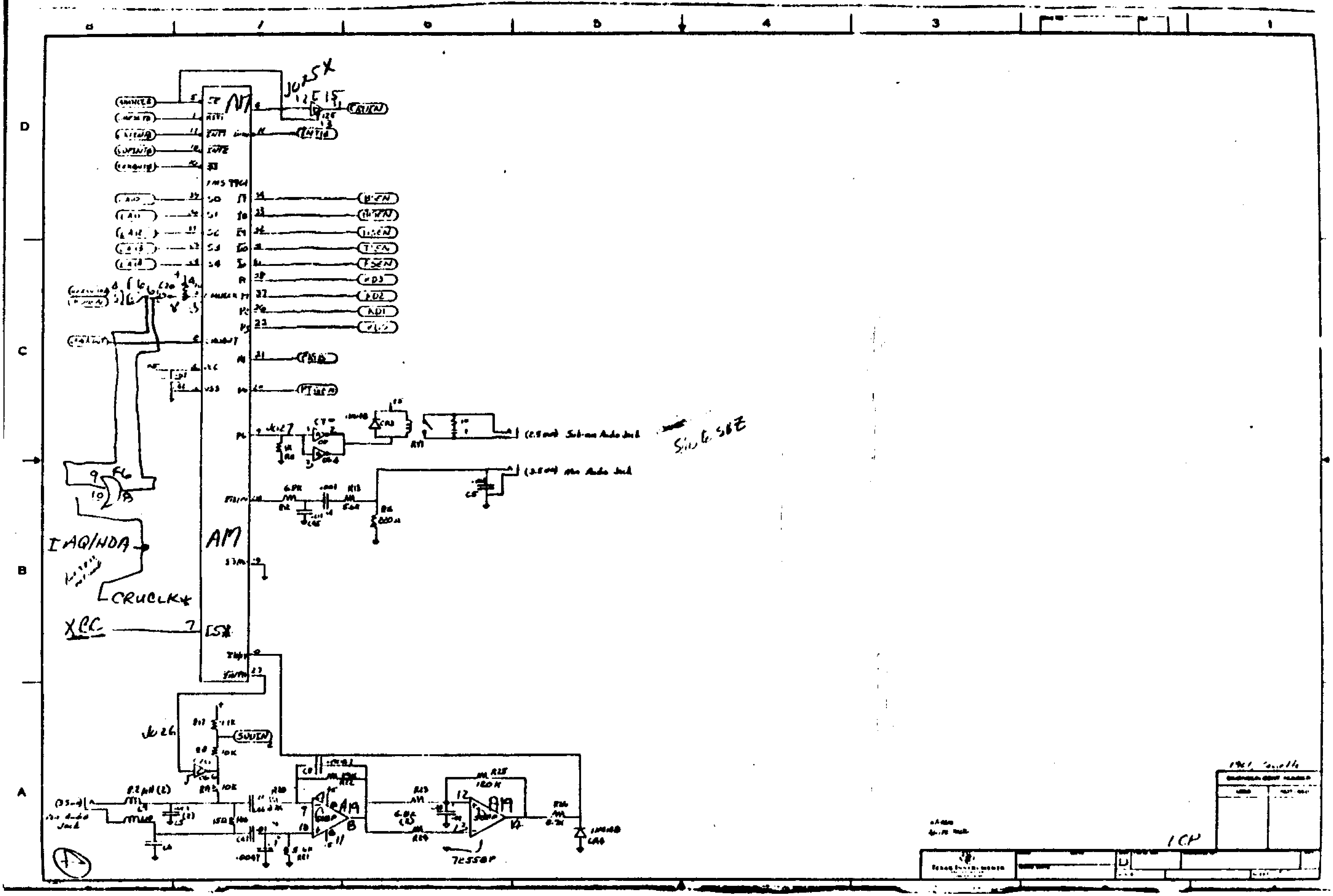
1/25/32


A9
CPURDY
CRUIN
INTI*
LOAD*
SRESET*
HOLD*
+
1K
5.10
5.10
CB
CB
CB
10pF
12pf
10.7MHz
4-1.2MH
9995
A7
DBMP
D1.MP
D2.MP
D3.MP
D4.MP
D5.MP
D6.MP
D7.MP
DBIN*
CB
MEMEN*
WE/CRUCLK
IAQ/HDA
CLKOUT
SCLK
LA00
LA01
LA02
LA03
LA04
LA05
LA06
LA07
LA08
LA09
LA10
LA11
LA12
LA13
LA14
LA15/CO
D0.M
D1.M
D2.M
D3.M
D4.M
D5.M
D6.M
D7.M
DBIN
MEMEN
WE/CRUCLK
IAQ/HDA
CLKOUT
SCLK

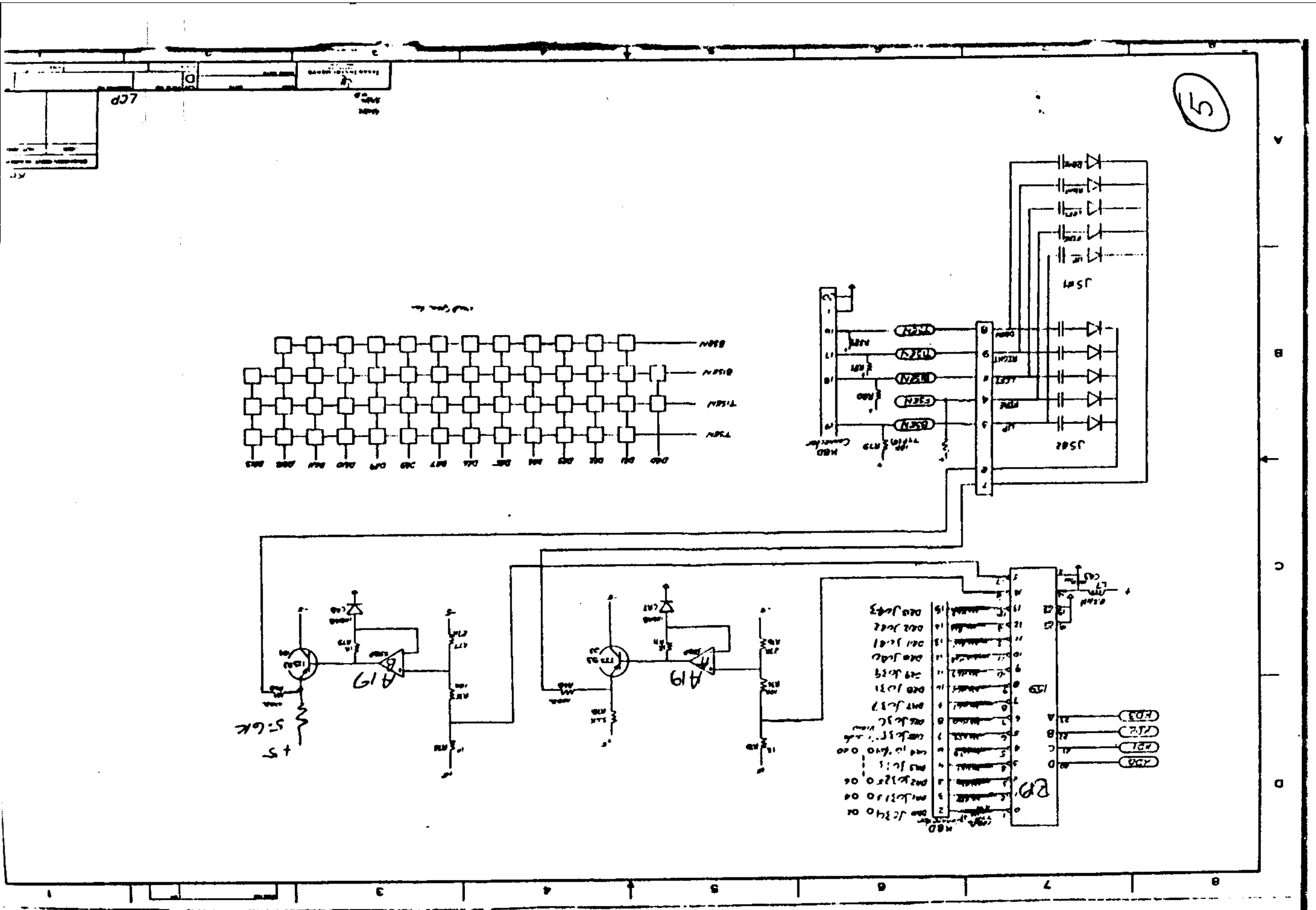
(1)

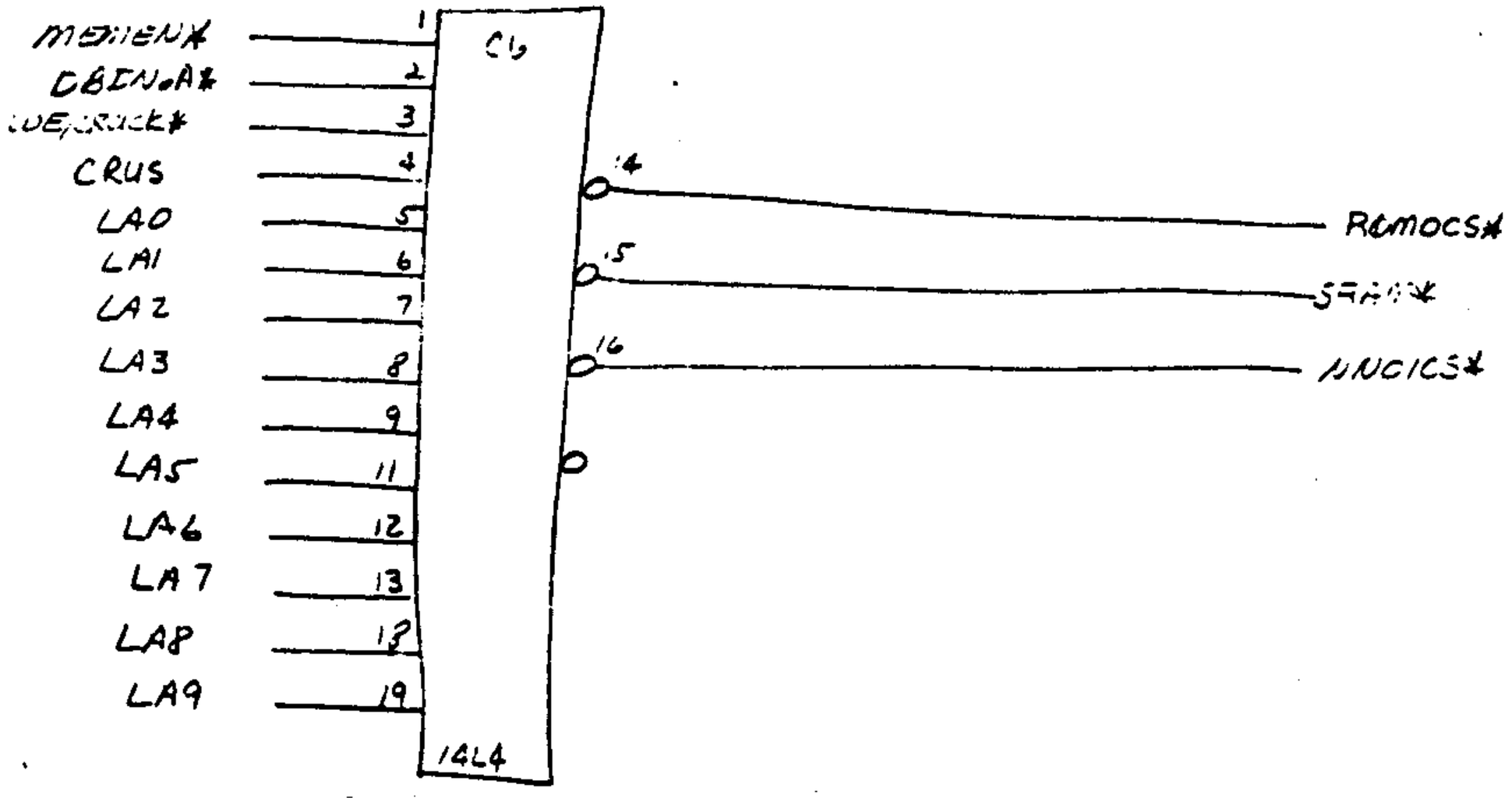

C4
LA03
LA04
LA05
LA06
LA07
LA08
LA09
LA10
LA11
LA12
LA13
LA14
LA15/
COUT
RAMCSK
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
CS
8KX8
ROM
D0.M
D1.M
D2.M
D3.M
D4.M
D5.M
D6.M
D7.M
D8
D7
D6
D5
D4
D3
D2
D1
A4
SRAMCSK
DBIN
WE
2KX8
SRAM


A3
C1
D1
E1
F1
C2
D2
E2
F2
4516
Pins 1+9 not connected on the 4516 chip
Video 5-pin DIN Conn.
(For VAL only)
Bottom View of DIN Conn.
Insertion End
A1, 2
B1, 2
C3
SNDOUT
LCP
VDP DRAM

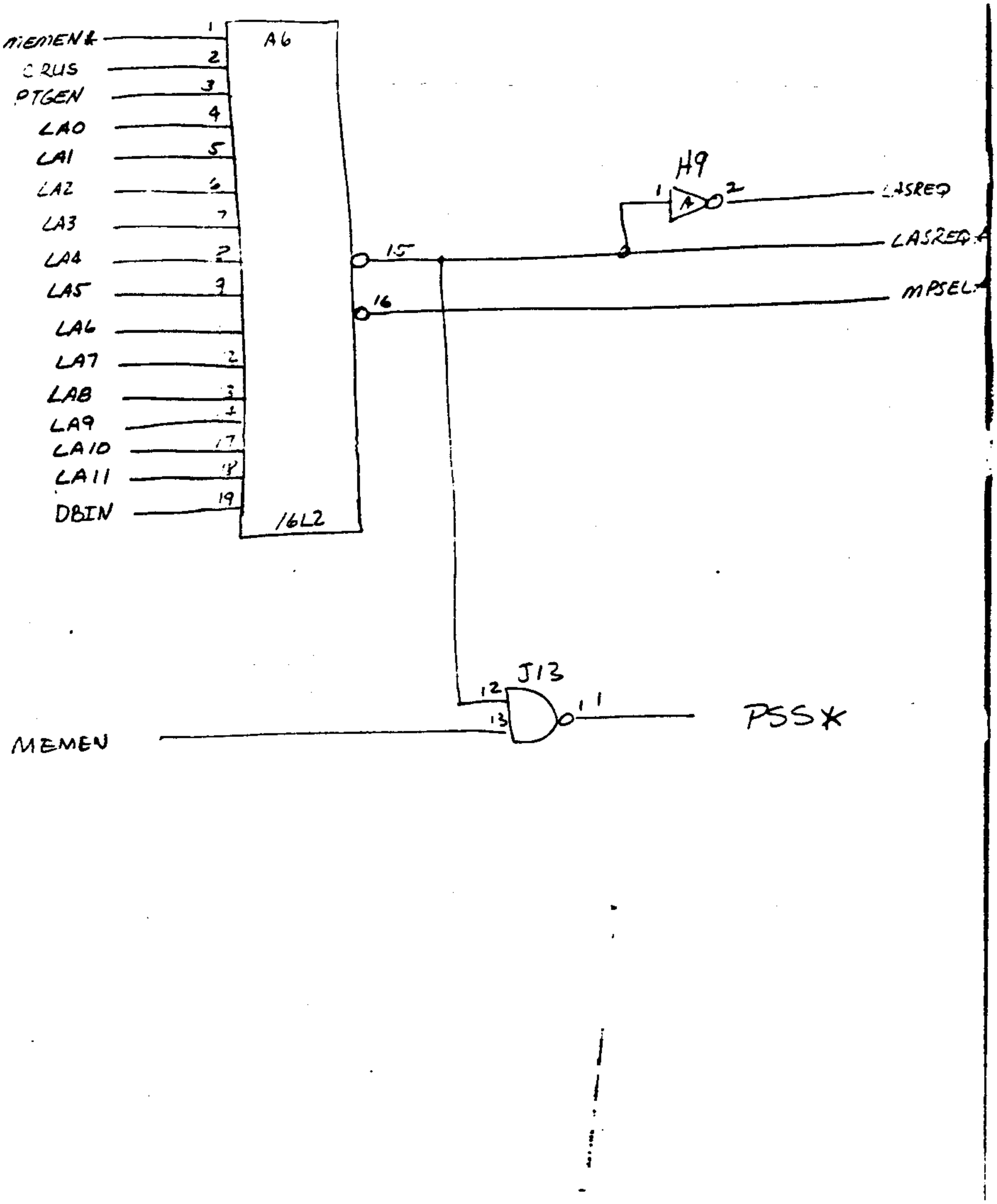


AM
XCC
CRUCLK*
IAQ/HDA
ICP
7255BP
SUUIN
(2.5 mm) Sub-min Audio Jack
(3.5 mm) Mini Audio Jack

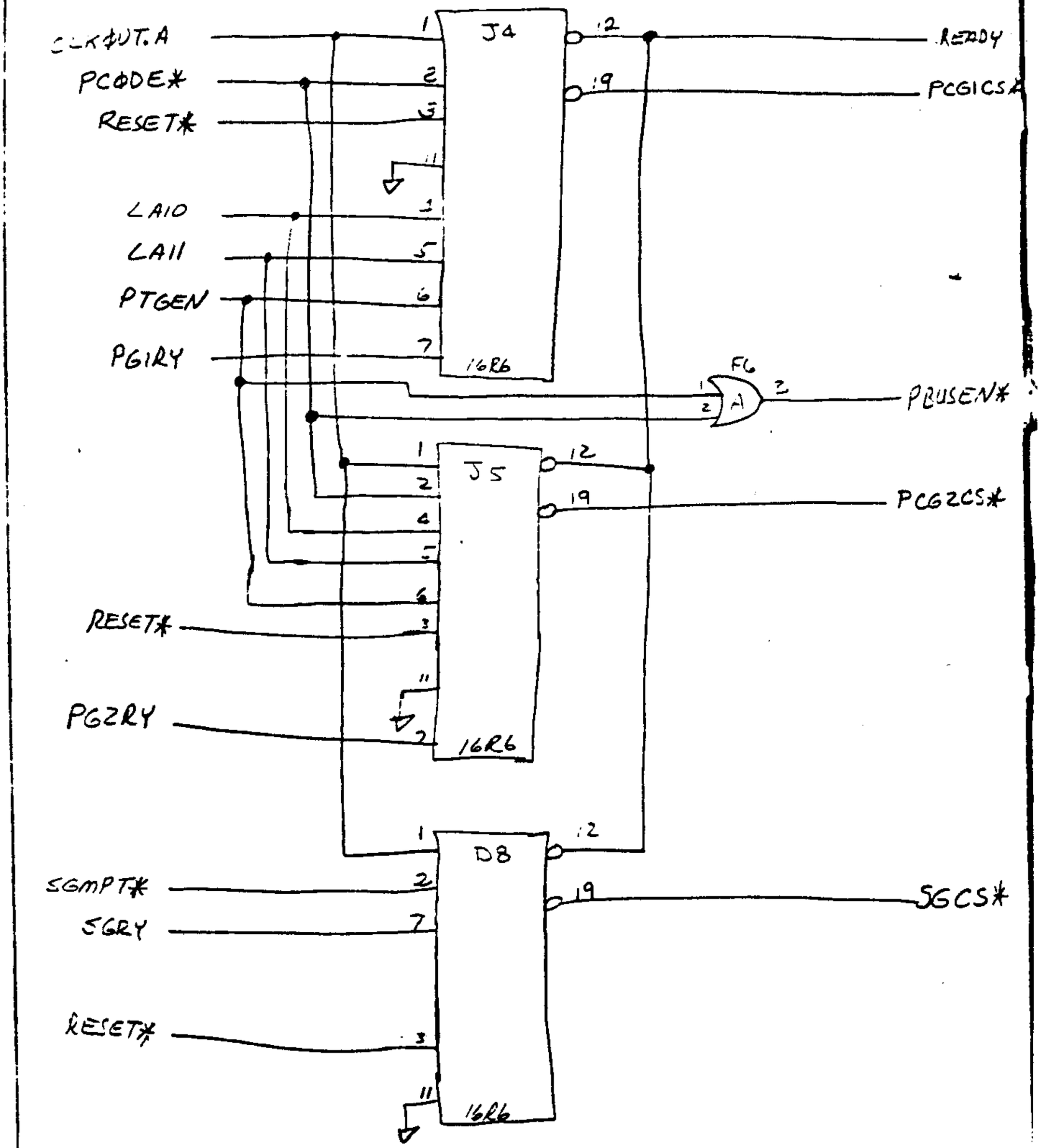




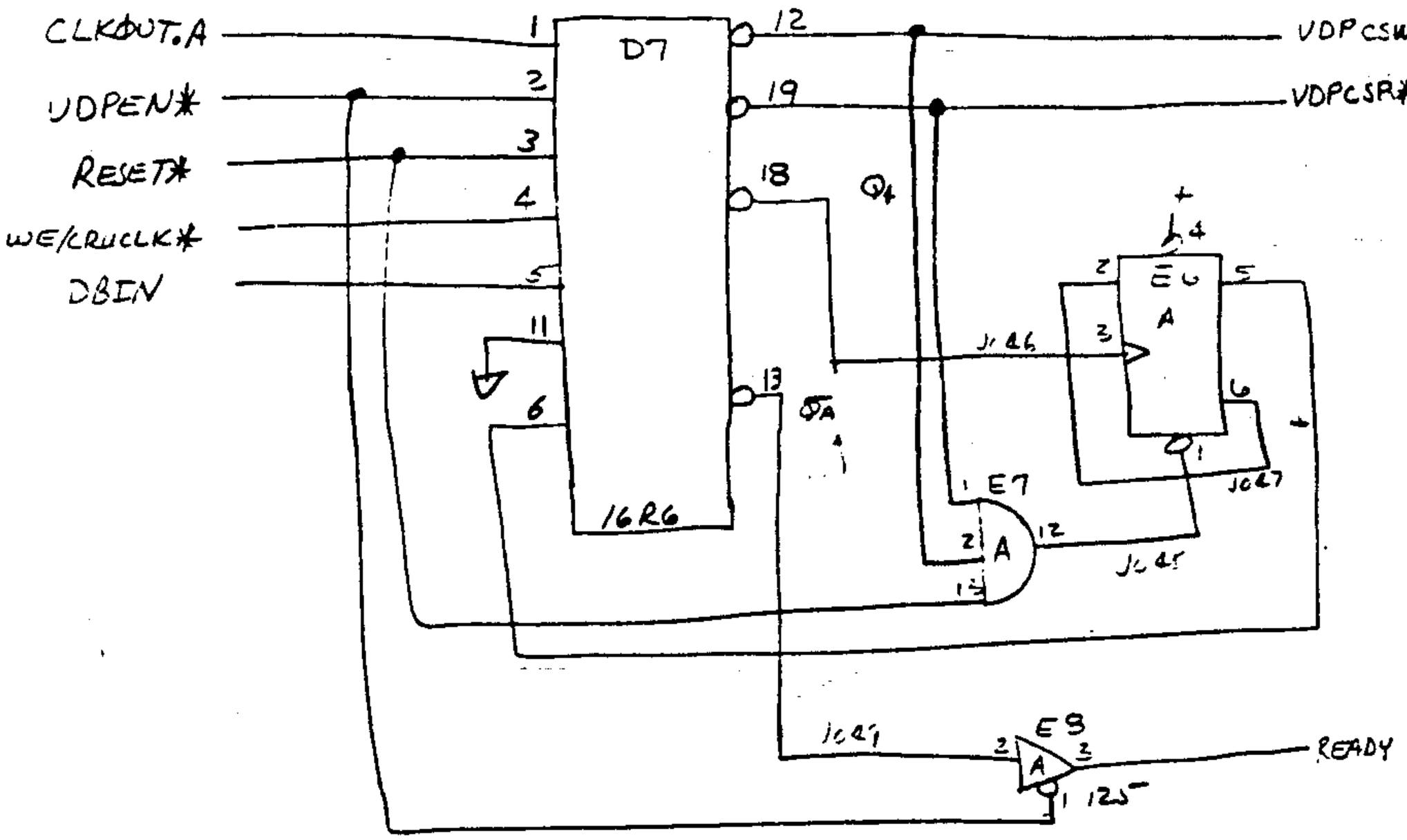
LAS Decode PLA's



Selects for ±5, MAP2 PLD



GROUP Protect Logic


CLKOUT.A
VDPEN*
RESET*
WE/CRUCLK*
DBIN
D7
16R6
1
2
3
4
5
11
6
12
19
18
13
Q4
$\overline{Q_A}$
VDPCSW*
VDPCSR*
J0 46
J0 47
J0 45
E7
E6
A
E9
READY
1049
1125

VDP Protect

CLKOUT

SPSRD*

SPSWT*

SSRCLK

F8

A

D4

CMOS 245

DO.M

D1.M

D2.M

D3.M

D4.M

D5.M

D6.M

D7.M

DBIN.A*

F4

9900

RS

WS

OSC

RDY

GND

DO

D1

D2

D3

D4

D5

D6

D7

ADD1

ADD2

ADD4

ADD8

ROMCLK

IO

I1

AUDIO

.1M

.1M

+5

E6

E9

JC:1

JC:2

J1

J3

ROMCLK

IO

I1

.22M

1.8K

100N

D3

9919

DO

D1

D2

D3

D4

D5

D6

D7

CE

WE

SNDCS*

GCLK

SNDIN

SNDI

330

RDY

SNDOUT

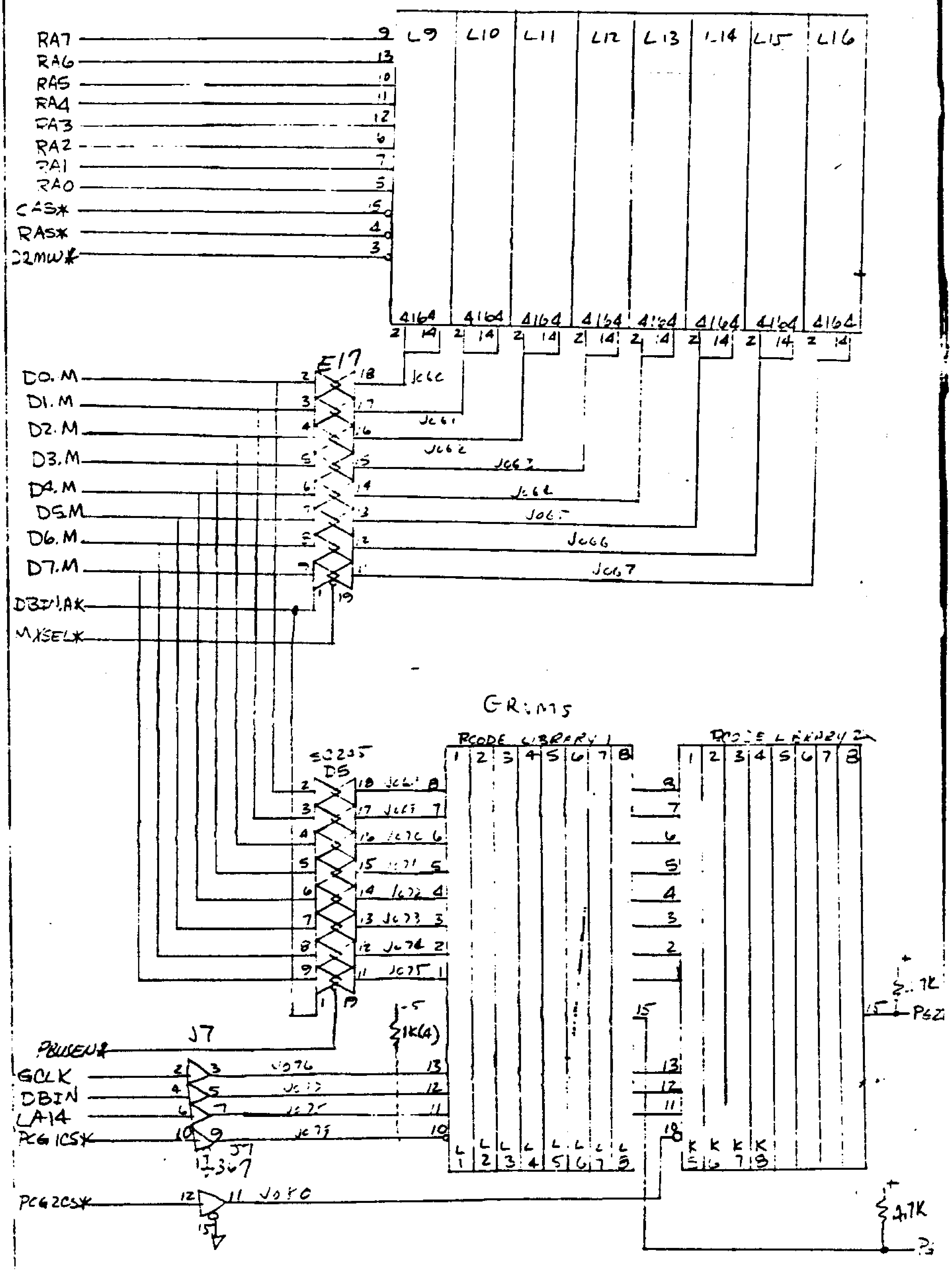
SNDOU

10

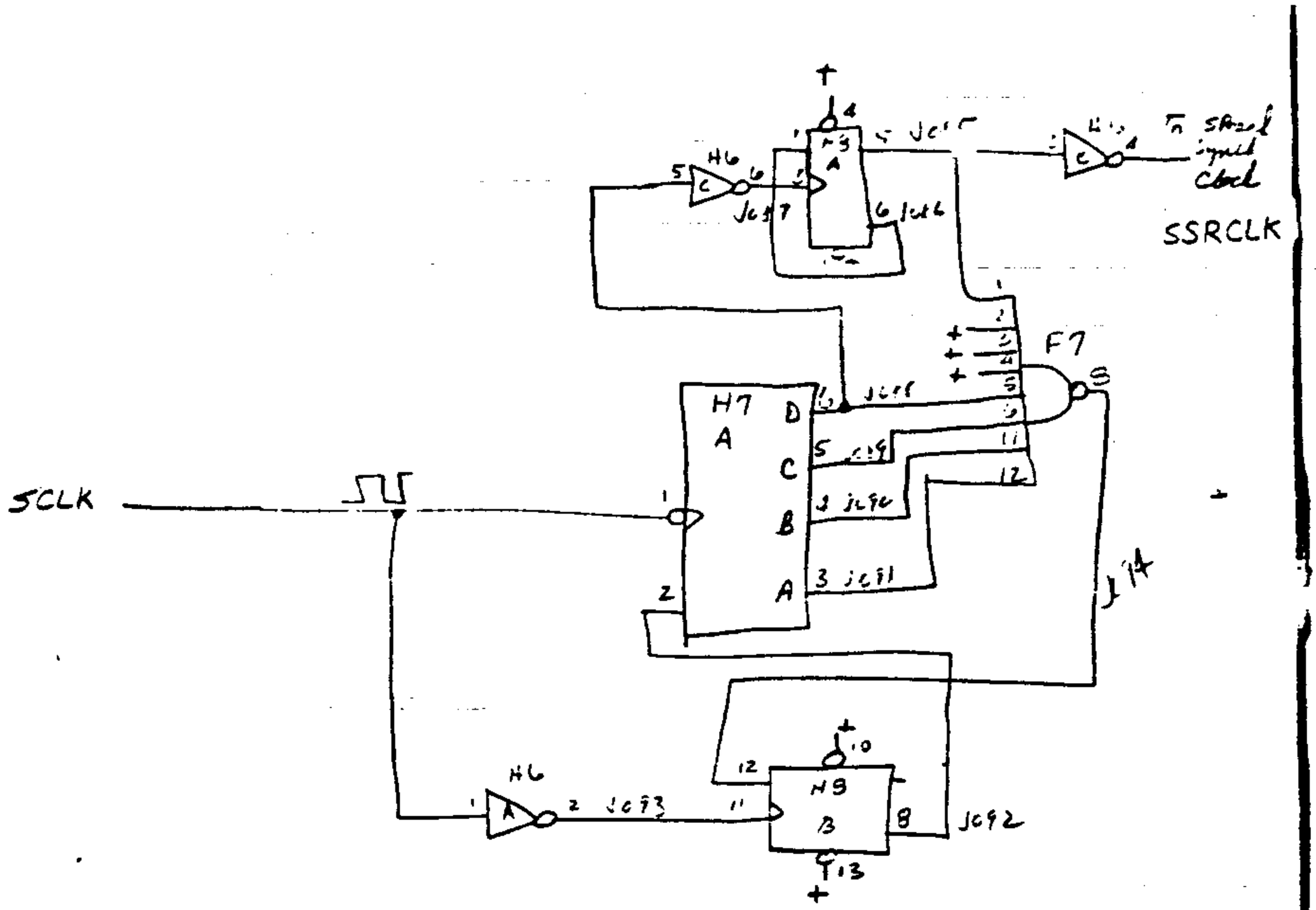
.1N

100N

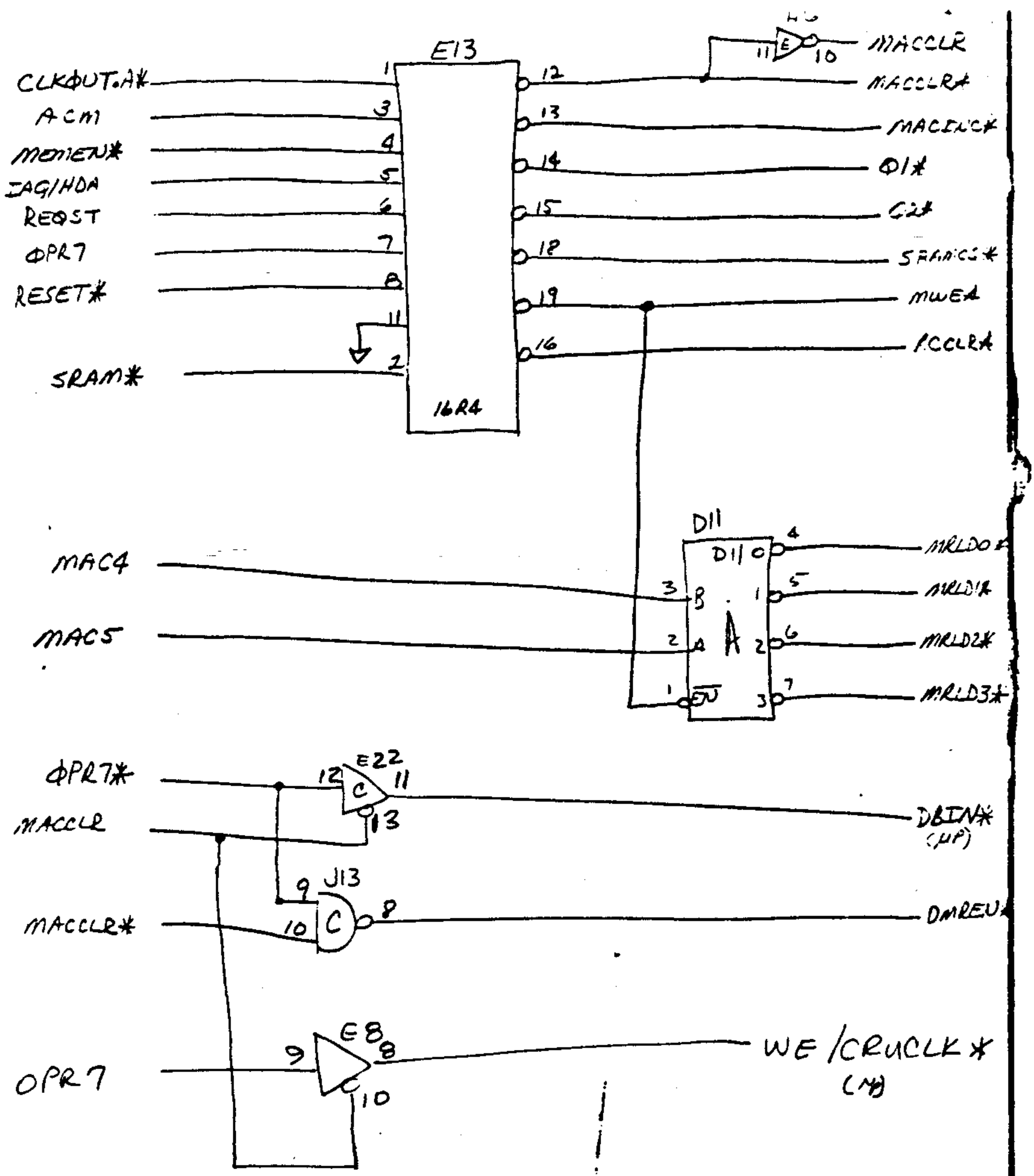
Speech, Sound Gen

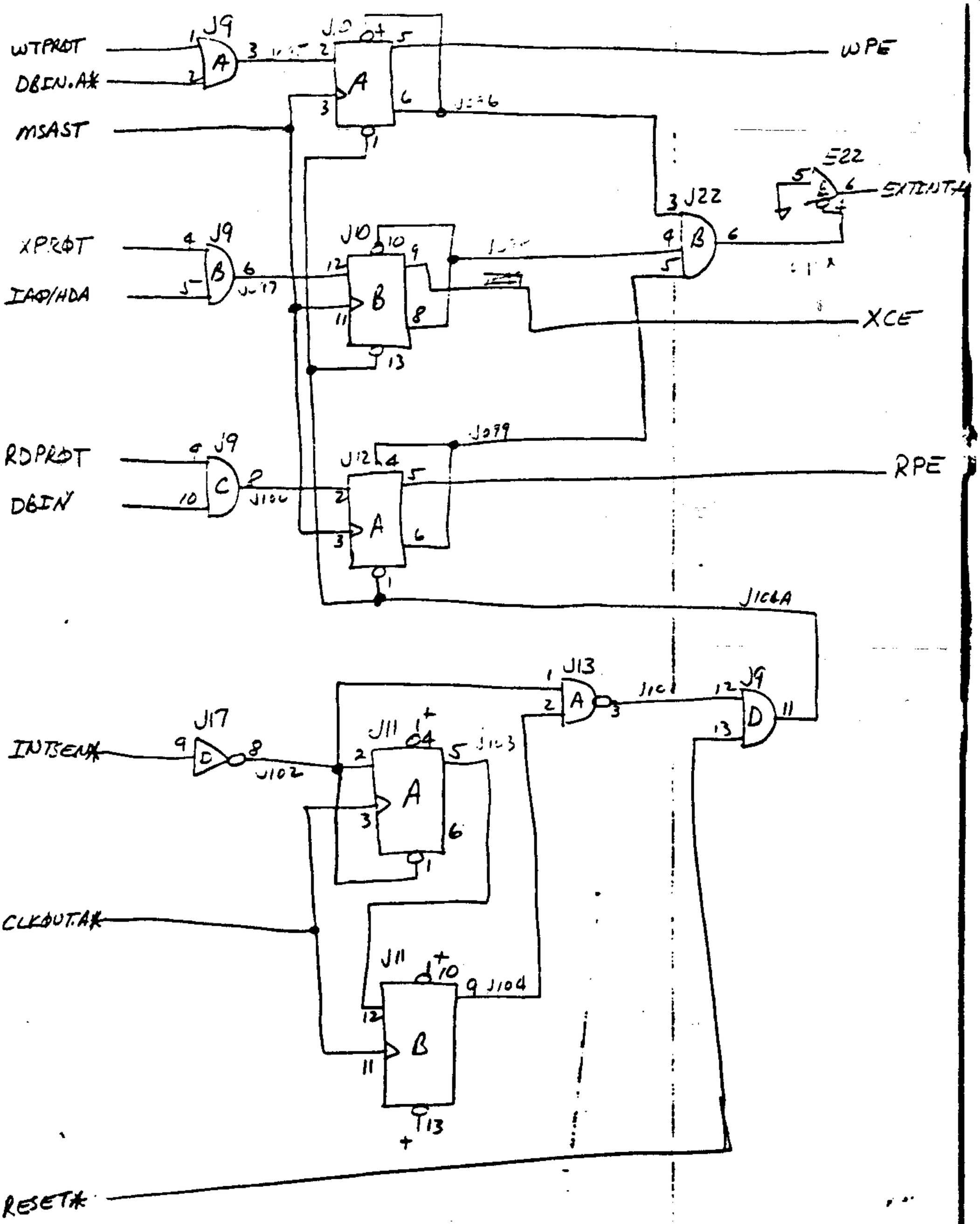


DRAM PCODE LIBRARIES



Speech Synth. Clock


E13
CLKOUT.A*
ACM1
MDMENU*
JAG/HDA
REQST
ΦPR7
RESET*
SRAM*
16R4
MACCLR
MACCLR*
MRLD0*
MRLD1*
MRLD2*
MRLD3*
D11
MAC4
MAC5
ΦPR7*
MACCLR
E22
J13
DBIN*
(μP)
DMREQ*
OPR7
E8
WE/CRUCLK*
(μP)


WTPROT
DBIN.A*
MSAST
XPROT
IACK/HDA
RDPROT
DBIN
INTSEN*
CLKOUT.A*
RESET*
WPE
XCE
RPE
EXTINT*
J1C6A
J9
J10
J11
J12
J13
J17
J22
E22

C12

LAO0

MACO

RFA0

LAO1

MAC1

RFA1

LAO2

MAC2

RFA2

LAO3

MAC3

RFA3

MACINC*

MACCLR*

F9

MACO

MAC1

E7

ACM

J105

F10

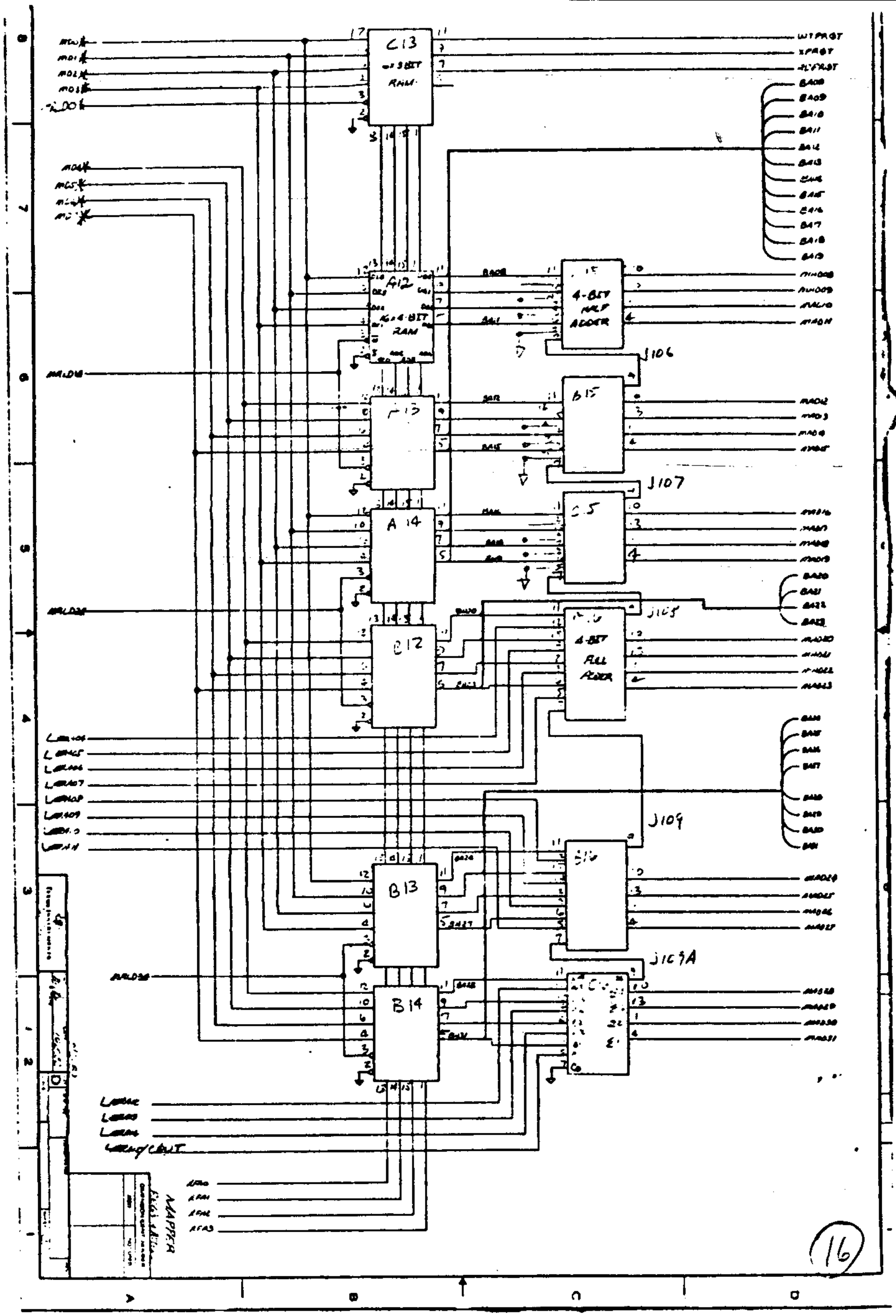
MAC2

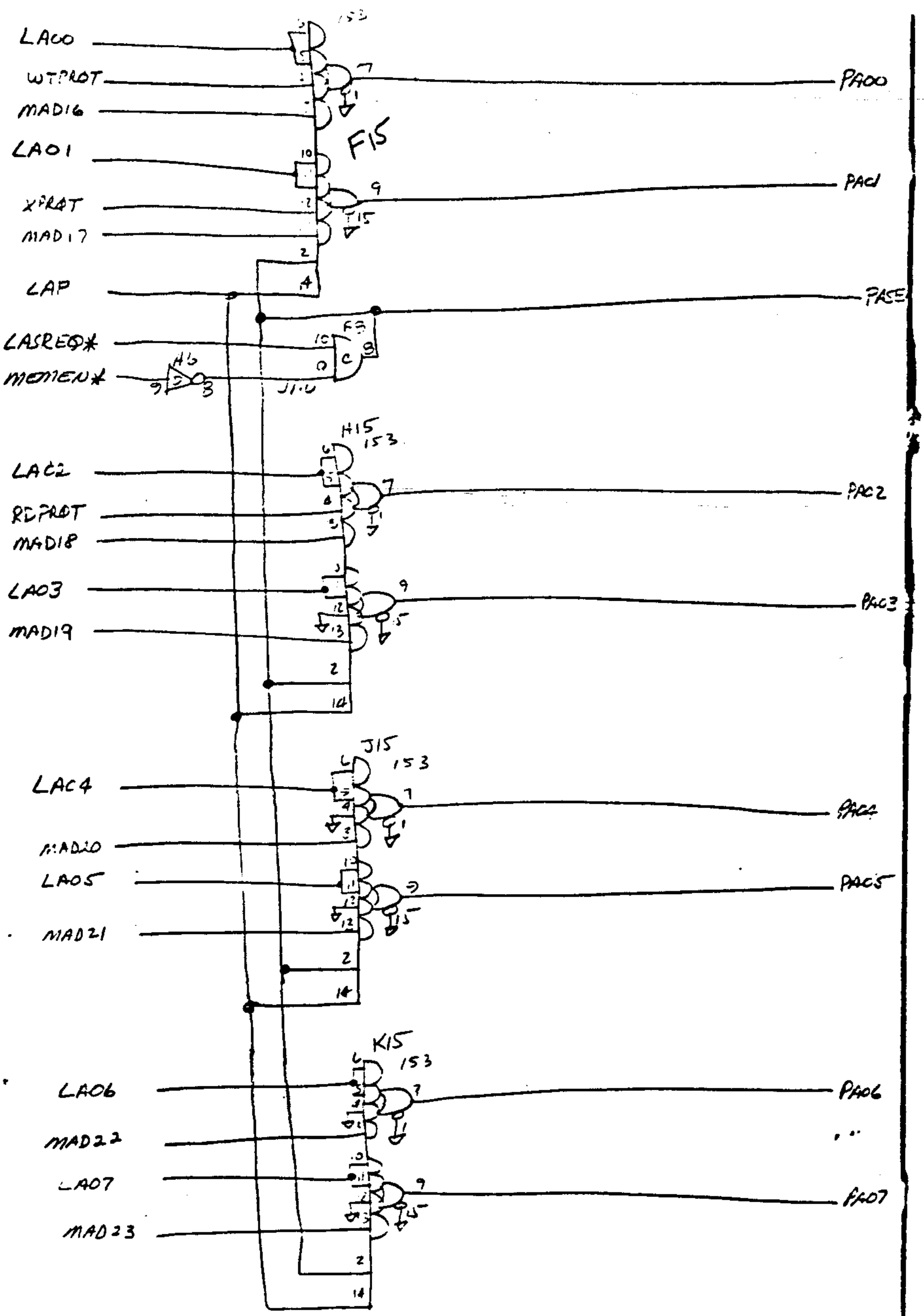
MAC3

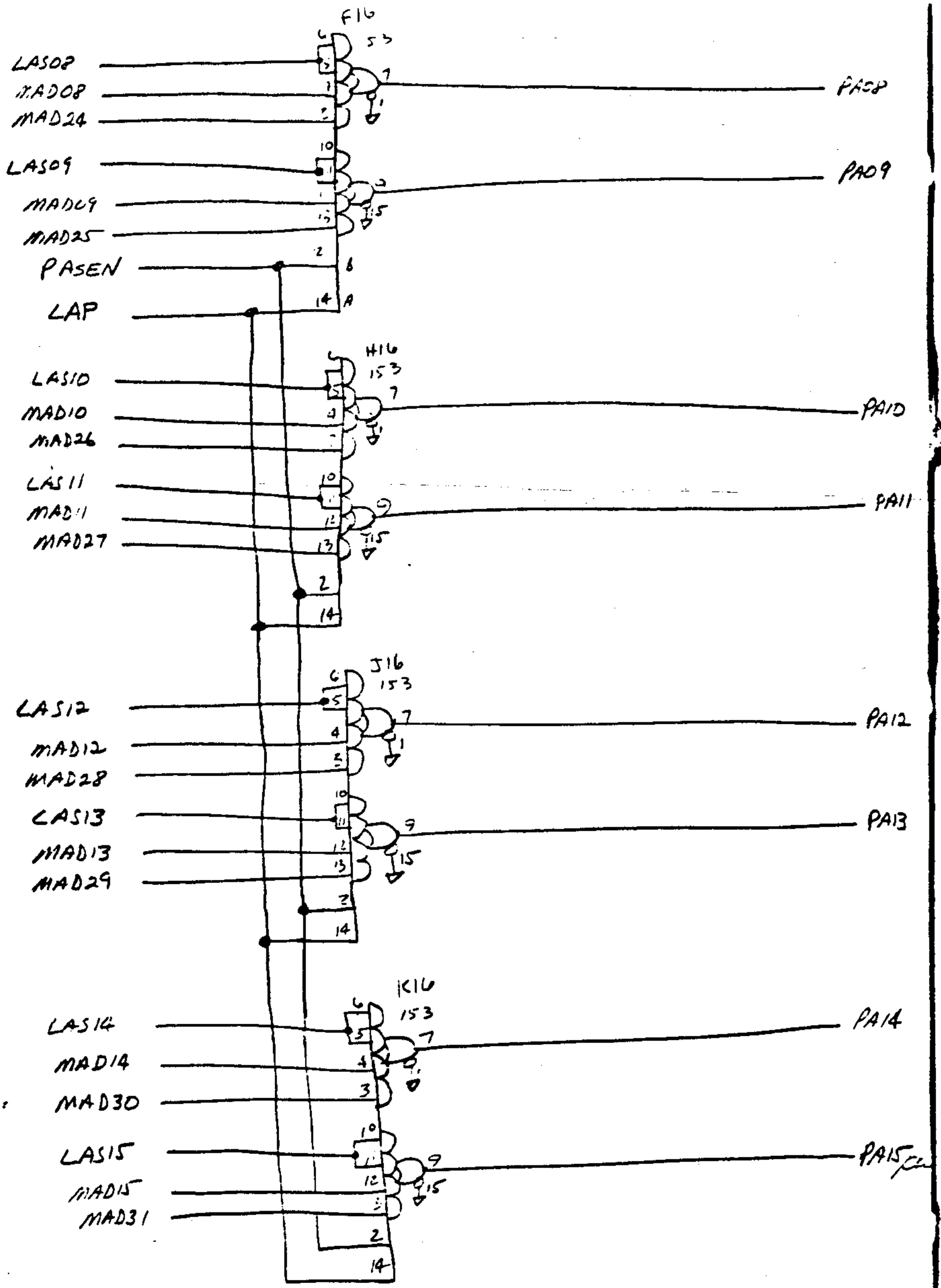
MAC4

MAC5

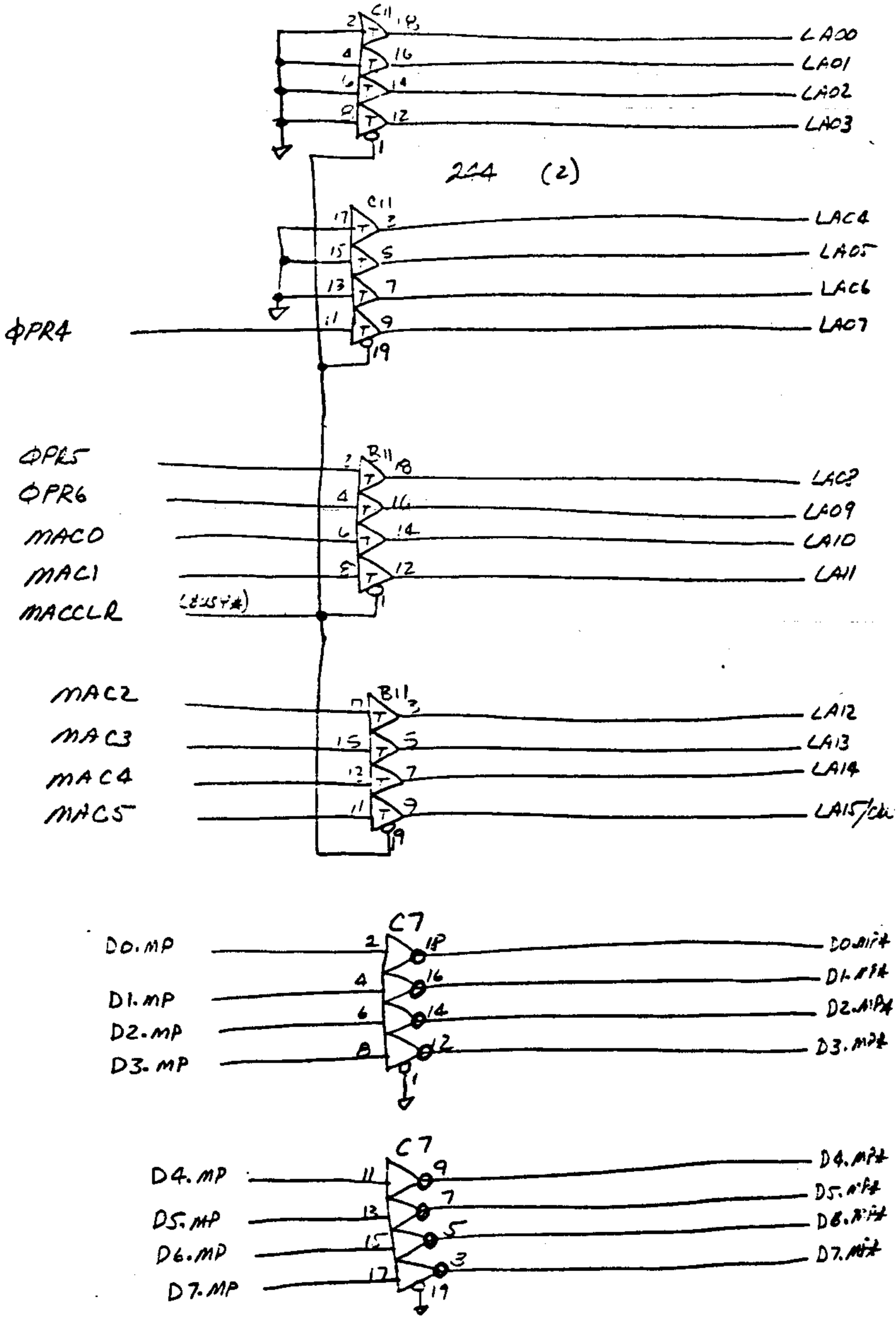
J105X


C13
4-BIT RAM
A12
4K x 4-BIT RAM
4-BIT HALF ADDER
J106
B15
J107
C5
A14
B12
4-BIT FULL ADDER
J108
J109
B13
B14
J109A
MAPPER
16


LAC0
WTPROT
MAD16
LAC1
XPROT
MAD17
LAP
LASREQ*
MEMEN*
LAC2
RDPROT
MAD18
LAC3
MAD19
LAC4
MAD20
LAC5
MAD21
LAC6
MAD22
LAC7
MAD23
PAC0
PAC1
PASE
PAC2
PAC3
PAC4
PAC5
PAC6
PAC7
F15
J15
K15
153
WIRE
LAS/PAS MUX

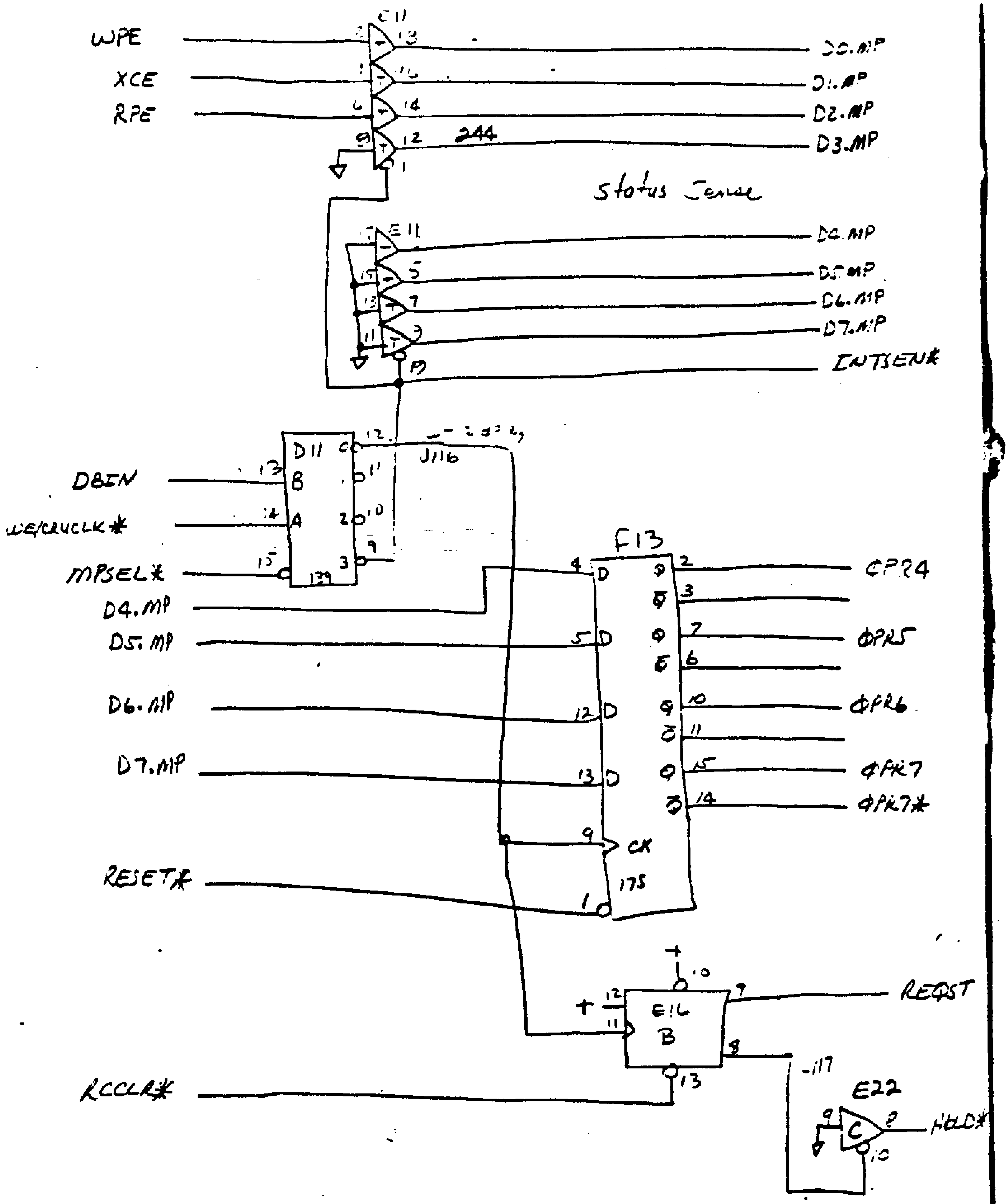


LAS/PAS MUX LSB4

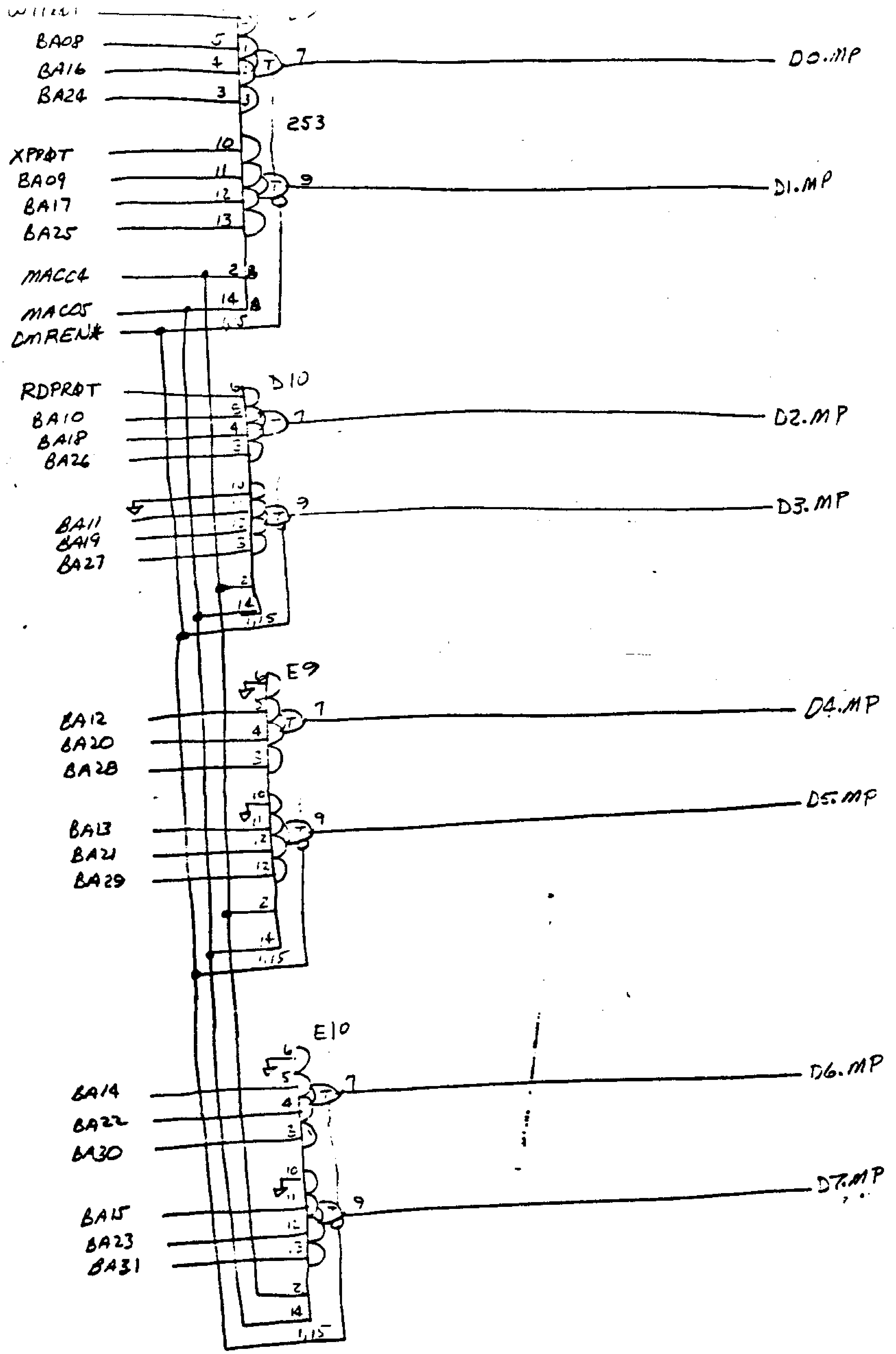


MAPPER

DMA Address Drivers

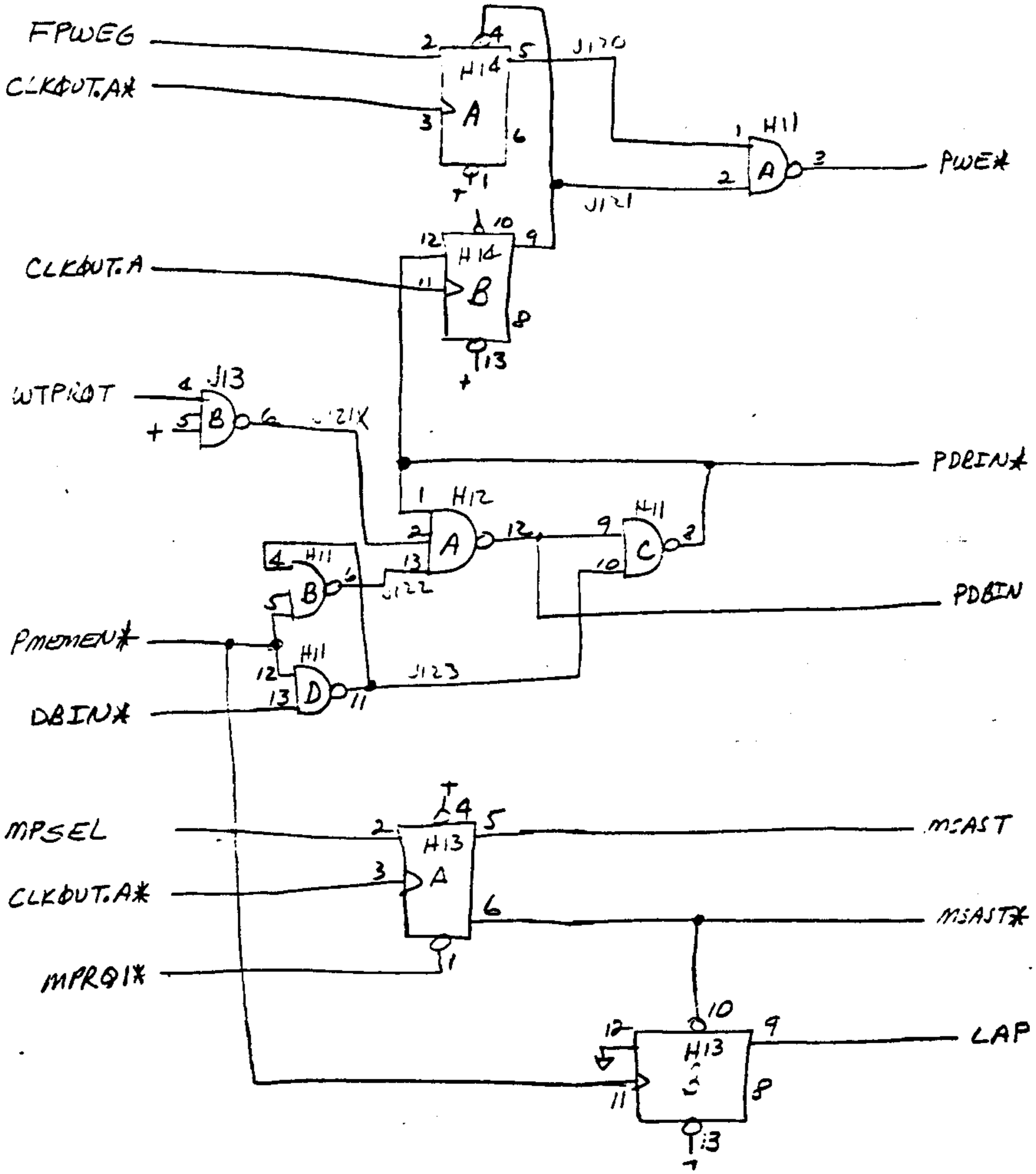


Status Sense, ΦP Reg

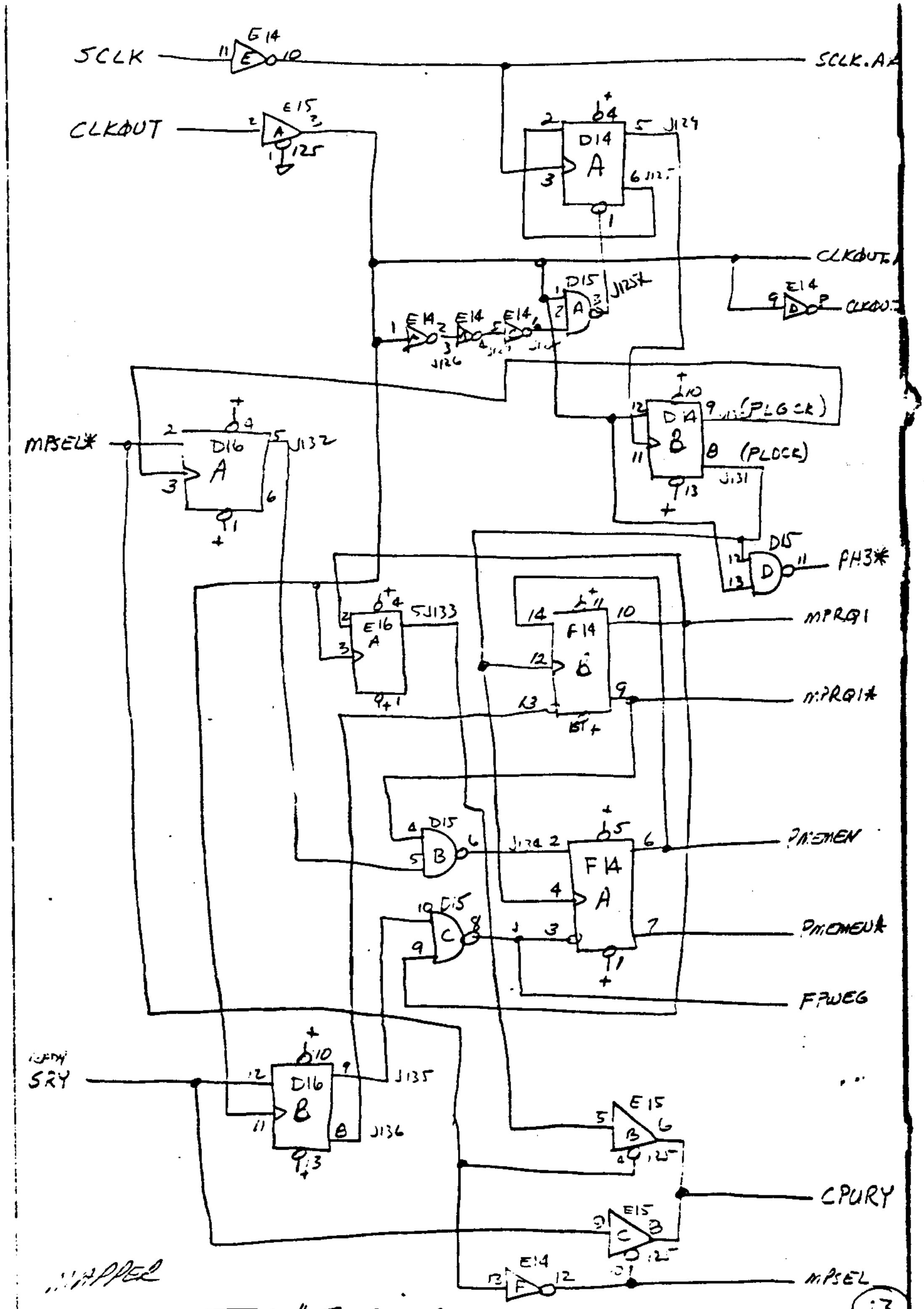


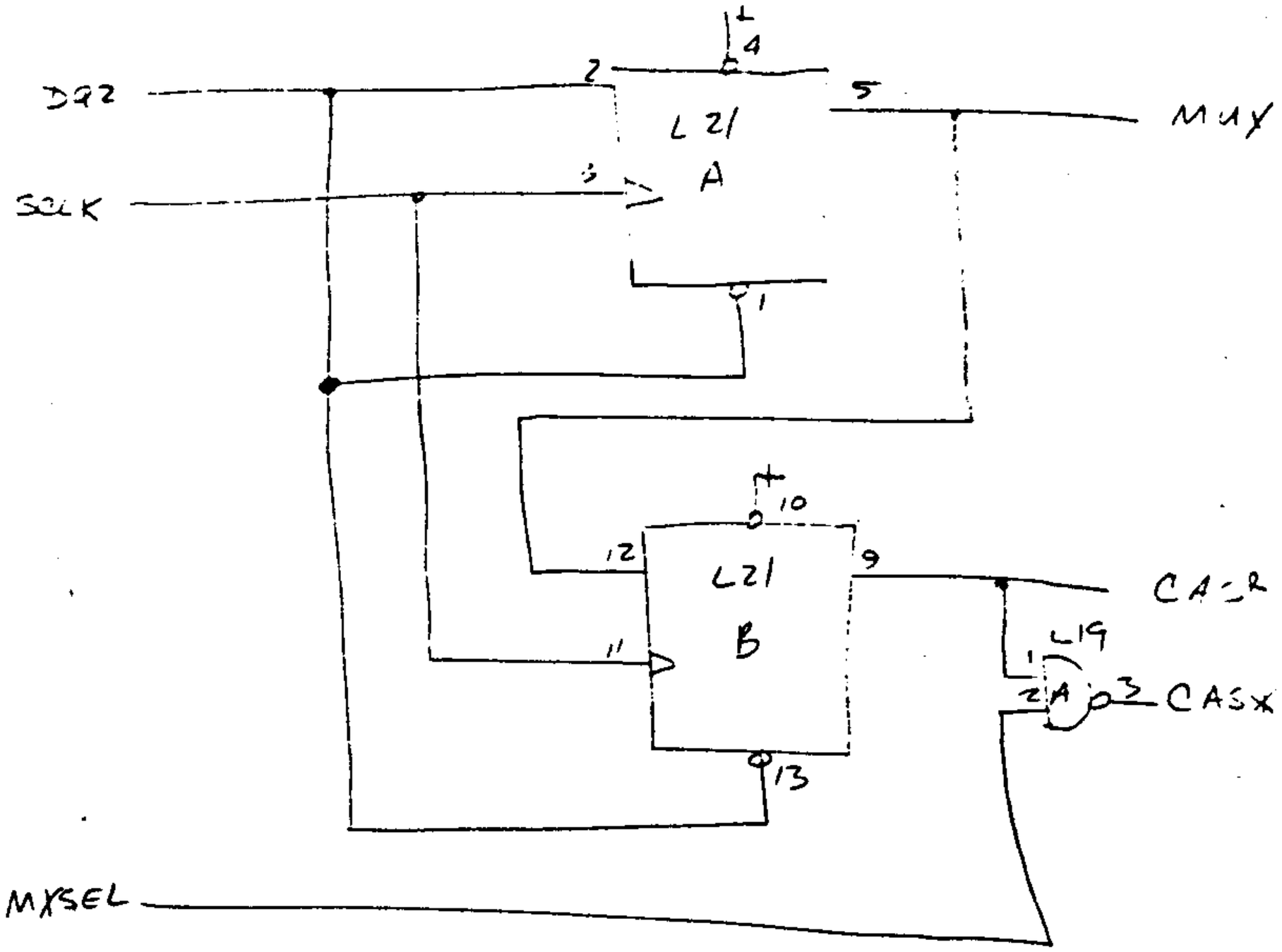
BA08
BA16
BA24
253
XPROT
BA09
BA17
BA25
MACC4
MAC05
DMREN*
D0.MP
D1.MP
D10
RDPROT
BA10
BA18
BA26
BA11
BA19
BA27
D2.MP
D3.MP
E9
BA12
BA20
BA28
BA13
BA21
BA29
D4.MP
D5.MP
E10
BA14
BA22
BA30
BA15
BA23
BA31
D6.MP
D7.MP

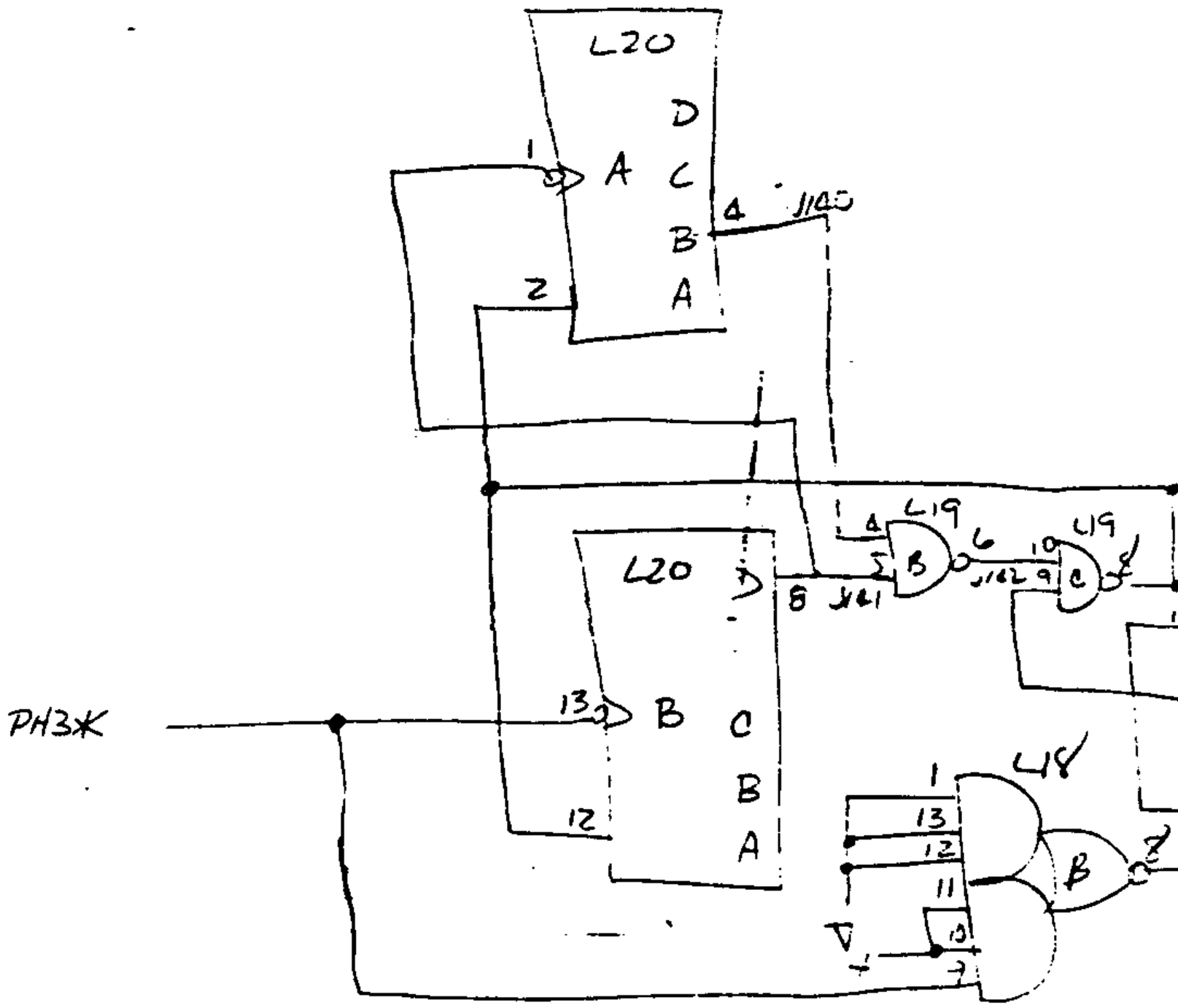
DMA READ MUX



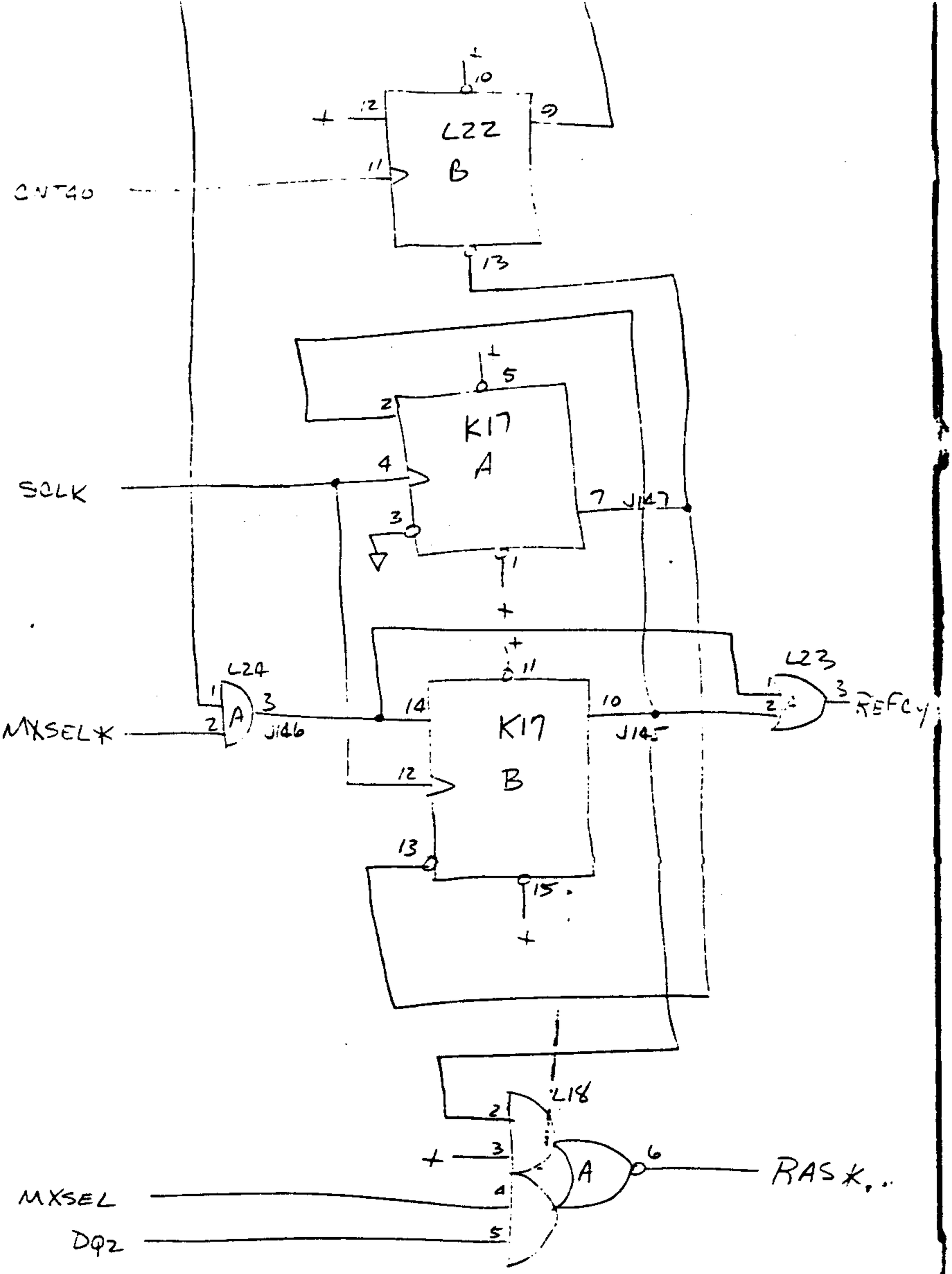
"P" Serial Gen #2


SCLK
G14
SCLK.A
CLKOUT
E15
D14
J129
J127
CLKOUT
D15
J125
E14
J126
D16
J132
MPSEL*
J131
(PLOCK)
PLOCK
D15
PH3*
E16
J133
MPRQ1
F14
MPRQ1*
D15
J134
F14
PMEMEN
PMEMEN*
FPWEG
D16
J135
J136
CPURY
E15
E14
MPSEL
TFC "P" Signals

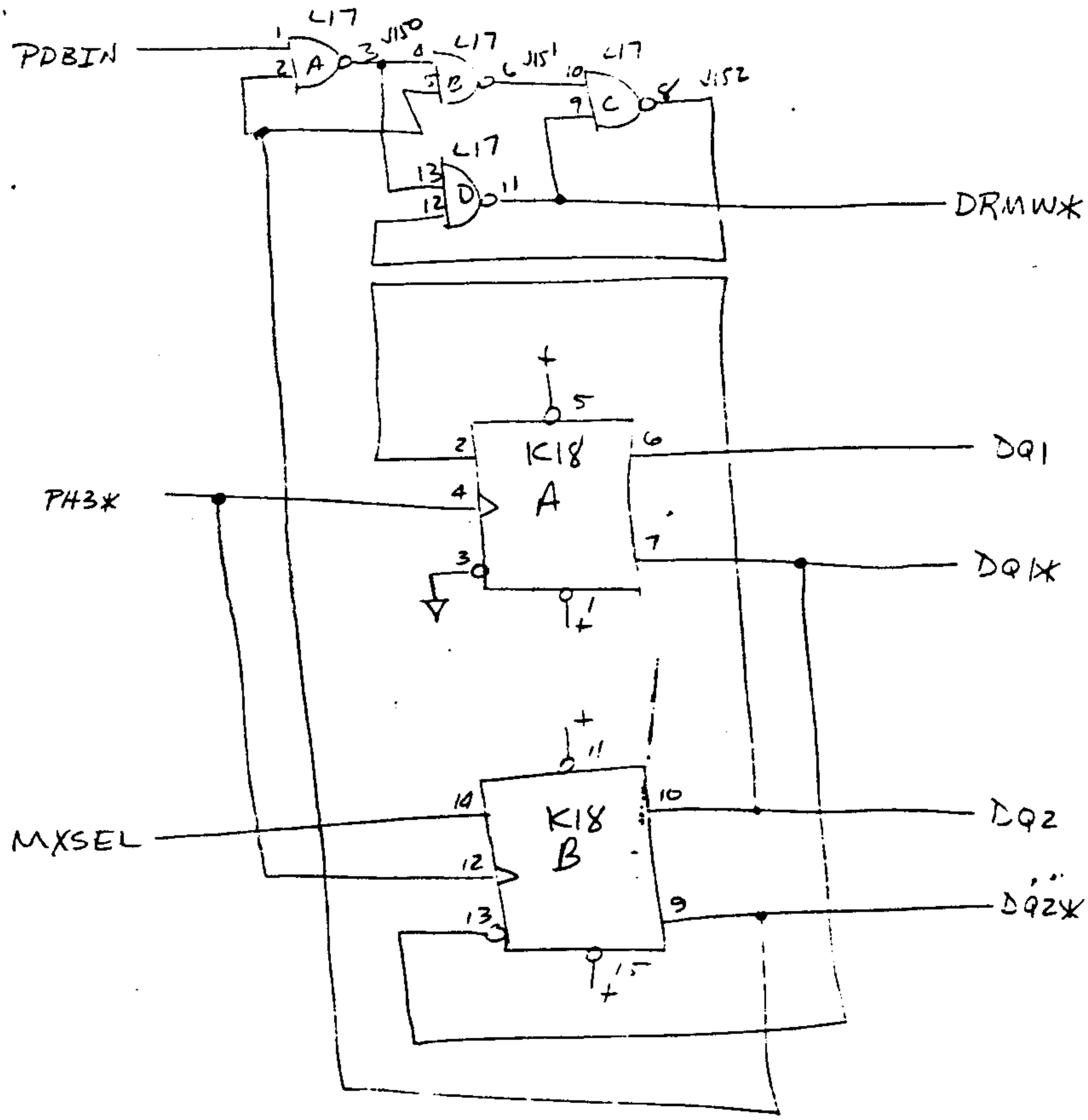

L
4
2
DQ2
5
MUX
L21
A
3
SCLK
1
10
12
9
L21
B
CASR
L19
11
1
2
A
3
CASX
13
MXSEL


L20
D
1
A
C
4
J145
B
2
A
CNTO
L19
4
5
B
6
10
L19
J142
9
C
8
J141
L19
12
D
11
J14
13
B
C
PH3X
B
12
A
L18
1
13
12
11
B
8
PH2
10

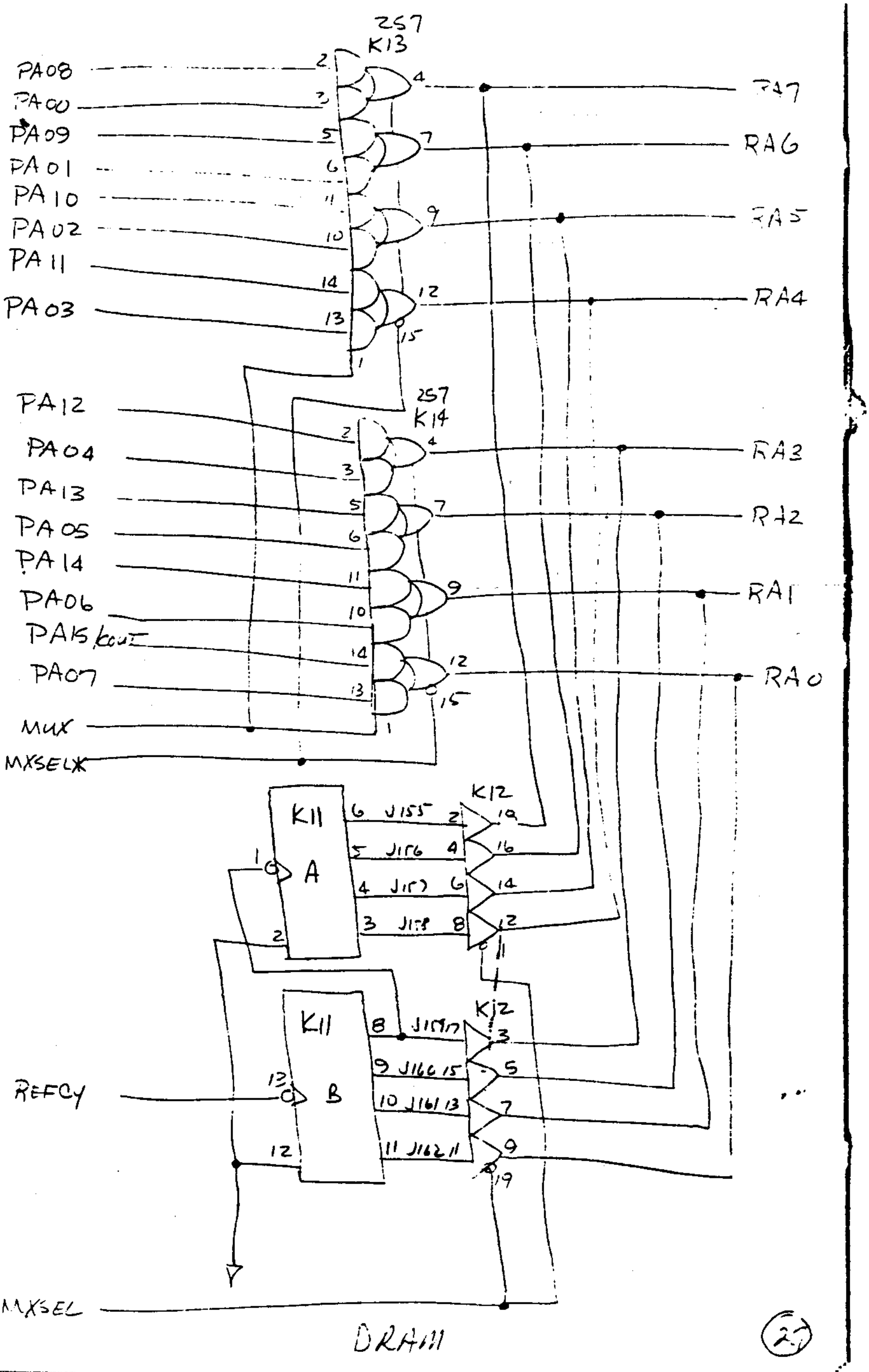
DRAM

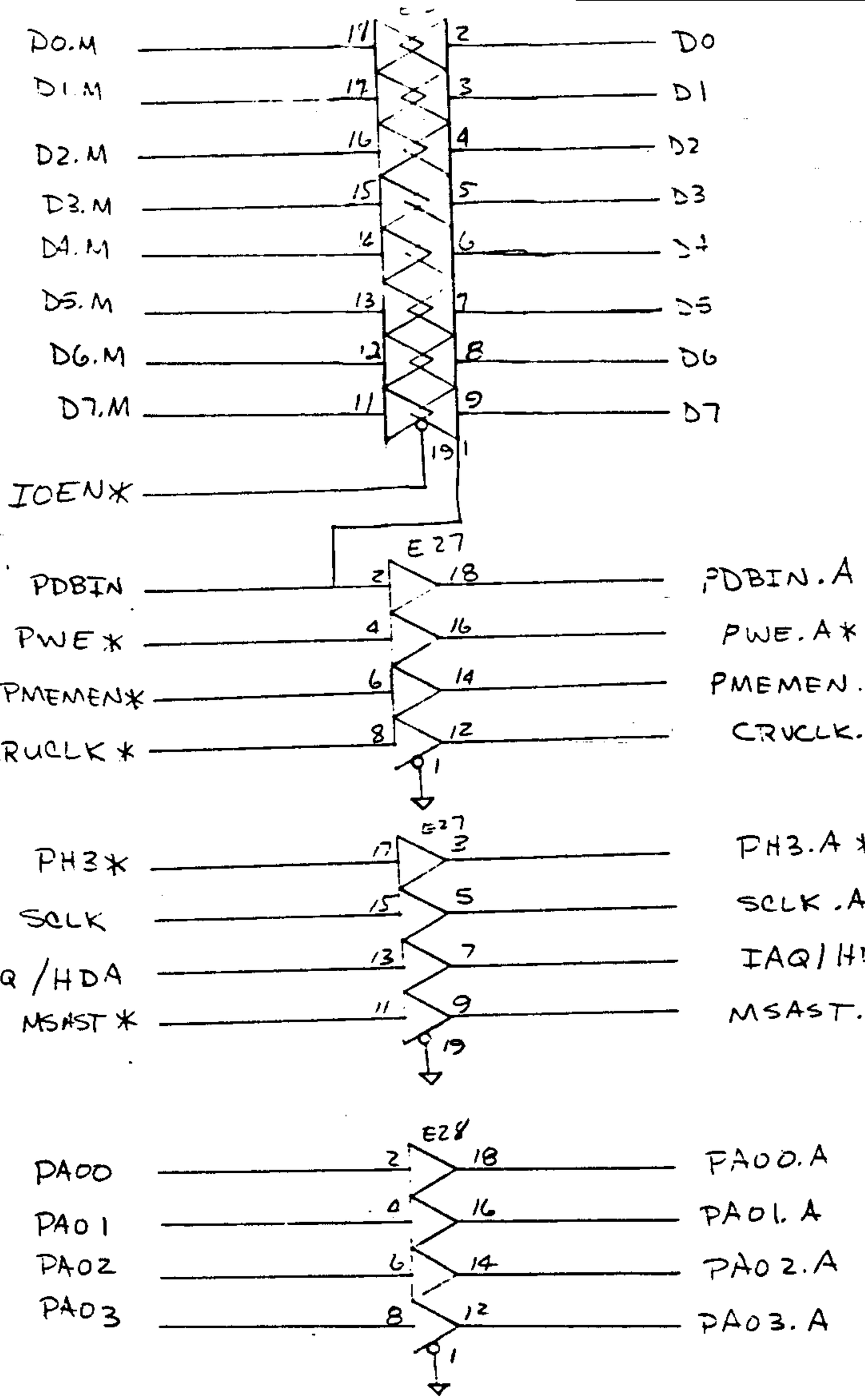

CNTRO
L22
B
K17
A
SCLK
J147
L24
MXSELX
J146
K17
B
J145
L23
REFCY
L18
MXSEL
DQ2
RASX..

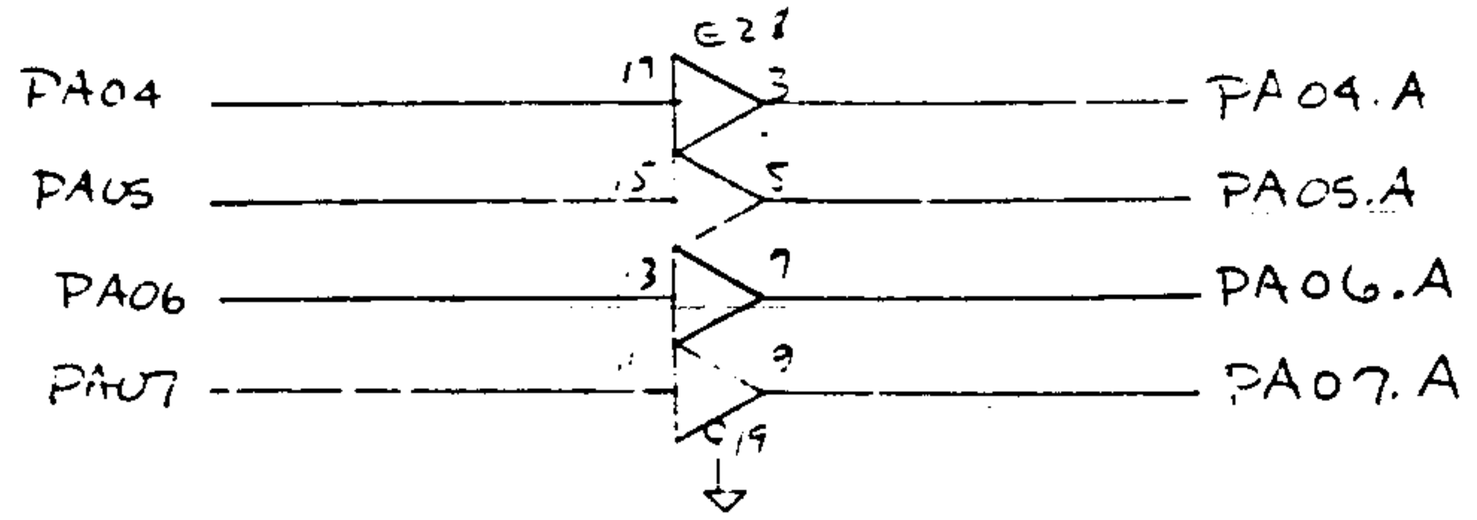
DRAM

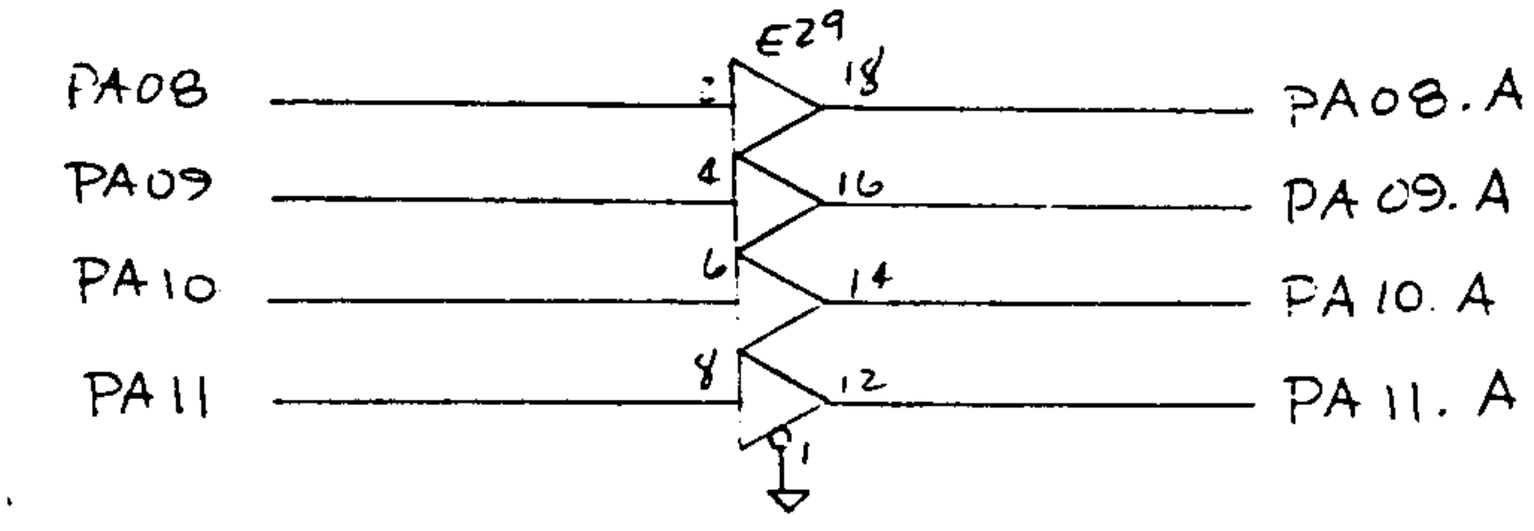

PDBIN
L17
J150
J151
J152
A
B
C
D
DRMW*
+5
IC18
A
DQ1
PH3*
DQ1*
MXSEL
IC18
B
DQ2
DQ2*

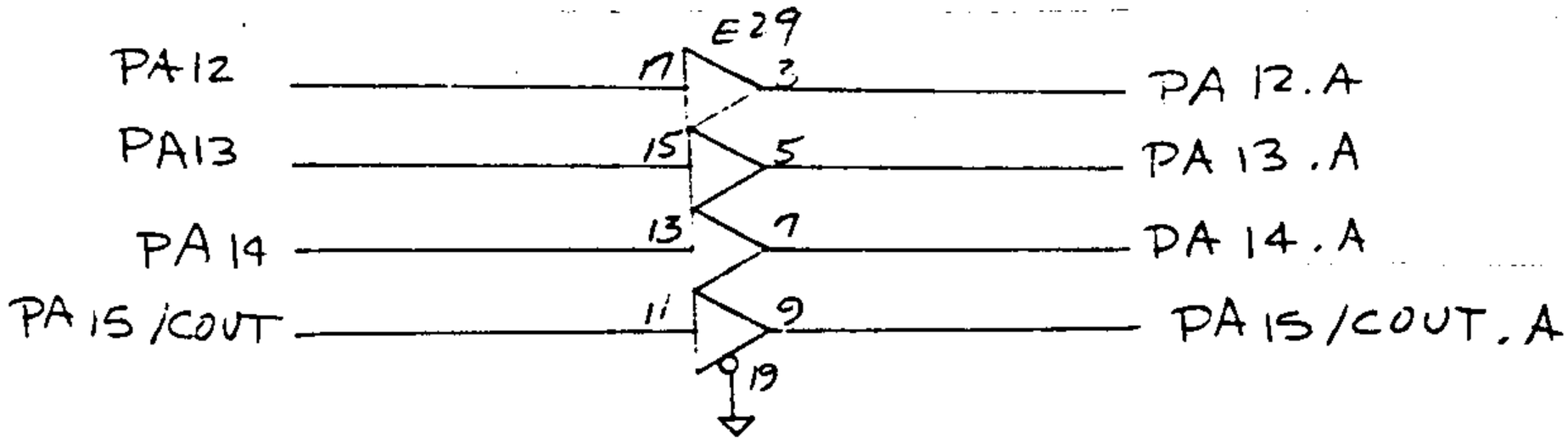
DRAM

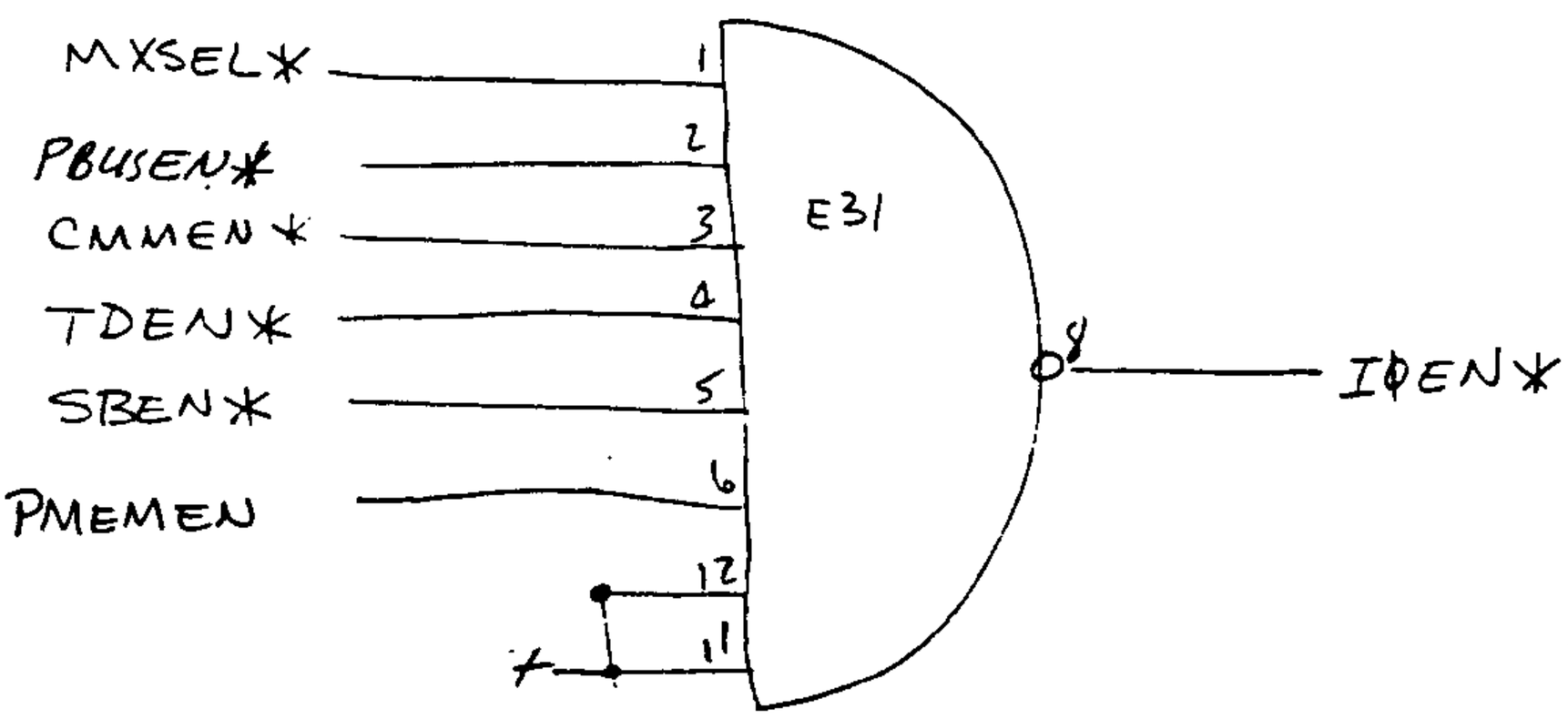

257
K13
PA08
PA00
PA09
PA01
PA10
PA02
PA11
PA03
PA12
PA04
PA13
PA05
PA14
PA06
PA15/EOUT
PA07
MUX
MXSELX
257
K14
RA7
RA6
RA5
RA4
RA3
RA2
RA1
RA0
K11
A
K11
B
REFCY
MXSEL
K12
K12
DRAM

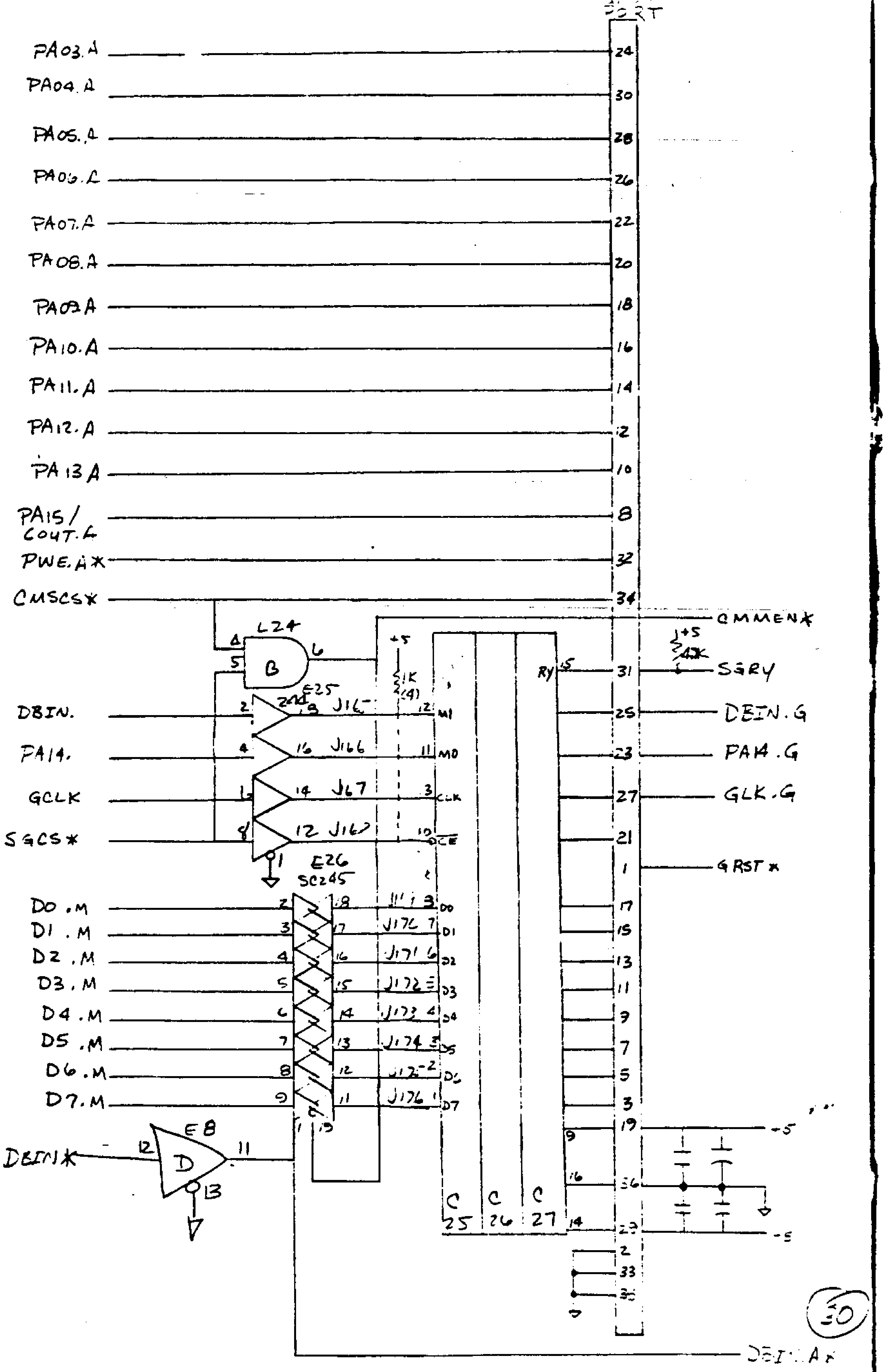

D0.M
D1.M
D2.M
D3.M
D4.M
D5.M
D6.M
D7.M
IOEN*
E27
PDBIN
PWE*
PMEMEN*
CRUCLK*
D0
D1
D2
D3
D4
D5
D6
D7
PDBIN.A
PWE.A*
PMEMEN.A*
CRUCLK.A*
E27
PH3*
SCLK
IAQ/HDA
MSAST*
PH3.A*
SCLK.A
IAQ/HDA.A
MSAST.A*
E28
PA00
PA01
PA02
PA03
PA00.A
PA01.A
PA02.A
PA03.A

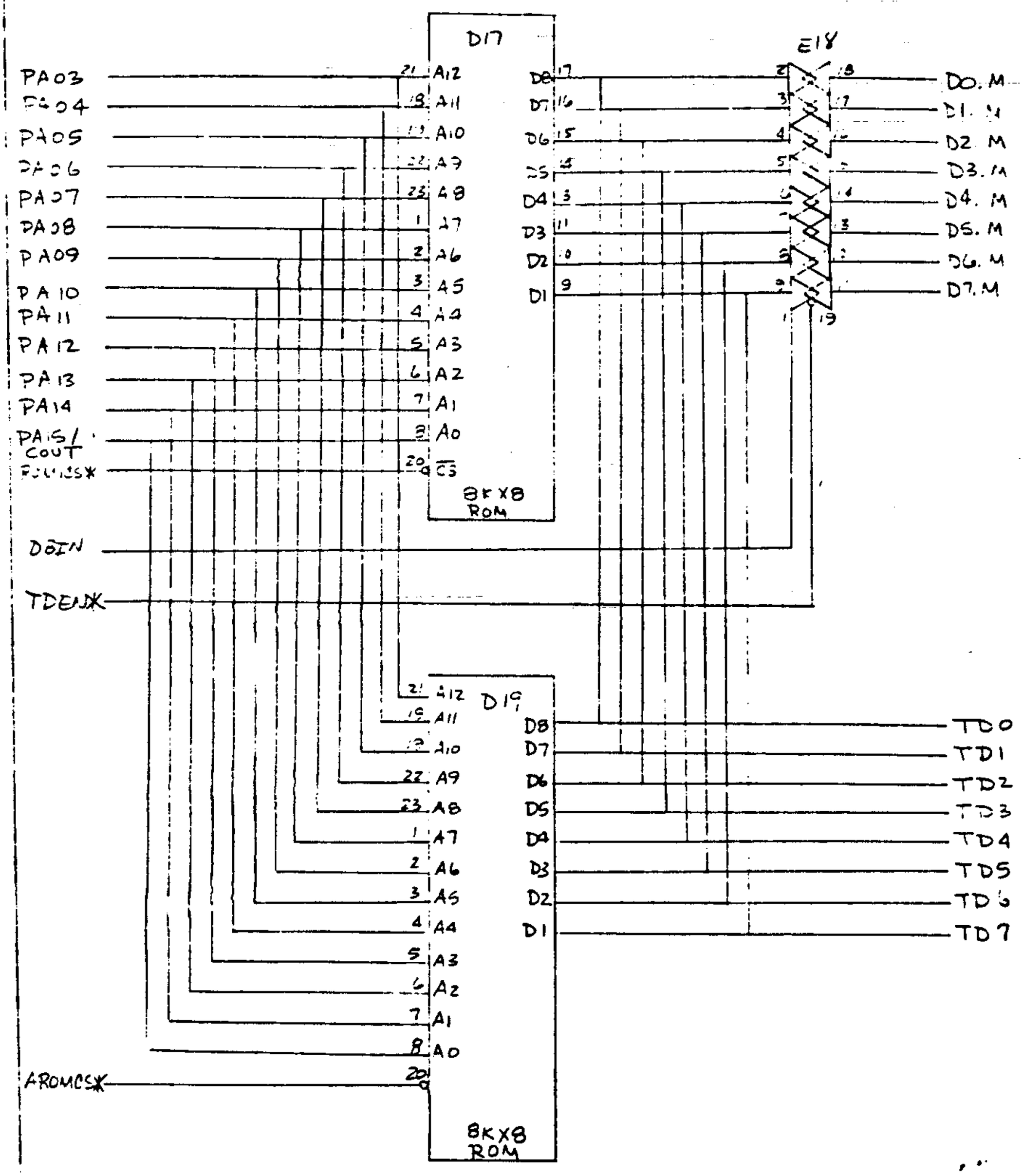

E28
PA04
PA05
PA06
PA07
17
15
3
19
3
5
7
9
PA04.A
PA05.A
PA06.A
PA07.A


E29
PA08
PA09
PA10
PA11
2
4
6
8
1
18
16
14
12
PA08.A
PA09.A
PA10.A
PA11.A

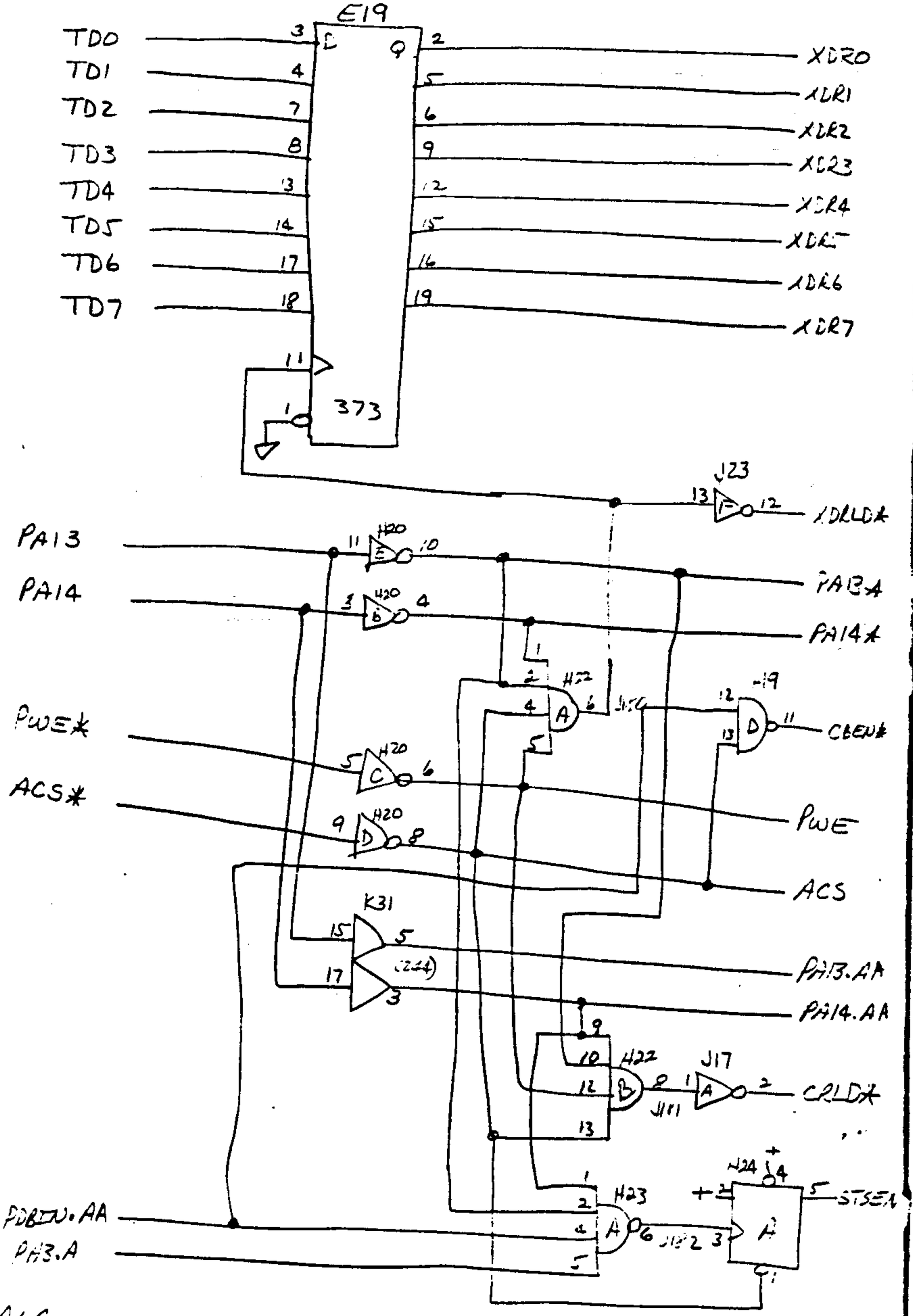

E29
PA12
PA13
PA14
PA15/COUT
17
15
13
11
19
3
5
7
9
PA12.A
PA13.A
PA14.A
PA15/COUT.A


MXSEL*
PBUSEN*
CMMEN*
TDEN*
SBEN*
PMEMEN
1
2
3
4
5
6
12
11
E31
8
IOEN*


PORT
PA03.A
PA04.A
PA05.A
PA06.A
PA07.A
PA08.A
PA09.A
PA10.A
PA11.A
PA12.A
PA13.A
PA15/
COUT.A
PWE.A*
CMSCS*
L24
B
E25
DBIN.
PA14.
GCLK
SGCS*
J165
J166
J67
J167
E26
SC245
D0.M
D1.M
D2.M
D3.M
D4.M
D5.M
D6.M
D7.M
E8
D
DBIN*
+5
1K
(4)
M1
M0
CLK
CE
D0
D1
D2
D3
D4
D5
D6
D7
J176
J171
J172
J173
J174
RY
C 25
C 26
C 27
CMMEN*
+5
4.7K
SGRY
DEIN.G
PA14.G
GLK.G
GRST*
+5
-5
DEIN.A*

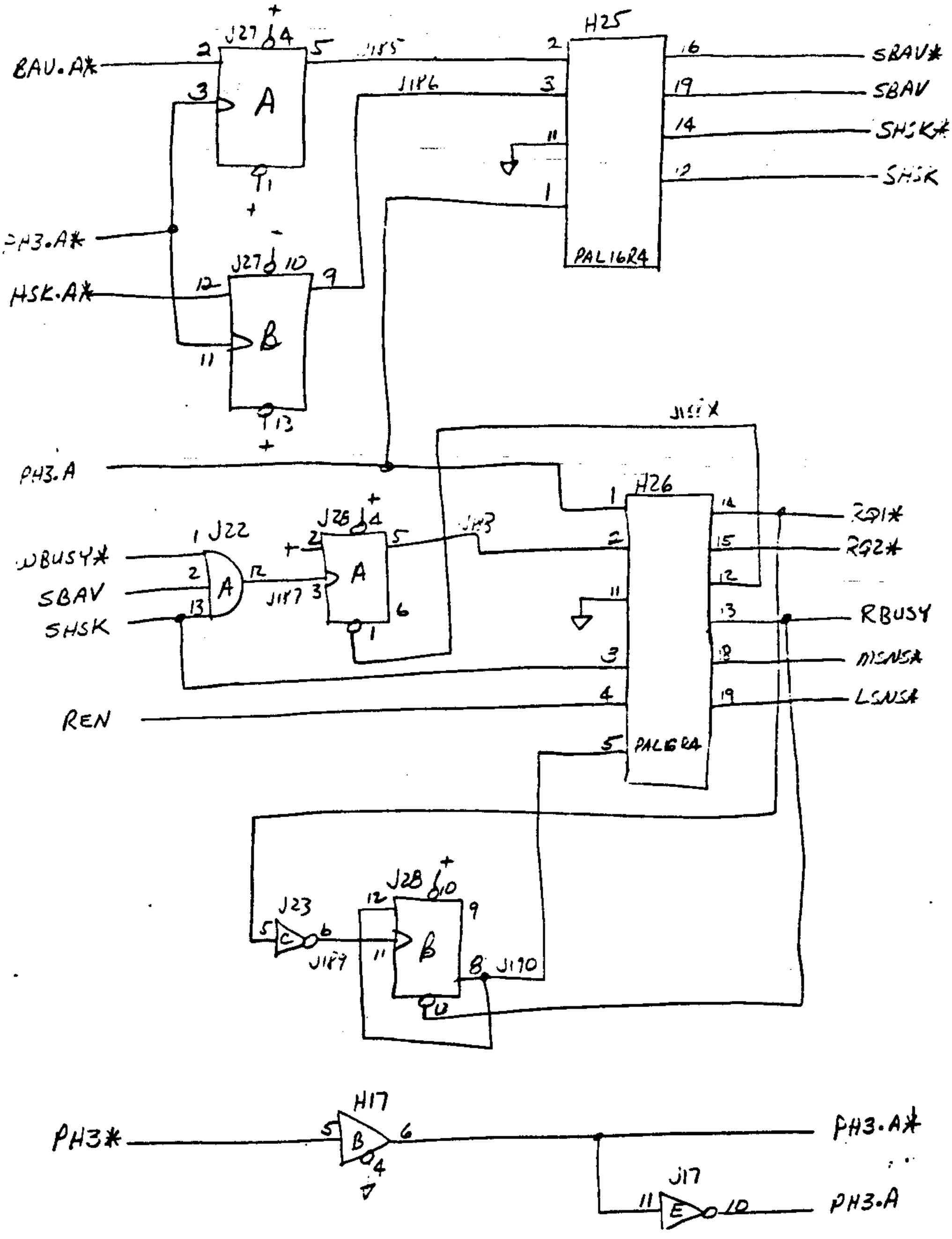

D17
PA03
PA04
PA05
PA06
PA07
PA08
PA09
PA10
PA11
PA12
PA13
PA14
PA15/ COUT
FCLKCSX*
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
CS
8K X 8 ROM
D0
D7
D6
D5
D4
D3
D2
D1
E18
D0. M
D1. M
D2. M
D3. M
D4. M
D5. M
D6. M
D7. M
DOIN
TDEJX
D19
TD0
TD1
TD2
TD3
TD4
TD5
TD6
TD7
AROMCSX
8KX8 ROM

PAS ROM



ALC

XMIT DR, Reg Decodes



HLC

(33)

BAU, HSK sync, REN = state counter logic

XDRLD*

PH3.A*

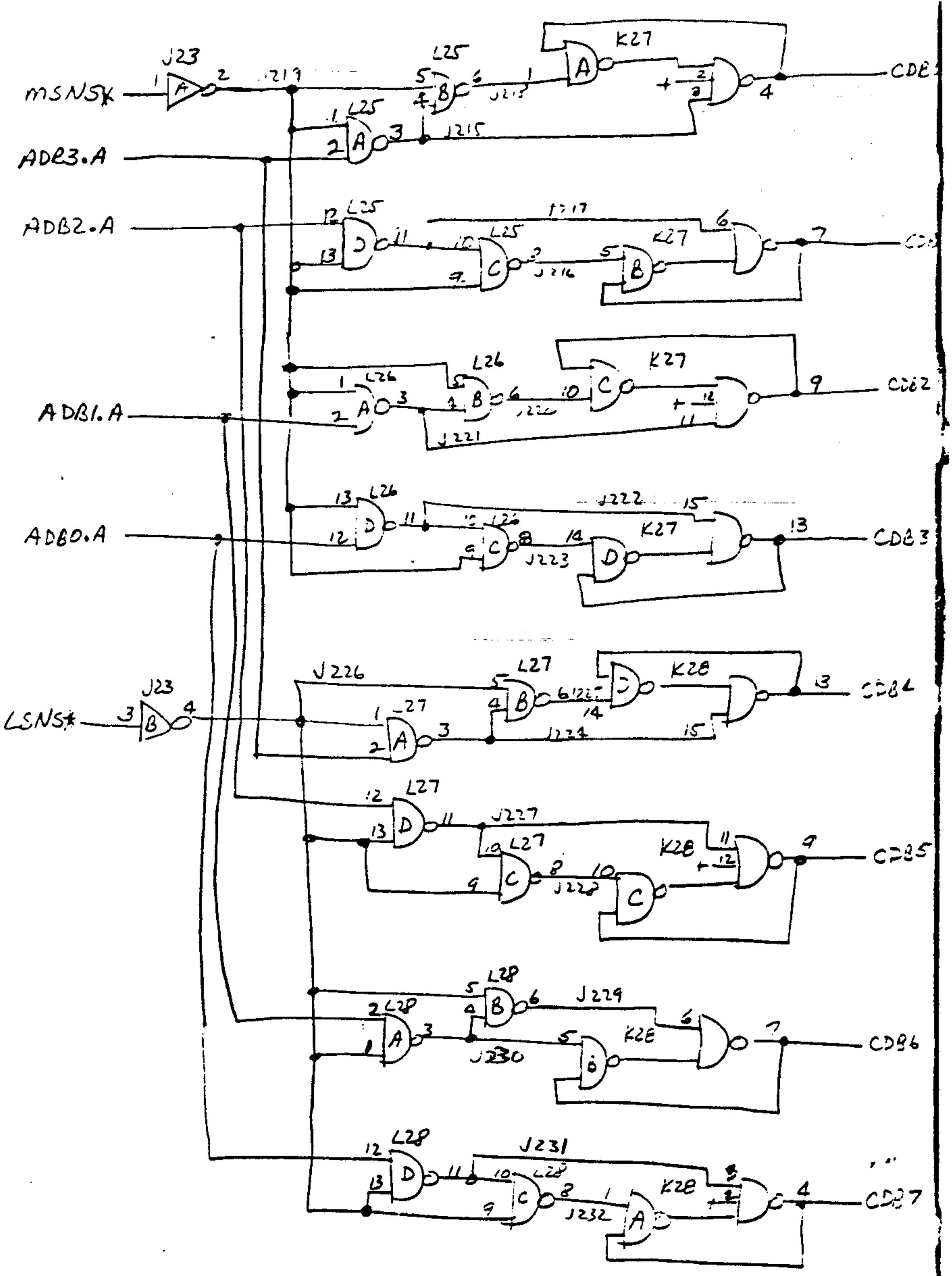
WEN

PH3.A

S-SK.

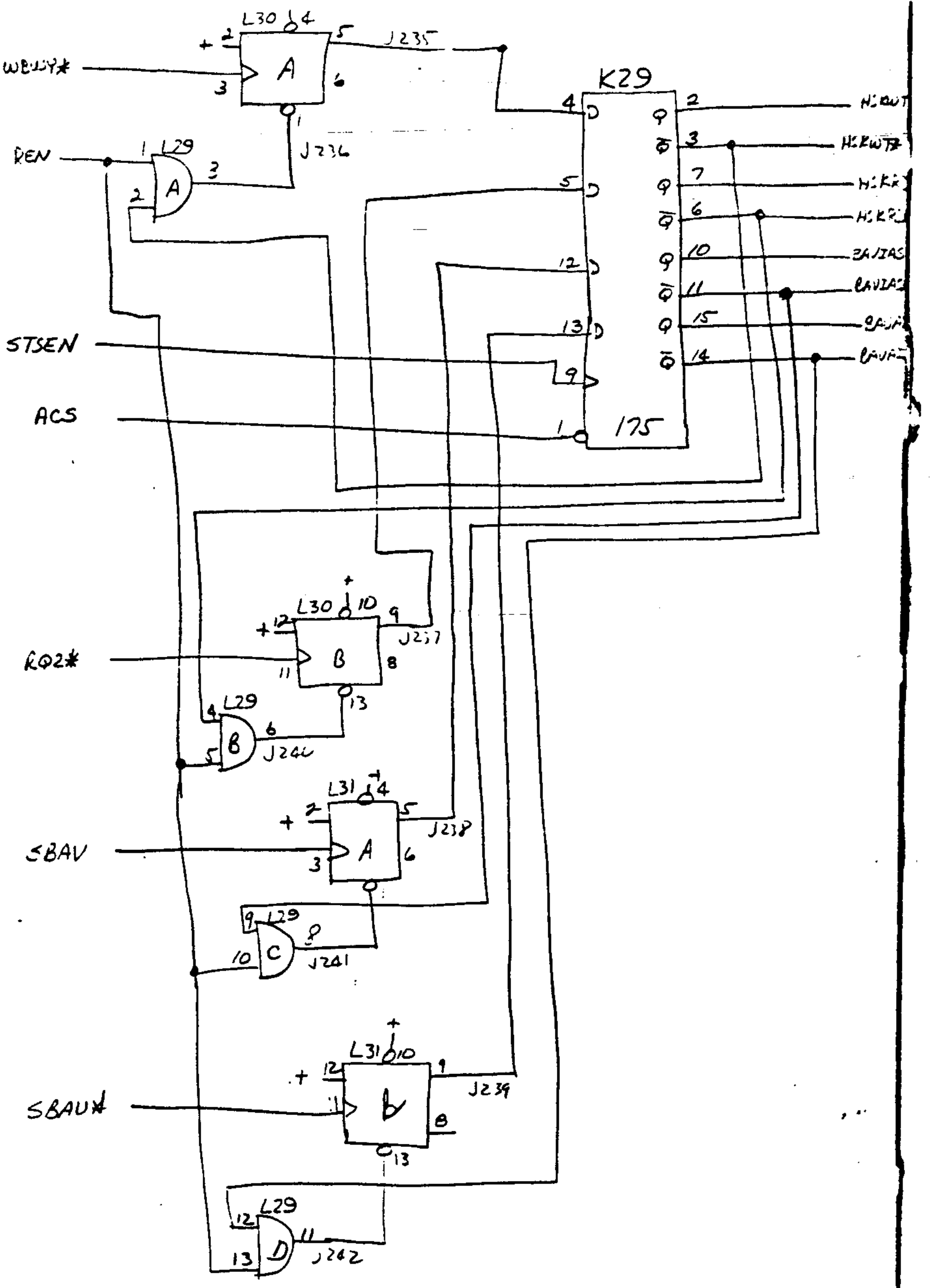
ALC

WRITE State Counter



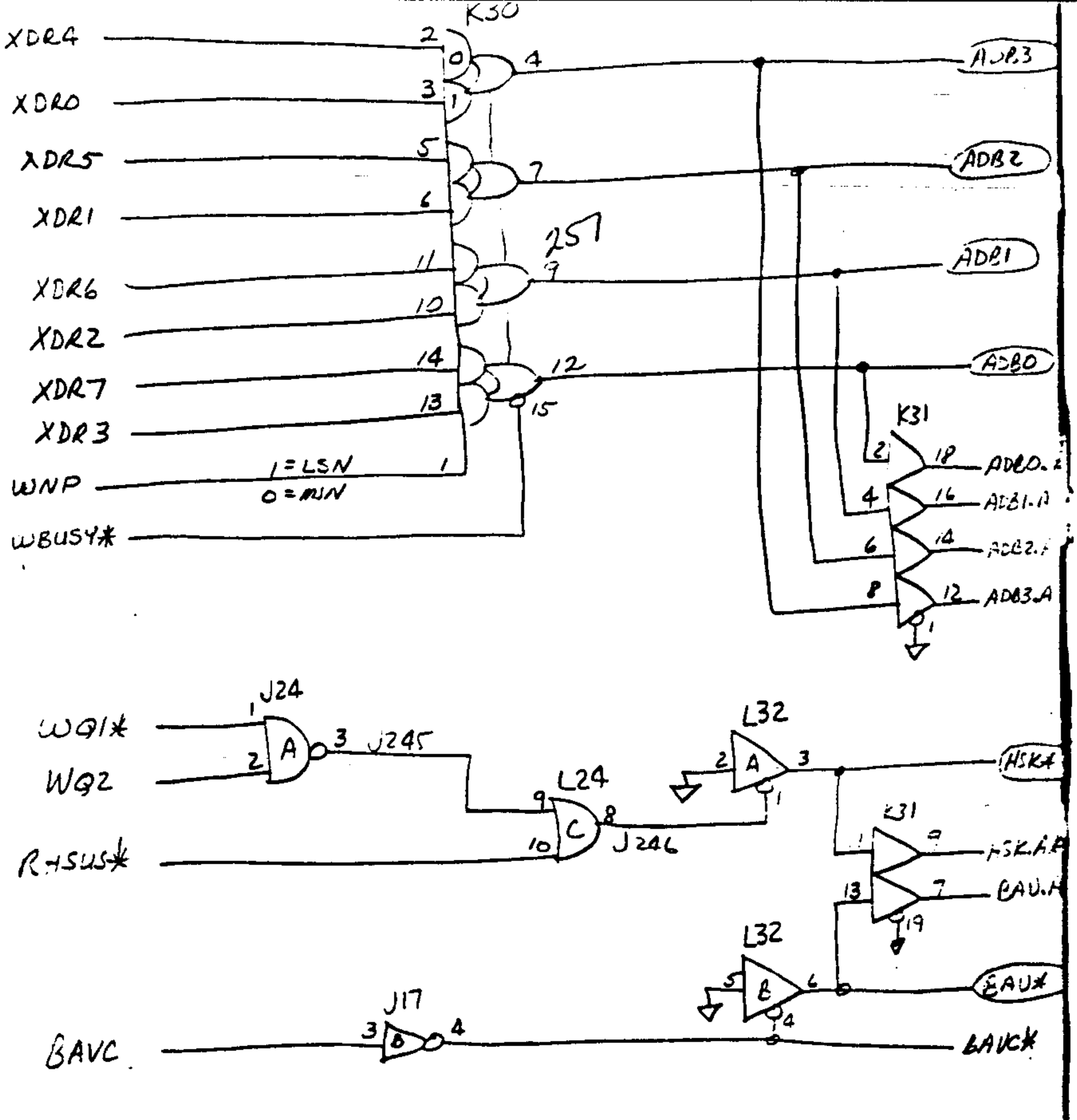
ALC

ALC RCHD REG



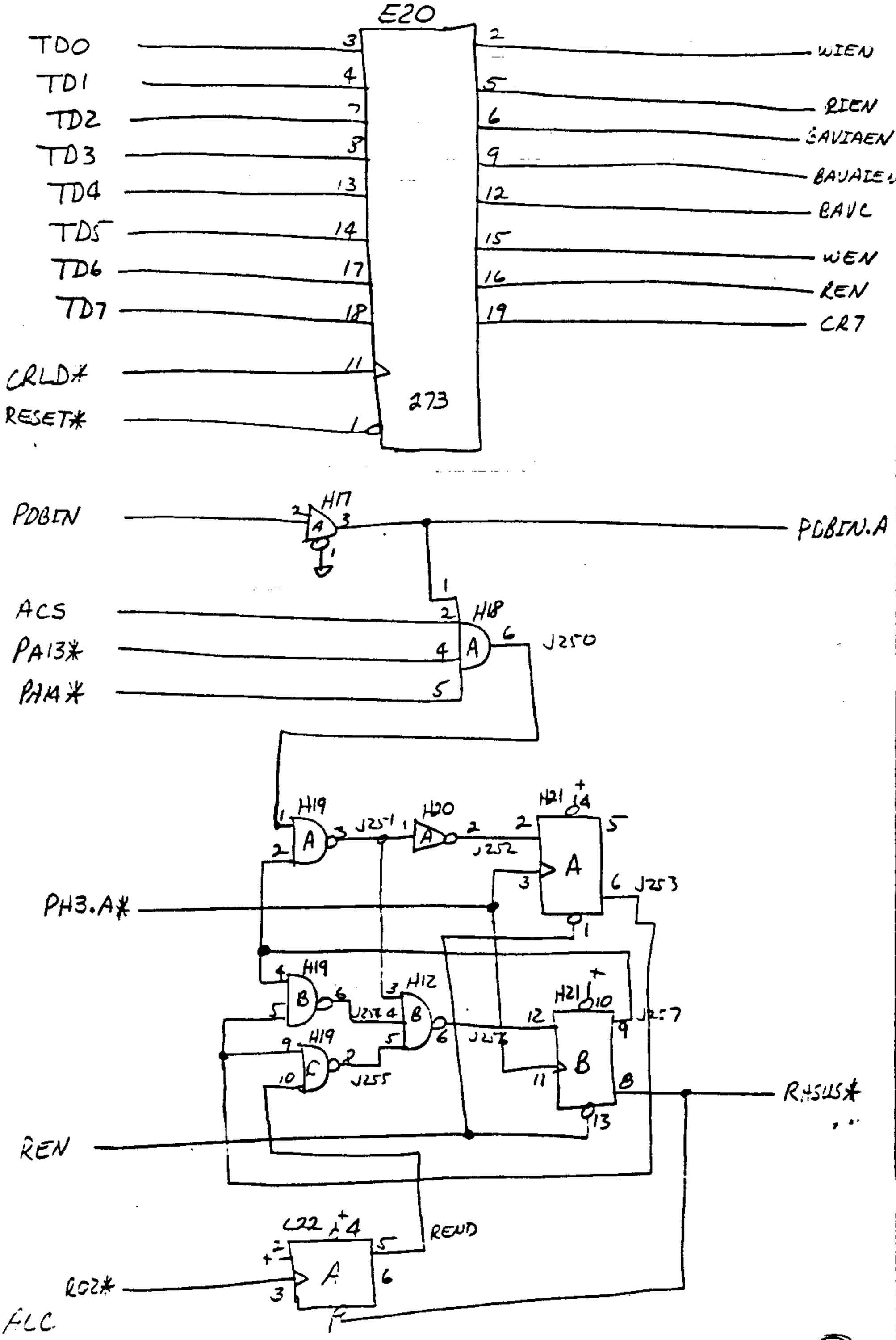
ALC

Status Reg Sense w/ RESET

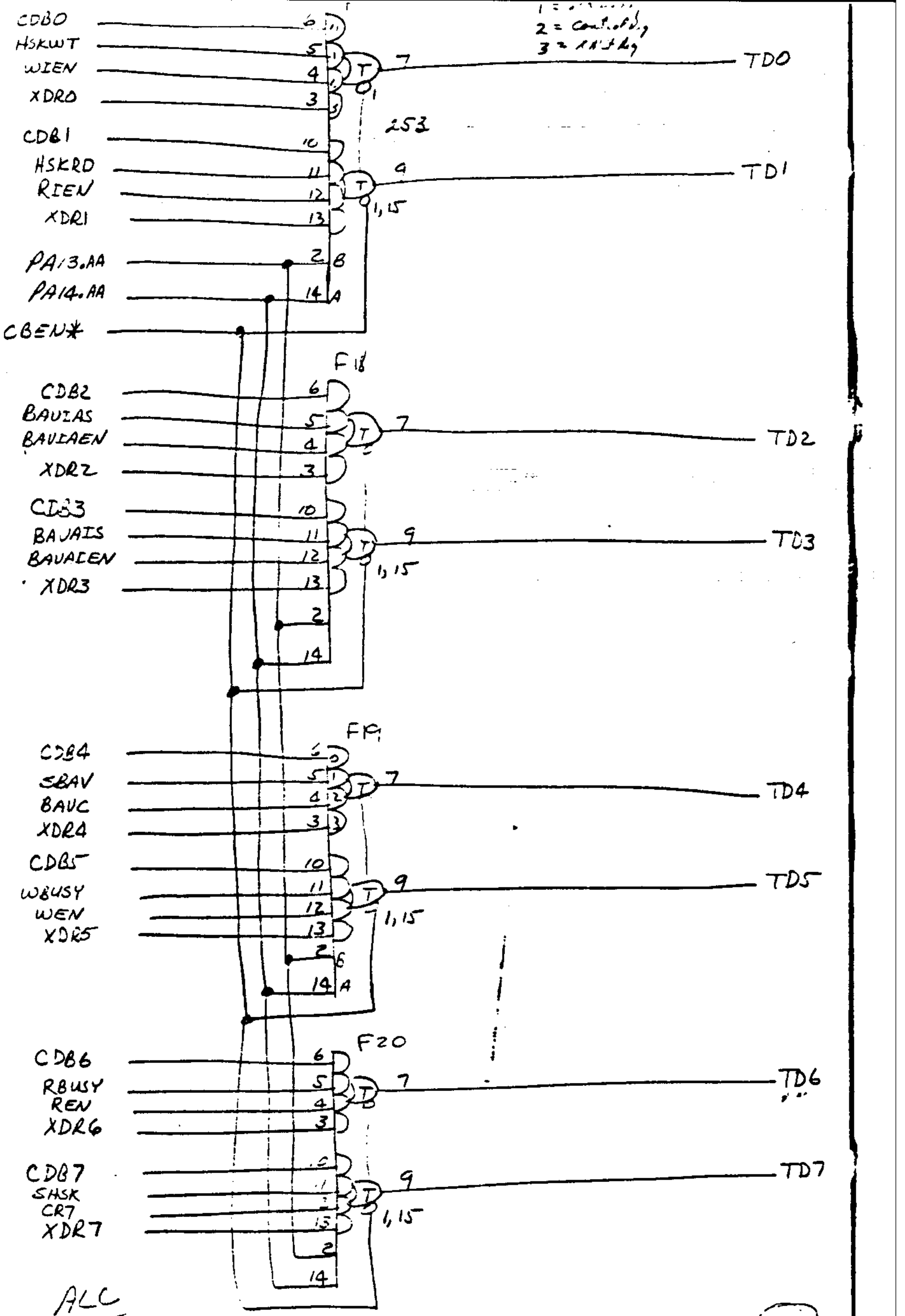


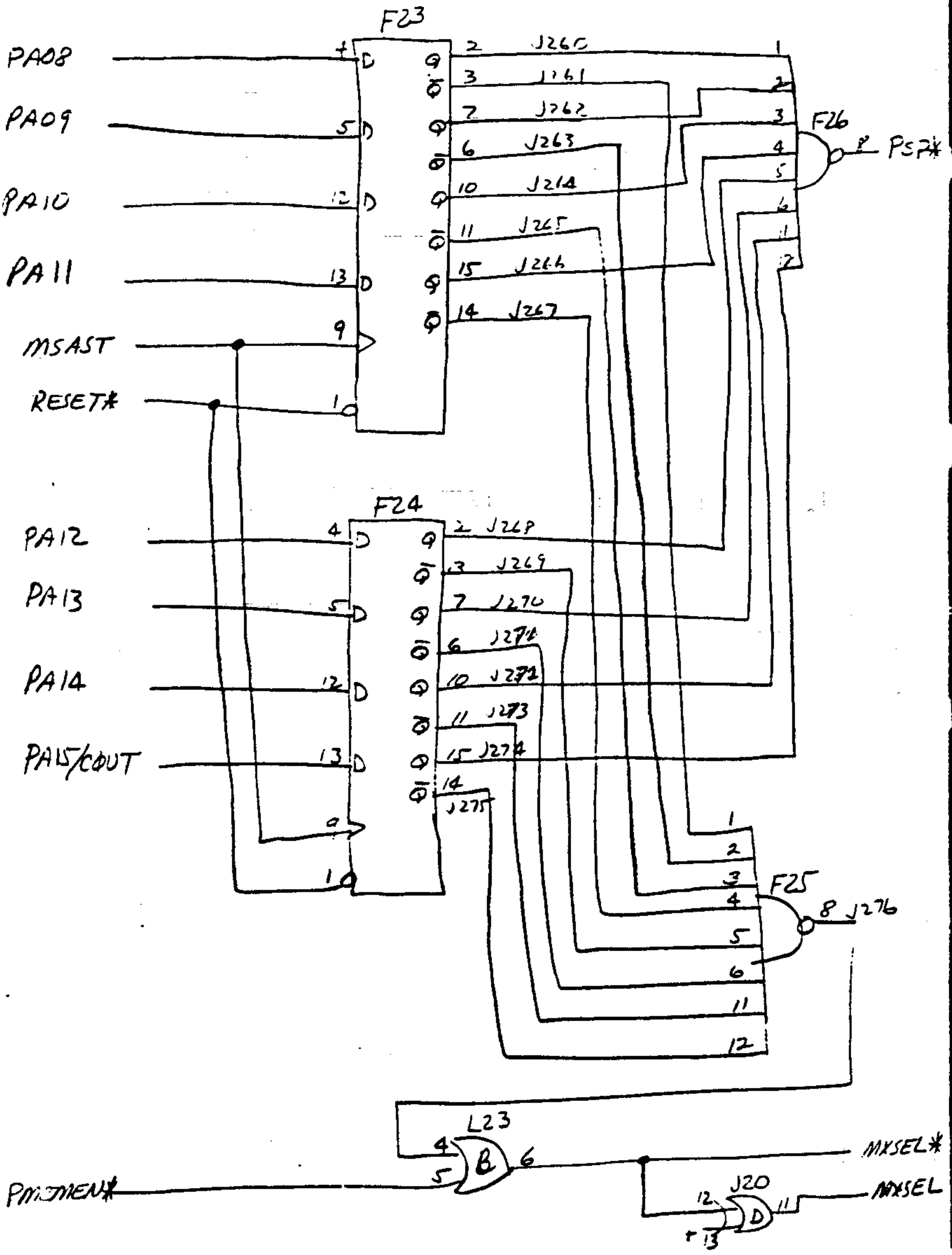
ALC

ALC Data Bus, HSK, EAV

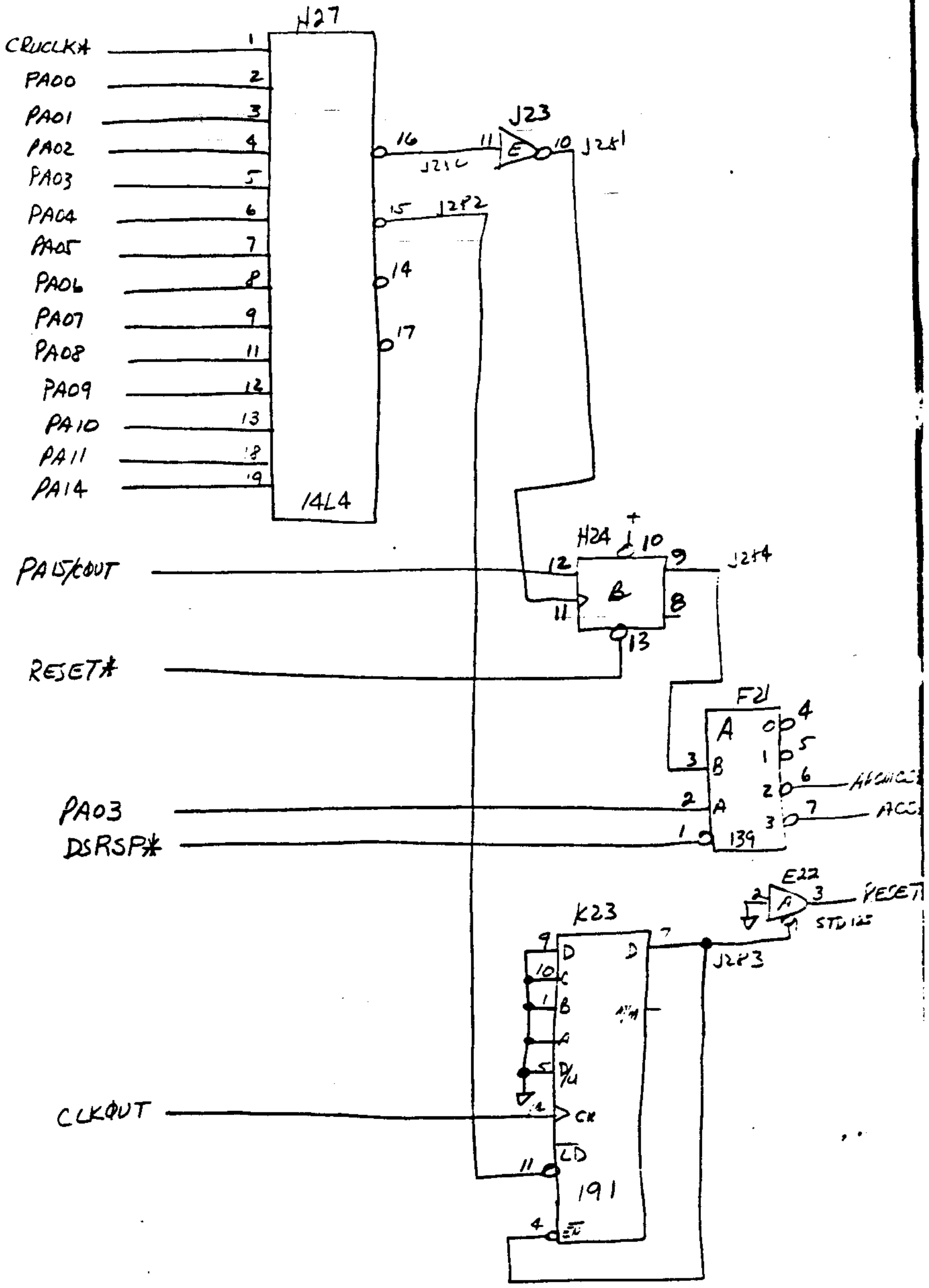


Central Reg Unit HSK Sentinel Logic


CDBO
HSKWT
WIEN
XDRO
CDB1
HSKRD
RIEN
XDR1
PA13.AA
PA14.AA
CBEN*
CDB2
BAUIAS
BAUIAEN
XDR2
CDB3
BAUAIS
BAUAIEN
XDR3
CDB4
SBAV
BAUC
XDR4
CDB5
WBUSY
WEN
XDR5
CDB6
RBUSY
REN
XDR6
CDB7
SHSK
CR7
XDR7
TDO
TD1
TD2
TD3
TD4
TD5
TD6
TD7
253
F18
F19
F20
ALC
39

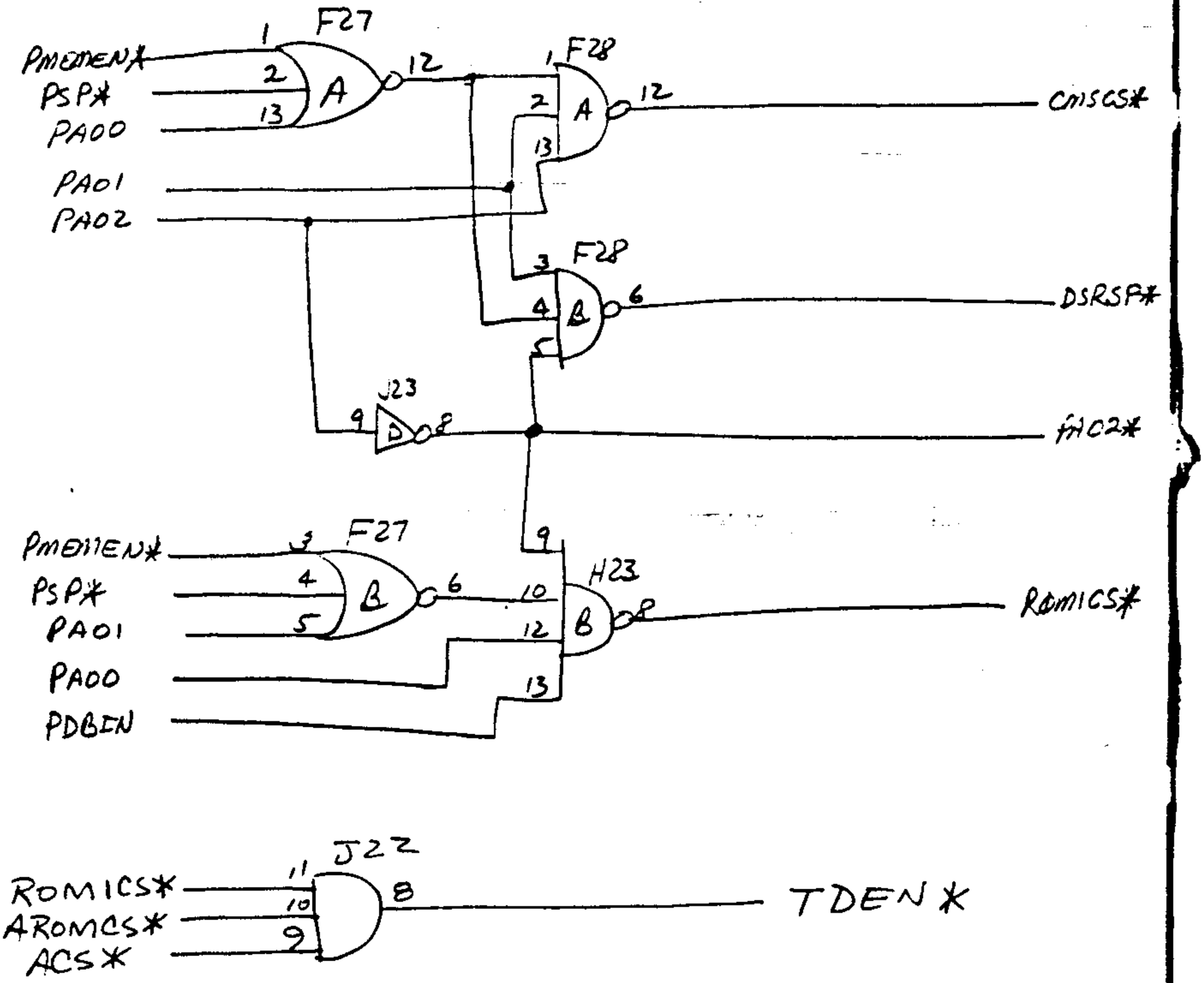

F23
PA08
PA09
PA10
PA11
MSAST
RESET*
J260
J261
J262
J263
J264
J265
J266
J267
F26
PSP*
F24
PA12
PA13
PA14
PA15/COUT
J268
J269
J270
J271
J272
J273
J274
J275
F25
J276
L23
PRIMEN*
MXSEL*
J20
MXSEL

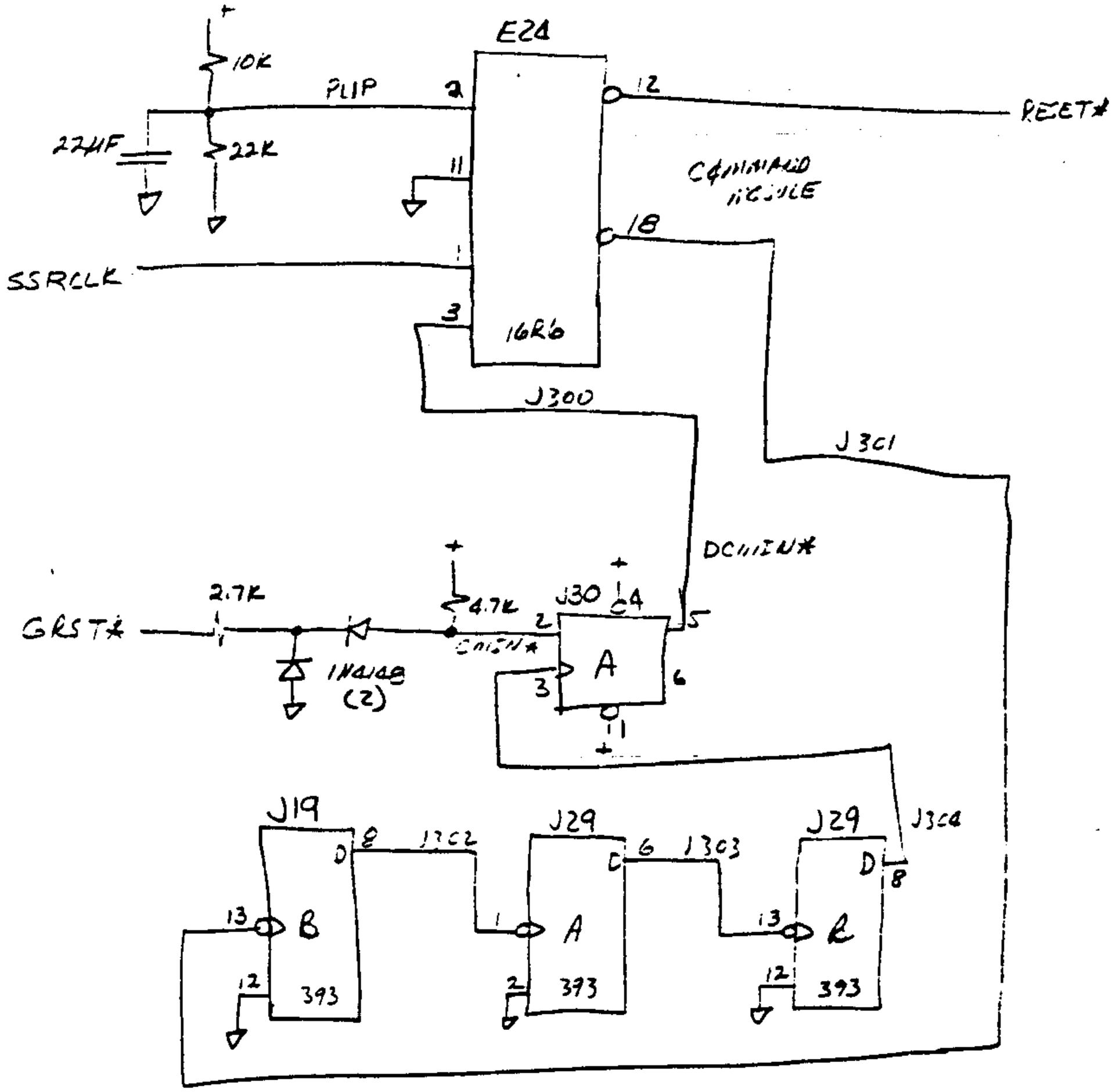
PAS Decode



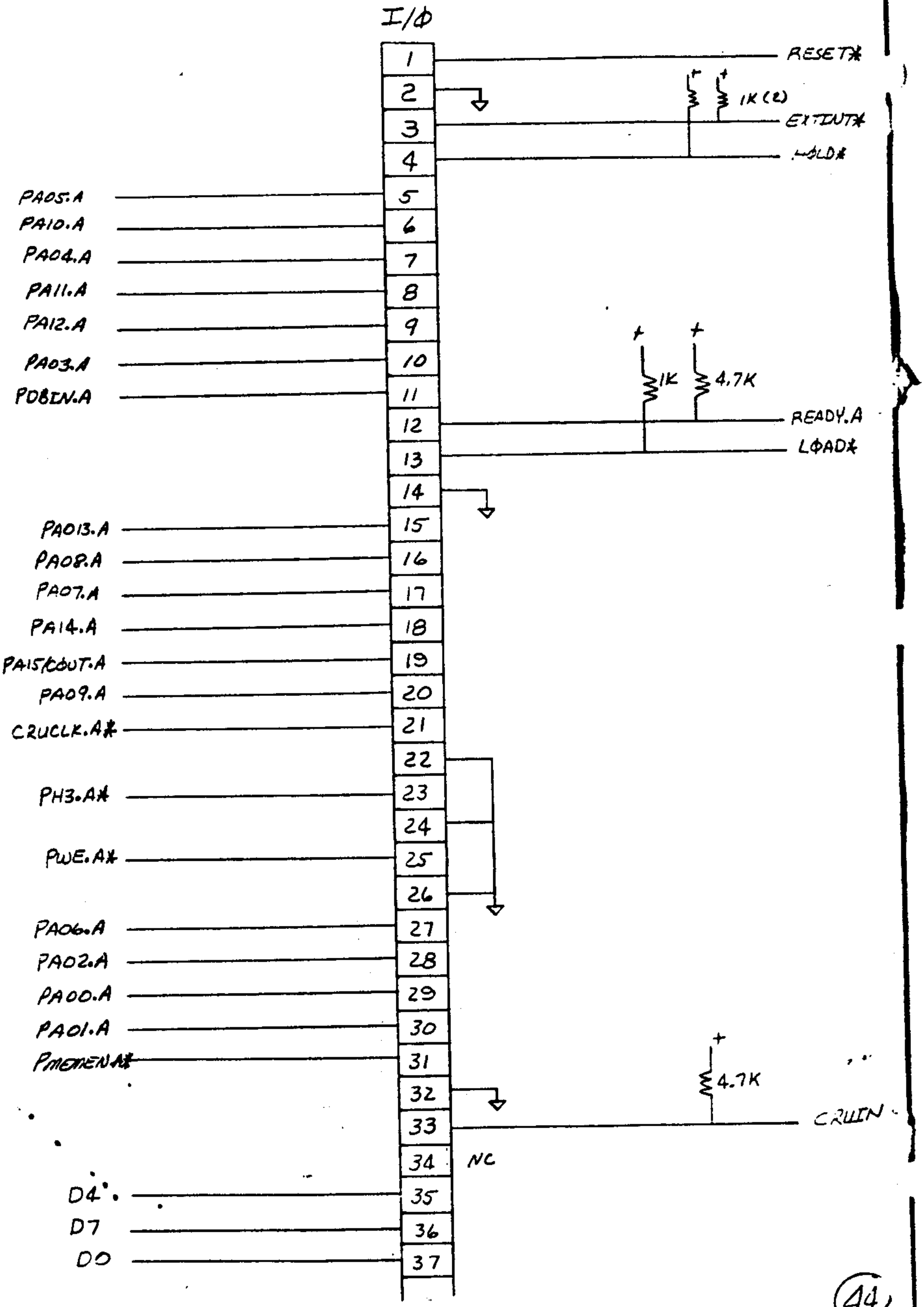
CRU DECODES

(7.1)


F27
PMEMEN*
PSP*
PA00
PA01
PA02
F28
F28
J23
CMISCS*
DSRSP*
MIO2*
F27
PMEMEN*
PSP*
PA01
PA00
PDBIN
H23
ROMICS*
J22
ROMICS*
AROMCS*
ACS*
TDEN*



COMMAND MODULE RESET


I/Φ
1
2
3
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18
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21
22
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24
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26
27
28
29
30
31
32
33
34
35
36
37
RESET*
1K (2)
EXTINT*
HOLD*
PA05.A
PA10.A
PA04.A
PA11.A
PA12.A
PA03.A
PDBIN.A
1K
4.7K
READY.A
LOAD*
PA013.A
PA08.A
PA07.A
PA14.A
PA15/COUT.A
PA09.A
C2UCLK.A*
PH3.A*
PWE.A*
PA06.A
PA02.A
PA00.A
PA01.A
PMEMEN.A*
4.7K
CRUIN
NC
D4
D7
D0
44
I/Φ CONN