TI 99/7 COMPUTER
HARDWARE THEORY OF OPERATION

Corporate Engineering Center
Dallas

By Richard Tarrant

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RELATED DOCUMENTS

The following documents are important to understanding the theory of operation of the 99/7:

Reference	Title
1	Texas Instruments Home Computer Technical Data Manual
2	TMS 9918A Video Display Processor Preliminary Description
3	TMC 0430 Graphics Read Only Memory Specification 1015960
4	TMS 5200 (old TMS 0285) Voice Synthesis Processor Data Manual
5	TMS 6100 (old TMS 0350) Voice Synthesis Memory Data Manual
6	SN76489AN (TMS9919) Data Specification for the Sound Generator
6a	Application Report - A Guide to Using the Texas Instruments SN76489A Sound Generator
7	Texas Instruments (DSG) Specification Control Drawing 984039 "Keyboard, Unencoded, without Keytops"
8	TI EPN3621 Thermal Character Printhead Specification
9	TI DSG Dwg. LU2214191 "Description, PVOLTs IC" - functional description of 2543
9a	TI DSG Dwg. 2210840 "IC, Switching Voltage Regulator" - data sheet on 2543
10	TI DSG Dwg. LU2214194 "Specifications, Motor Drive IC" - func. descrip. 2444A
10a	TI DSG Dwg. 2210843 "Integrated Circuit, Motor Drive" - data sheet on 2444A
11	TI DSG Dwg. 999256 "Motor, Stepping Paper Drive"
12	TI DSG Dwg. LU2214192 "Specification, Power Good IC MOG 2613" - func. descrip. 2613
12a	TI DSG Dwg. 2211371 "Integrated Circuit,

Power Good" - data sheet on 2613

13 9900 Family Systems Design and Data Book

drive bus uses one half of its pins for signal ground; thereby, providing a ground-plane effect to reduce RFI emissions.

The keyboard and printer mount to the top side of the Up board; hence, are outside of the system shielding. Mounting brackets and two 12 pin signal connectors for the keyboard attach to the top of the Up board. Printer standoffs penetrate Up and Down boards to attach to bottom case plastics. Five connectors (predefined by the DSG printer assembly) attach to the top surface of the Up board.

COOLING AND THERMAL PROTECTION

Cooling is furnished by the standard 765 exhaust fan mounted in the left, rear of the case. Air inlet slots are provided under the front lip of the case and thru the front portion of the side panels. The fan is powered by -12 VDC supplied directly from the Power Supply board via a 3-pin connector.

Two temperature sensors mounted to the bottom side of the Up board provide a user warning then a power supply shutdown if overtemperature conditions occur within the shielded package. As shown on the the Up Board schematic Sheet 10 (UP BD SH.10), the sensors consist of normally closed switches (Curie-point controlled reed switches) which open at fixed temperatures. The Over Temperature Warning sensor opens at the lower temperature to provide a software-monitored user warning. When open, this sensor pulls -EXT INT (External Interrupt) low to generate a level 1 interrupt thru the TMS9901 to the TMS9900 CPU. The same signal(OVRTP) is provided as a high (logic "1") to the decoder chip U___ on UP BD SH.7. To implement the user warning feature, the software should always have EXT INT enabled, and upon receiving this interrupt, should poll OVRTP to verify that the temperature sensor caused the interrupt (EXT INT is also used by the RS-232). Polling of OVRTP consists of setting the TMS9901 P14/P13/P12 outputs to 111 and testing 9901 INT6 for the decoded OVRTP value. The software may then generate a user message to warn of the rising temperature condition (maybe due to failed fan or blocked air inlets).

NOTE: -EXT INT will remain low as long as the warning sensor is open; therefore to avoid further interrupts, 9901 INT1 must be software masked and cannot be used by the RS-232.

The second temperature sensor, Over Temperature Power Shutdown, (UP BD SH.10) opens at a higher temperature and interfaces directly to the system power supply thru an optically-coupled SCR (on the Power Supply board). The opening of this sensor will cause an abrupt shutdown of the power supply. The supply can only be brought back up by waiting for the sensor to re-close at a lower temperature and turning the console power switch Off then back On.

BUS STRUCTURE

As shown in Figure 1 several different buses are used in the 99/7. The standard TMS9900 bus with 16 bit-wide data path is used for the fastest directly accessable CPU memory. As in the 99/4 the data bus is narrowed to 8 bits for use by the rest of the system including device service ROM's, GROM, Sound, and Speech. The multiplexing of the data bus adds 4 wait states to memory residing on the 8 bit path (see Ref. 1 for timing). Additional wait states are used by GROM, Sound, Speech, and some peripherals (discussed in later sections).

The 8 bit data path is further divided into a TTL level and a MOS signal level bus thru U85 CMOS Buffer (74C245) and U84 (74LS245) as shown on DN BD SH. 4 schematic. This is done to eliminate the offset ground and data pullup circuits which would otherwise be necessary to interface to the P-cannel GROM memories, Sound, and Speech chips. This MOS level bus (MOSD0-MOSD7) extends to the Up board to interface the external GROM port. The TTL level bus interfaces to the N-channel device ROM's on the Up board and on the Mezzanine board.

As shown on DN BD SH. 7 schematic, the full 15 signal Address bus (A0-A14) plus A15/CRUOUT (added by the bus multiplexing logic) extends to the Up board. CRUIN and CRUCLK supply CRU capability to the Up board. All memory control lines connect to the Up board including MEMEN, DBIN, and WE. Signals supplied to the 60 pin I/O connector, but not used by the Up board are LOAD and IAQ, both of which may be used in external test circuits such as TIBUG.

INTRODUCTION

The TI 99/7 computer incorporates the 99/4 home computer mainframe architecture with 99/4 peripheral controllers plus expanded memory into the case plastics of the Digital Systems Group 765 terminal for compactness and portability. The 99/7 will retain software compatibility with the 99/4 while providing additional faster-access memory as well as a larger keyboard and 80 column printer.

Figure 1 shows a detailed block diagram of the 99/7. A comparison of features between a 99/4 with its external peripherals and the 99/7 is as follows:

	99/4	99/7
Operating System ROM	8k/0.7(W)*	8k/0.7(W)
Workspace RAM	256/0.7(W)	512/0.7(W)
Display (VDP) RAM	16k/8.0(B)	16k/8.0(B)
Internal GROM	18k/6.0(B)	90k/6.0(B)
Sound	TMS9919	TMS9919
Keyboard	40 key polled	58 key+4 rock. sw. poll or interrupt
Video Display	40 char x 24 line color NTSC (VDP)	40 char x 24 line color NTSC (VDP)
Cassette Interface	1 port 650 baud 2 unidirect. mtr. cntr.	1 port 650 baud 2 bidirect. m.c.
Joystick Interface	Dual scan/1 port	Dual scan/1 port
External I/O	40 pin full cpu with 8 bit data	9 pin with 8 bit latched data
Expansion CPU RAM	32k/2.0(W)**	64k/0.7(W)
Speech	TMS0285+ 2-TMS0350**	TMS0350+ 2-TMS0350
Printer	32 col/30 cps**	80 col/30 cps
Disk Controller (drives external)	3-single density single side**	3-single density single/double side
RS-232	Dual 9600 baud**	Dual 9600 baud
Modem	300 baud acoustic originate**	300 baud acoustic originate/answer

* memory in bytes/microseconds access per (Word) or (Byte)
** external peripheral unit required

Details of the above 99/7 features are described in sections which follow.

PHYSICAL CONFIGURATION

The 99/7 logic hardware is split between two main circuit boards, the DOWN (or CPU) board and the UP (or Peripheral) board. These 2 printed wire boards are form-fitted to the 765 case plastics and use the predefined 765 board, printer, and keyboard standoffs. Additional standoffs have been added between the 2 boards to accomodate more severe vibration. See Figure 2.

Two smaller boards mount to the main boards. The Power Supply board mounts to the top, rear part of the Up board where case height is available near the fan cavity for the transformer. DC power is fed thru a staked-pin connector to the Up board and then via #18 AWG cable to the Down board. The optional Mezzanine board for future expansion mounts to the top of the Down board and is connected thru staked connectors to signal and power.

All connections to the outside world are made thru connectors mounted to the Up board. The Up board is mounted even with the case side-panels which provide convenient hole penetrations to the outside. Hence, all peripheral circuits which require outside connectors are located on the Up board. Three cable connectors provide interconnection between Up and Down boards; these are 8-pin Video, 60-pin I/O (signal), and 10-pin Power Interconnects.

RFI SHIELDING

Radio Frequency Interference shielding to meet FCC Class B (Consumer product) requirements is provided by a physical shield and extensive signal filtering. The shield consists of a metal pan which sits in the bottom of the case plastics and extends upward around the sides to enclose the Down board. The shield mates with the bottom outer edges of the Up board. The Up board is multilayer with a solid shield plane (with the exception of holes for component leads, connectors, and standoffs) on top to provide the shield "lid".

Signal filtering consists of a combination of T-filters, rise time minimization, extensive bypass filtering, and ground plane utilization. The T-filters are used on particularly noisey outgoing lines such as the keyboard, printer, RS-232, and Auxiliary Port signals. The T-filter may be 2 ferrite inductors or two 150 ohm resistors with a .001 or .01 microfarad capacitor in between to shield ground. The resistors provide equivalent impedance to the ferrites at 5 MHz and are smaller and cheaper, but can't be used where TTL signal levels must be preserved. The larger capacitor is used where signal risetime is not a factor. Risetime minimization is provided by series resistors in signal bus lines. This slows the usual TTL risetimes to reduce high frequency harmonics and also supplies some impedance matching to dampen line reflections and negative-going signal undershoots. Bypass filtering of voltage buses to ground consists of .01 or .1 microfarad capacitors between most IC power pins and ground. All memory chips have bypass caps on each voltage. Additionally, bulk capacitors of 22 (10 on +12v) microfarads are provided for approximately every 4 IC's. The disk

SYSTEM MEMORY

MEMORY MAP

System memory consists of memory located within the 64k byte CPU address space, memory in an additional 64k mappable-into-CPU space, and memory outside the normal CPU address space but accessable thru memory-mapped I/O techniques.

The CPU address space is allocated as follows:

STANDARD 99/4 CONFIGURATION	ADDITIONAL 64K SPACE		
ADR XOOO	1XOOO	*MAPPED I/O IN 8000-A000	
0			
CONSOLE ROM	8K RAM	8200-82FF	ADDED 256 BYTE WORKSPACE STATIC RAM
2		8300-83FF	STANDARD 99/4 256 BYTE WORKSPACE STATIC RAM
OPEN	8K RAM	8400	SOUND
4			
PERIPHERAL DSR ROM	8K RAM	8800	VDP READ DATA
6		8802	VDP READ STATUS
CARTRIDGE ROMG/RAM	8K RAM	8C00	VDP WRITE DATA
8		8C02	VDP WRITE ADDRESS
WSP RAM, MAPPED I/O*	8K RAM	9000	SPEECH READ
A		9400	SPEECH WRITE
OPEN	8K RAM	9800	GROM BANK 0 READ DATA
C		9802	GROM BANK 0 READ ADDRESS
OPEN	8K RAM	9C00	GROM BANK 0 WRITE DATA
E		9C02	GROM BANK 0 WRITE ADDRESS
OPEN	8K RAM	9820	GROM BANK 8 READ DATA
F		9822	GROM BANK 8 READ ADDRESS
		9C20	GROM BANK 8 WRITE DATA
		9C22	GROM BANK 8 WRITE ADDRESS
		9900	PASCAL GROM READ DATA
		9902	PASCAL GROM READ ADDRESS
		9D00	PASCAL GROM WRITE DATA
		9D02	PASCAL GROM WRITE ADDRESS

At power-up or upon a LOAD interrupt signal, the memory mapping hardware (DN BD SH.2 schematic) is cleared by the -RST/LD signal to U2. This zeros MAPON, thereby routing A0,1,2 thru U12 around the Mapping RAM U11 and into the system as A'0, A'1, and A'2. A00 is also held at zero. The result is that the system powers-up to appear as standard 99/4 memory (left column of above memory map). LOAD interrupt on the 60 pin I/O connector also accomplishes this to allow external TIBUG memory into CPU space E000-FFFF.

In order to map any of the 8k RAM blocks into the OPEN 99/4 CPU logical address space or move any standard 99/4 space to other logical addresses, it is necessary to program the memory mapper RAM U11 (74S189) thru the CRU-addressed latch U2 (74LS259). The latch has a CRU base address of >0040 (or >0050, >0060, or >0070) as decoded by U13 (74LS138) to yield -MAPDATA. A12-A14 then address the 8 specific bits of the latch. Using >0040 base address, the following CRU to mapper RAM input results:

CRU ADR	U2 LATCH OUTPUT	U11 MAPPER RAM INPUT	U11 MAPPER RAM OUTPUT	
0040	Q0	---	---	MAPON
0042	Q1	D1	A'2	
0044	Q2	D2	A'1	
0046	Q3	D3	A'0	
0048	Q4	D4	A00	
004A	Q5	ADB (A2)	---	
004C	Q6	ADC (A1)	---	
004E	Q7	ADD (A0)	---	

NOTE: In keeping with 99/4 convention, CRU addresses assume a 16 bit address format which makes hardware and software addresses identical, but are 2 times "conventional" 9900 CRU addresses, i.e.

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15
0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0

equals above >4A CRU address.

After the latch is setup with the mapper RAM address (ADB-ADD) and data (D0-D4), then -MAPWR is strobed with a CRU output to >0080 in order to write the data into the 74S189 RAM. Up to 8 of the 16 four bit RAM locations may be programmed in this manner. MAPON can then be activated by setting CRU output bit >0040. Until MAPON is turned off, the TMS9900 addresses A0-A2 will be converted to A'0-A'2 thru the mapper RAM.

A00 is the extra mapper-generated bit which specifically addresses the 64k expansion CPU RAM. Since A00 is also programmed as above, any 8k block of expansion RAM can be interchanged for any 8k block of memory in the low order 64k bytes of physical address space. Example:

With base adr (R12) = >40

	ADD	ADC	ADB	D4	D3	D2	D1	MAPON							
LDCR @LOC,8 of	1	1	0	0	1	0	0	0	X	X	X	X	X	X	X	X

followed by R12 = >80 and SBO 0 to strobe -MAPWR, will move GROM cartridge ROM (ROMG) from >8000->9FFF to >C000->DFFF when MAPON is activated with SBO 0 to >40.

and

With base adr (R12) = >40

	ADD	ADC	ADB	D4	D3	D2	D1	MAPON							
LDCR @LOC,8 of	1	1	1	1	0	1	1	0	X	X	X	X	X	X	X	X

followed by R12 = >80 and SBO 0 to strobe -MAPWR,
will move RAM block from physical address space >16000->17FFF
to CPU logical space >E000->FFFF when MAPON turns on with
SBO 0 to >40.

The contents of the mapper RAM can be read at any time thru a CRU input by setting the base address (R12) to >40 and storing the data as follows:

	ADD	ADC	ADB	D4	D3	D2	D1	MAPON							
STCR @LOC,8 of	ADD	ADC	ADB	D4	D3	D2	D1	MAPON	X	X	X	X	X	X	X	X

This causes U10 (74LS251) to multiplex the current ADB-ADD and MAPON from the U2 latch, along with the respective 4-bit D1-D4 from the mapper RAM, onto the CRUIN line. Additional RAM locations may be read by updating the latch RAM address via CRUOUT commands and repeating the CRUIN command.

ROM

ROM memory consists of TMS4732 4k ROM's located as follows:

PHYSICAL ADDRESS	CPU DECODE	CRU ENABLE	USE	SCHEMATIC LOCATION
0000-1FFF	-ROMEN	----	CONSOLE ROM even	DN BD SH. 2 U18
"	"	----	CONSOLE ROM odd	" U23
4000-4FFF	-MBE	1100	DISK DSR	UP BD SH. 3
5000-5FFF	"	1100	DISK DSR	"
4000-4FFF	"	1300	RS-232 DSR	"
4000-4FFF	"	1800	PRINTER DSR	"
4000-4FFF	"	1900	MEZZANINE DSR	MEZZ. BOARD
5000-5FFF	"	1900	"	"
6000-6FFF	-ROMG	----	GROM CARTRIDGE ROM	UP BD SH. 9
7000-7FFF	"	----	"	"

Console ROM timing is shown in Figure 3. EPROM ROM's may be substituted for masked ROM's (TMS2532 for TMS4732) in all locations. This requires that CS2 (pin 21) of all 4732 ROM's be masked-programmed as active high to correspond to Vpp of the EPROM's. The console ROM's have a 270 ohm resistor between CS2 and +5v to allow a jumper ground disable for test purposes.

STATIC RAM

Two contiguious 256 byte blocks of static RAM are located at >8200-82FF (DN BD SH. 2 U16, U21) and at >8300-83FF (U17, U22). The latter block corresponds to the Workspace RAM of the 99/4. Two each Motorola MCM 6810 RAM's (128x8) are located on the 16 bit data bus to give 128x16 or 256 bytes per block. The RAM's are enabled by

-WSPRAM (WorkSPace RAM). Timiing is shown on Figure 3.

EXPANSION RAM

Expansion RAM (DN BD SH. 6) can be configured as 32k bytes (16k x 16) using TMS4116 (16k x 1) dynamic RAM's or as 64k bytes (32k x 16) using TMS4532 (32k x 1) dynamic RAM's. The 4532 (sometimes called TMS4163) are partial 64k x 1 RAM's.

Use of the 4532's requires R47 be inserted to pick-up the eighth RAM address line RA7. Also, the jumpers must be inserted as shown on SH. 6 to supply Vcc to pin 8 and remove the +12v and -5v required for the 4116's. On Sheet 5 the 4532 jumper J2 to U39 pin 9 and J5 to U41 pin 9 must be inserted. All 4116 jumpers are removed. Since partial RAM's operate out of only one half of a full 4164 memory, the appropriate half is designated by the jumpers J3, J4 to U39 pin 11. See TMS 4532 Data Sheet (or equivalent OKI MSM3732).

Control for the Expansion RAM is shown on UP BD Sheet 5 schematic with timing shown in Figure 4. A memory cycle starts when -RAMSEL is decoded from -MEMEN*A00. -MEMEN going low shuts down the Refresh Timer U26 (74LS161) by causing the timer load input to go low. This inhibits further refresh until the cycle is over. The Address Multiplexor U39, U40 (74LS257) turns on with -RAMSEL while the output of the Refresh Counter U42 (74LS393) is gated off by U41 (74LS244). The Address Mux. multiplexes Row or Column address from the CPU address bus A'0-A14. Initially the Mux Flip Flop U24 selects Row address from A9-A14. -RAS is brought low by the RAS F-F and CPU clock Phase 3 to strobe Row address into the memories via RA0-RA7. Phase 4 then clocks the Mux F-F to shift the Address Mux. to Column addresses A'0-A7 which are then strobed into the memories via RA0-RA7 by -CAS going low at the next Phase 1 (U24). This then either causes the RAM's to place data on the CPU data bus (CD0-CD15) or causes the RAM's to write data into their cells (-W having gone low earlier with DBIN low to initiate an early write cycle). The memory cycle ends when -MEMEN goes high and releases -RAMSEL.

The Refresh Timer U26 starts a refresh cycle on the next Phase 3 after a memory cycle ends (the timer has been loaded with >E while -MEMEN low) by counting to >F and raising its carry output, REFEN. The next Phase 4 causes Ref RAS F-F U25 to bring -RAS low which strobes in the current Refresh Counter U42 count as the refresh address. The next Phase 3 counts the Timer to 0 and drops REFEN. Phase 4 then toggles Ref RAS F-F to raise -RAS, thus ending the refresh and incrementing U42 to the next refresh address. A refresh cycle will occur every 5.3 microseconds until another Expansion RAM memory cycle occurs. A 270 ohm pull down resistor on U42 clear pins is provided for test purposes. 33 ohm resistors in the memory address and control lines are designed to minimize signal undershoot transients.

DISPLAY RAM

Display RAM (or VDP RAM) consists of 16k bytes of dynamic RAM (eight

4116's) controlled by the Video Display Processor TMS 9918A. See DN BD SH. 1 schematic. As shown in the memory map, data is written to or read from this memory thru a memory-mapped I/O address after first loading the VDP with the appropriate Display RAM address. This memory is identical to the VDP memory of the 99/4. Memory cycle and refresh timing is described in the VDP Specification (Reference 2).

GROM

GROM (Graphics Read Only Memory) lies outside of the conventional CPU address space and is accessed thru memory-mapped I/O addresses shown in the memory map. This P-channel ROM with built-in address register (see GROM Spec. Ref. 3 for details) provides 99/4 Console BASIC in 3 chips, U86, U87(stack of 2, DN BD SH. 4). U86 is selected by -GROM SEL and supplies GROM Ready for all GROM's except the PASCAL System GROM's. Up to 8 GROM's can reside in one commonly decoded bank, each GROM being one page (Page address is masked-programmed into the GROM). Since U86 is a common page, the available pages are:

PAGE	BANK 0	BANK 8
0	CONSOLE BASIC CHIP 1	CONSOLE BASIC CHIP 1
1	CONSOLE BASIC CHIP 2	PASCAL INTERPRETER CHIP 1
2	CONSOLE BASIC CHIP 3	PASCAL INTERPRETER CHIP 2
3	GROM CARTRIDGE CHIP 1	PASCAL INTERPRETER CHIP 3
4	GROM CARTRIDGE CHIP 2	PASCAL INTERPRETER CHIP 4
5	GROM CARTRIDGE CHIP 3	
6	GROM CARTRIDGE CHIP 4	
7	GROM CARTRIDGE CHIP 5	

The PASCAL System GROM's are decoded independently of the above banks in order to provide a full 8 chip bank that corresponds to the 99/4 PASCAL System. U90 therefore provides Ready for these GROM's.

GROM RDY (GROM Ready) is generated by OR'ing the two chip readies and passing the result thru the U78 (74LS194) shift register to resolve any timing ambiguities (DN BD SH. 4). As shown in the GROM timing diagram (Figure 5), the chip Ready is normally low. This overcomes the slow internal logic problems of the P-channel memory, but requires chip Ready be AND'ed with chip select to provide an actual ready. Chip Ready only goes high on the 3rd GROM clock after chip select and stays high until chip select goes away. Since all GROM's on the same select activate their Ready, only one chip ready needs monitoring. However, individual chips may be out of synchronization by one clock. U78 solves this problem by delaying system GROM RDY for 2 additional clock cycles. This also overcomes the access delay problem described in the GROM Spec. (Ref. 3) by preventing a second I/O operation from occuring too soon (software no longer needs to build-in this delay).

The GROM select and control lines are pulled up to +5v to meet the GROM specification of Vih = Vcc - 0.7 volts min. As explained in the previous section on Bus Structure, the data bus voltage requirements are met by buffering thru the CMOS 74C245 bidirectional buffer. Buffer direction is controlled by DBIN, and five select signals

including -GROM SEL and -PASCAL SEL control the buffer enable. Direction should be stable on U84 and U85 before the slower, decoded select signals enable the buffers. This avoids any momentary bus contention. The additional TTL buffer U84 (74LS245) insures that the CMOS buffer is not overloaded by the rest of the system.

SOUND AND SPEECH

The Sound and Speech circuits are located on the Down Board Sheet 4 schematic. The Speech chip U66 (TMS0285) and associated dual, stacked ROM's U48 (TMS0350) are wired similarly to the 99/4 Speech peripheral. Speech Read (-SPEECH RD) and Speech Write (-SPEECH WR) are independently decoded by U47 (74LS138) as >9000 and >9400 respectively.

The Speech chip clock (U66, pin 6) may be derived thru the jumper option from a fixed 672KHz clock originating at the VDP chip, or from the chip's internal oscillator whose frequency is tuned by proper selection of external resistors R48, R49, R50. The latter option is to be used only if the fixed clock causes speech quality problems (resistors are selected per 99/4 Speech Peripheral test specifications). The ROMCLK output (pin 3) of the Speech chip is OSC (pin 6) divided by 4 and is used by the Speech ROM's (see Speech chip spec. Ref 4 and Speech ROM spec. Ref 5). The Speech ROM's contain a total of approximately 250 spoken words. Pre-encoded words can also be loaded into the Speech processor chip from the system data bus. Speech output is thru a small filter network into the Sound chip.

The Sound chip U67 (TMS9919 or SN76489AN) accepts sound input from the Speech chip thru its Audio In pin 9 and drives the external TV monitor sound via the SNDOUT (SouND OUT) signal. Sound can also originate within the Sound chip when frequency and attentuation parameters are loaded over the data bus (See Sound Chip spec. Ref. 6). -SOUND SEL decoded by U47 (74LS138) at >84XX provides chip select and -WE strobes data into the chip. The Sound chip clock is provided thru a jumper option which can supply the 3.58 MHz SGCCLK for the TMS9919 or the 447.44 KHz GRMCK for the newer TMS9919A (SN76494N). The 3.58 MHz clock is routed thru a section of coax soldiered to the Down PWB. Sound and Speech chip Ready signals are wire-or'd together to produce SP/SND RDY.

KEYBOARD

The keyboard along with the Auxiliary Connectors and Cassette Interface is interfaced to the system thru the TMS9901 controller chip U___ (UP BD SH.6). A summary of 9901 I/O utilization is as follows:

Base Address = 0000

Signal	Pin	Select Bit	Use (I)=Input (O)=Output	
INT1	17	1	-EXTINT External Interrupt	(I)
INT2	18	2	-VDPINT VDP Interrupt	(I)
INT3	N/C	3	Internal 9901 Timer Interrupt	---
INT4	8	4	Keyboard Interrupt or Scan Input	(I)
INT5	7	5	Func.Key,Cassette In,Orig/-Ans Scan	(I)
INT6	6	6	Auxiliary Port 1 Scan Input	(I)
P0	38	16	Keyboard Row/Modem Test Select LSB	(O)
P1	37	17	" "	(O)
P2	26	18	" " MSB	(O)
P3	22	19	Keyboard Column Select LSB	(O)
P4	21	20	" "	(O)
P5	20	21	" " MSB	(O)
P6	19	22	Keyboard Interrupt Clear/Scan En.	(O)
P7	23	23	Cassette Output	(O)
P8	27	24	Cassette Motor Control 1	(O)
P9	28	25	Cassette Motor Control 2	(O)
P10	29	26	Aux. 1 Joys.A GND/Output Enable	(O)
P11	30	27	Aux. 2 Input Gate	(O)
P12	31	28	Auxiliary Connector 1 Select LSB	(O)
P13	32	29	" "	(O)
P14	33	30	" " MSB	(O)
P15	34	31	-AUXSEL (Auxiliary Conn.2 Select)	(O)

As shown on the schematic, the keyboard consists of 55 keys in a Row/Column matrix, 2 Function keys, 4 Function rocker switches, and 1 LED indicator. All lines are RFI filtered with a T-filter composed of 2 ferrites (or 150 ohm resistors) and a capacitor-to-shield ground. The keyboard is a seperate assembly which connects to the UP Board thru two 12 pin connectors (J___). See Reference 7 for details of the keyboard. Pull-up resistor values are selected to supply (summed with TTL gate currents) 1 to 3.6 milliamps thru the key switches per the Keyboard Specification.

At power-up, the 55 R/C keys are enabled for Row and Column scan. Setting 9901 (Base Address >0000) P6 output to zero will cause U___ (74LS244) to pull all 7 rows to zero and release U___ (74LS74) flip-flop to clock to a "1" upon closure of any of the 55 keys. This will cause a "0" on the 9901 INT4 input. Consequently, INT4 can be used to interrupt the 9900 via the 9901 Interrupt Request lines. This input may also be polled for a zero input indication of any matrix key depression.

Upon receiving the INT4 interrupt (or polling a "0"), the software

should set 9901 P6 to a one. This will reset the flip-flop, thereby clearing the interrupt, and will release the Row lines for normal scan to determine which R/C was depressed.

Scanning of the R/C keys involves:

1. Setting U___ (74LS156) decoder outputs 2Y0 thru 1Y2 (MSB) to zero for each Row line. This is done by incrementing the three 9901 outputs P0-P2 (MSB) from 0 to 6.
2. For each Row line at "0", look at every column line via U___ (74LS251) data selector. This is done by incrementing the three 9901 outputs P3-P5 (MSB) from 0 to 7 while looking for a "0" on 9901 INT4 input.
3. When the R/C key is located, set 9901 P6 output to zero again in order to enable the U___ flip-flop interrupt and select INT4 for common key interrupt or poll.

Since every R/C key can be individually scanned, simultaneous depression of 2 or more keys can be detected by continuing the scan after the first key is located. Hence, N-key rollover protection can be implemented in the software.

The 2 Function Keys (Control and Shift) and the 4 Function rocker switches are scanned separately from the R/C keys. Each of the 6 Function signals is brought to a separate data selector U___ which is also addressed by 9901 P3-P5 outputs; however, the input is into 9901 INT5. The 9901 P3-P5 outputs should be incremented from 0 to 5 to select the Functions. A "0" into INT5 indicates that Function is active. Note that Originate/Answer rocker switch signal is sent to the Modem for independent, hardwired selection of mode, but its status can be monitored thru INT5.

The keyboard LED is independently controlled by the Modem circuit to indicate Carrier Detect. This signal is also fed to the Function decoder U___ input D7 for software monitoring thru INT5.

AUXILIARY CONNECTORS

Two D-type 9 pin connectors (J___, J___) are provided in the left side panel for auxiliary functions. J___ , nearest the console front, serves as Auxiliary Connector 1. This connector can interface to a 99/4 type of Y-cabled joystick pair, or can be used as a limited I/O port for other auxiliary purposes. As shown on UP BD SH. 7 schematic, Auxiliary Connector 1 interfaces to the TMS9901 chip (U___) thru 74LS05 open-collector gates and U___ (74LS251) 3-state data selector. TMS9901 P10 output drives pins 7 and 2 of Aux. Conn. 1 thru two 74LS05 gates to provide standard 99/4 Joystick select signals JSA (JSAGND) and JSB (JSBGND), which in fact, are pseudo-ground signals that are routed thru the joystick switches to the data selector, U___. Inputs to the data selector are selected by P12-P14 of the 9901 and multiplexed into the 9901 INT6 input as follows:

9901 Select P14/13/12(lsb)	Selector Data In	Aux. Conn. 1 Pin	Function 99/4 Joystick	Function Auxiliary I/O
000	D0	8	-DN (Down)	STBIN1 (Strobe In 1)
001	D1	N/C	---	---
010	D2	9	-RT (Right)	STBIN3 (Strobe In 3)
011	D3	5	-LT (Left)	STBIN4 (Strobe In 4)
100	D4	4	-UP (Up)	STBIN2 (Strobe In 2)
101	D5	3	-PB (PushButton)	INGATE (Input Gate)
110	D6	N/C	---	---
111	D7	N/C	---	OVRTP (Over Temp.)
---	--	7	JSAGND	OUTEN (Output Enable)
---	--	6	---	AUX5V (5volts/17MA)
---	--	2	JSBGND	-OUTEN
---	--	1	---	GND (Signal Ground)

STBIN1-STBIN4 are four inputs which may be monitored as general, polled inputs. INGATE is an input that allows an externally generated signal to gate or latch 8 bits of parallel information thru Auxiliary Connector 2 into U___ (74LS373); a wire-or connection to 9901 P11 output allows an internally generated signal to also perform this latch function. Further explaination is made in the Auxiliary Connector 2 discussion.

NOTE: 9901 P11 (Select Bit 27) must be set low to enable -PB or INGATE.

OUTEN and -OUTEN provide a +4.3 volt logic "1" or a -0.7 volt logic "0" (compensates for joystick switch voltage drop) as selected by 9901 P10. -OUTEN also turns on U___ (74LS373) to place 8 bits of outgoing information on Auxiliary Connector 2.

AUX5V (Auxiliary Connector 5 volts) supplies a filtered, current-limited, voltage which can be used to power an external LED or optoisolator. Current is limited to 17 milliamp maximum or 12 MA at 1.5 volts (typical optoisolator input voltage). The optoisolator can then be switched by OUTEN or a Aux. Conn. 2 output to provide a

totally isolated signal.

OVRTP (Over Temperature) is neither a joystick nor I/O function, but is tied to the console temperature warning sensor (UP BD SH. 10) and is monitored by U___ and 9901 INT6 for convenience. See earlier discussion on Thermal Protection.

Auxiliary Connector 2 is a general purpose, bidirectional, 8-bit, interface. Incoming data can be latched into U___ by pulling INGATE low as described above. This latched data can be read by setting 9901 P15 (Select Bit 31) output low to raise AUXSEL (Auxiliary Select), and then moving any byte from peripheral memory (>4000-5FFF) to some other location. As shown on the schematic (UP BD SH. 7), MBE is gated with AUXSEL and DBIN to turn on U___ (74LS373). Consequently, the setting of AUXSEL will cause the incoming 8 data bits to appear in all 8k bytes of peripheral memory. This provides a simple hardware interface, but means AUXSEL must be enabled only when looking at an incoming external byte, and then, should be immediately disabled. The 9901 powers-up with AUXSEL disabled.

NOTE: Keep 9901 P15 high (AUXSEL disabled) except to access Aux. Conn. 2.

Outgoing data thru Aux. Conn. 2 is latched into the other 74LS373 (U___). Data is written to this latch by moving a byte from memory to any peripheral memory location (>4000-5FFF) with AUXSEL enabled (9901 P15 low). MBE is gated with AUXSEL and -DBIN to form OUTGATE which latches the byte into U___. The latch's 3-state output must then be turned on by -OUTEN (9901 P10) pulled low. 9901 P10 powers-up as high.

NOTE: -OUTEN (9901 P10) must be high when external data is expected into Aux. Conn. 2 in order to avoid Input vs. Output bus conflict.

The bidirectional and latched nature of Auxiliary Connector 2 allows for "wrap around" type of diagnostic testing. Test software can be written to test all Aux. Conn. 2 hardware, except final filters and the connector itself, by latching output data into U___ and then reading the data back thru U___.

CASSETTE INTERFACE

The 9-pin cassette interface is unchanged from the original 99/4 design, except different TMS9901 bits are used and bidirectional relays replace the transistor motor controls. The interface configuration is as follows:

TMS9901 Signal	Select	Condition	CASSETTE Pin	Function
INT5	5	P5/P4/P3=110	8&9	MAG IN (Magnetic data In)
P7	23	Output	5&3	MAG OUT(Magnetic data Out)
P8	24	Output (low)	1&2	CAS CNTRL 1 (motor on)
P9	25	Output (low)	6&7	CAS CNTRL 2 (motor on)

As shown on UP BD SH. 6 schematic, the cassette input (MAG IN) is converted from analog to digital information by U___ (4558) op amp. The signal then passes thru U___ (74LS251) decoder where it can be selected by a 9901 P5/P4/P3 code of 110 for input into 9901 INT5 (Select Bit 5).

Output to cassette is direct from 9901 P7 (Select Bit 23) as shown on UP BD SH. 7. The digital signal is AC coupled and analoged thru the capacitor/resistor network before going out the connector.

Dual cassette motor on/off control is provided by U___ and U___ from 9901 P8 and P9 (Select Bits 24 and 25) outputs which, when taken low, will close the relays and turn on the cassette motors. The 9901 powers-up with P8 and P9 high and the relays open. These miniature electro-mechanical relays allow any cassette player to be used, no matter what its motor control polarity may be. The relays are driven by U___ driver. Coil voltage is +12 volts @ 30 MA. This avoids loading of the +5 volt bus. The Up board PWB is layed out to allow for either an Aromat HB1-DC12V relay or an equivalent Midtex 210 type relay. These relays are normally open, single pole, and are designed to handle the approximately 0.5 amp inductive load of the cassette motor. The PG1992 diodes across the relay coils minimize back EMF when the coil driver turns off. The series resistor/capacitor across the relay contact likewise reduces back EMF caused by the inductive load and protects the opening contact.

PERIPHERAL CONTROLLERS

Four peripheral controller circuits are mounted on the Up Board; these control the Printer, Disk(s), RS-232 ports, and Modem. An additional, but similar, controller can be mounted on the optional Mezzanine Board to control its functions. These controllers interface to the system in a manner identical to the way external peripherals interface to the 99/4. Hence, each controller has its own Device Service Routine ROM located on the 8-bit data bus in CPU address space >4000-5FFF and each controller is enabled by a specifit CRU address. CRU assignments for ROM enables are as follows:

CRU ADDR	CONTROLLER DSR ROM
1100	Disk
1300	RS-232
1800	Printer
1900	Mezzanine Board

As shown on UP BD SH. 3, the above enables are decoded by U___, U___(74LS138) and latched into U___ (74LS259) where the output, DISK ROM, RS232 ROM, or PRINTER ROM, is and'd with MBE to select the appropriate ROM. The Mezzanine Board uses similiar logic to enable its ROM.

NOTE: Only one DSR ROM should be selected at any one time to avoid data bus conflict.

As described in the Memory ROM section, the DSR ROM's are TMS4732 (or equivalent) 4K x 8 memories. TMS2532 EPROM's may also be used.

PRINTER

The Printer controller (UP BD SH. 1,2) utilizes DSG circuits and custom IC's to control the DSG printer mechanism, yet interfaces to the CPU in a manner similar to the 99/4 peripheral thermal printer. Dedicated CRU addresses are as follows:

CRU ADR	DEVICE OUTPUT	CONNECTOR PIN	FUNCTION
1800	U___-11	---	DSR ROM SELECT
1801	U___-5	---	HEAD STEP. MTR PHASE SELECT 2 (PHB)
1802	U___-6	---	" " " " " 1 (PHC)
1803	U___-7	---	" " " " ENABLE (STEP)
1804	U___-9	---	" " " GUICK DISCHRG. (FAST)
1805	U___-10	---	HEAD POSITION SENSOR ENABLE
1806	U___-11	LF3/HL2	STEP LF MTR/LIFT HEAD (HEADLIFT)
1807	U___-12	LF1/HL2	" " " / " " (LINEFEED)
18X0	U___-5	CRUIN	HEAD POSITION SENSOR (0=SENSE)
1810	U___-4	PH 17	PRINTHEAD COLUMN 5 (XD5)
1811	U___-5	PH 7	" " 4 (XD4)
1812	U___-6	PH 18	" " 3 (XD3)
1813	U___-7	PH 20	" " 2 (XD2)
1814	U___-9	PH 10	" " 1 (XD1)
1815	U___-10	---	STROBE-ON PRNTHD. DRIVERS (PHDSTRB)
1816	U___-11	---	START NEW PRNTHD. MATRIX (-STSEL)
1817	U___-12	---	TURN-ON PRINTHEAD (PRINT)

The printer mechanism consists of a 5 column by 7 row matrix printhead (Ref. 8) which is stepped across 80 columns of thermal paper by a 3 phase stepper motor. Another stepper motor (4 phase) controls paper linefeed while a solenoid raises the printhead. The mechanism is capable of 30 characters per second print speed.

The printhead is arranged as follows (viewed from heatsink side as it creates letter F on paper):

		COLUMN XD1	XD2	XD3	XD4	XD5
	YD7	X	X	X	X	X
	YD6	X				
	YD5	X				
ROW	YD4	X	X	X	X	
	YD3	X				
	YD2	X				
	YD1	X				

To print a character observe to following sequence:

1. Turn off "-STSEL" (SBZ >1816), then on (SBO >1816).
   --this clears U___(74LS164) and presets U___(74LS109)

to "1" to setup Row YD7 as first row.

2. Turn on "PRINT" (SBO >1817).
   --this starts U___(2543), DSG custom voltage regulator, to apply a ramped voltage (see below) to the printhead. This voltage starts at approx. 6vdc and rises to approx. 16vdc as controlled by a printhead temperature sensing diode feedback (DVOLTS) and the print Contrast Adjustment potentiometer. Thus, the voltage is designed to give a consistent thermal burn by compensating for increased element resistance as head temperature increases. PRINT signal is AC coupled a 1 microfarad capacitor to prevent a system failure from burning out the printhead (RC time constant is approx. 12 msec.).

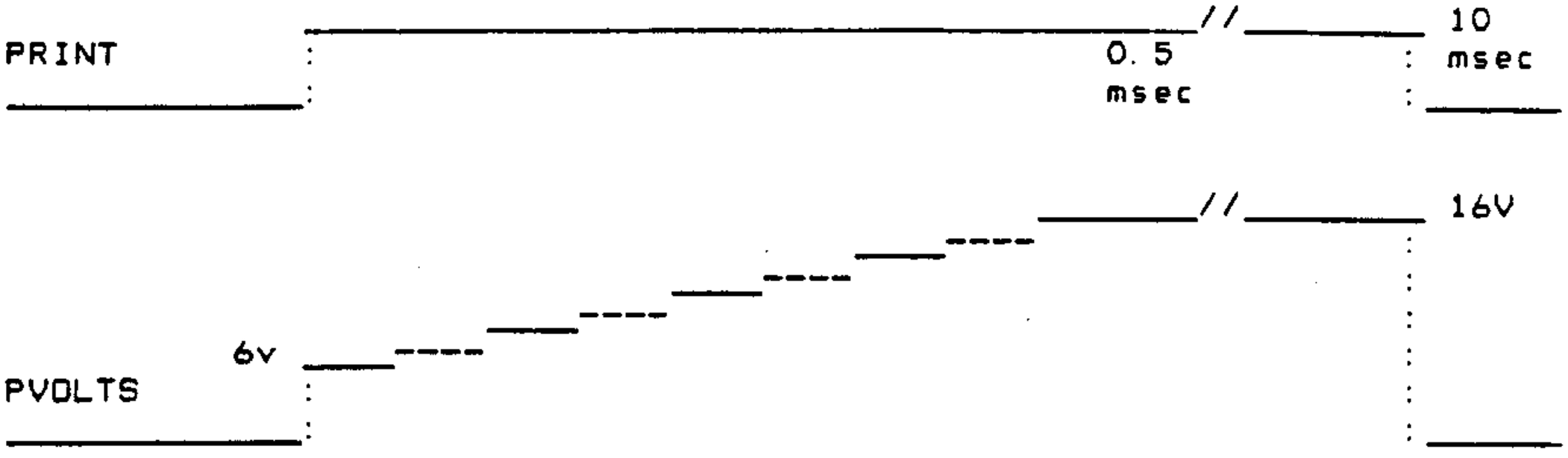
3. Load 5 columns of data for this row and turn on printhead drivers (U___, U___) with "PHD STRB" (PrintHeaD STRoBe).
   --since the 5 columns and PHD STRB are sequential CRU addresses (>1810-1815) this action can be done-with one LDCR instruction into U___(74LS259).

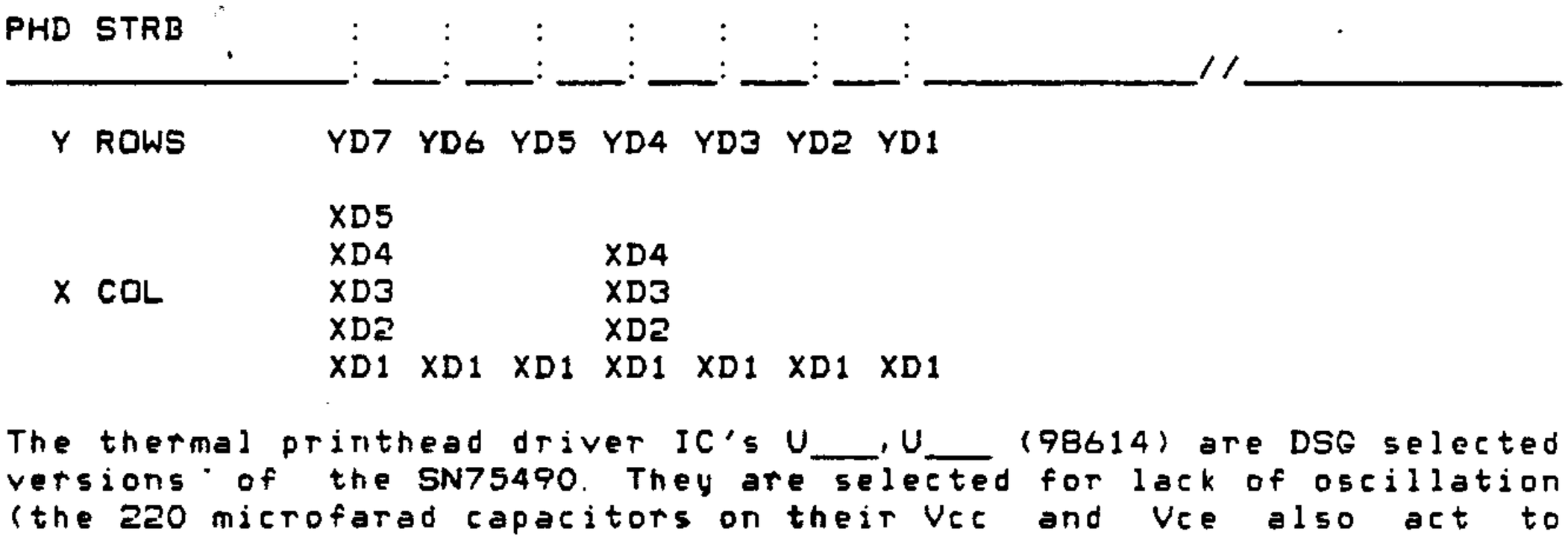
4. Turn off "PHD STRB" (SBZ >1815).
   --this toggles U___(74LS109) off and shifts U___(74LS164) to the next row YD6. The latching effect of the printhead SCR's will keep Row YD7 on as long as PRINT is on.

5. Continue as in Step 3 and 4 until all 7 rows of column data have been output.

6. After 10 milliseconds turn off "PRINT" (SBZ >1817).
   --this completes the burn of one character.

The timing sequence for burning the character F would be approximately as follows:





Y ROWS	YD7	YD6	YD5	YD4	YD3	YD2	YD1
X COL	XD5						
	XD4			XD4			
	XD3			XD3			
	XD2			XD2			
	XD1	XD1	XD1	XD1	XD1	XD1	XD1

The thermal printhead driver IC's U___,U___ (98614) are DSG selected versions of the SN75490. They are selected for lack of oscillation (the 220 microfarad capacitors on their Vcc and Vce also act to prevent output oscillation). The drivers switch printhead row and column addresses between -4.75 volts nominal (off) and +3.5 volts. Since row and column are AND'd together on the printhead to gate the printhead-mounted SCR's on, both voltages must be positive along with PVOLTS (SCR anode) to latch the particular 1 of 35 elements on. Likewise, both row and column must be negative voltage and PRINT off in order to turn any element off.

As mentioned above the custom switching voltage regulator IC U___ (2543 - see Ref. 9) acts to ramp up PVOLTS as controlled by DVOLTS temperature feedback and Contrast Adjustment. The reduced voltage (6.4-8.5 volts) at row/column loading also precludes inductive spikes on the printhead ground lead from causing erroneous turn on or turn off of other elements (see Ref. 8). SD1 (pin 9) of the 2543 is actually a pulse width modulated signal which switches Q___ , the +30v power transistor, on or off as dictated by DVOLTS (offset by Contrast) in order to approximate the PVOLT rms level required to properly heat the printhead resistor element. The PWM SD1 output is turned on by the 20.8 KHz PWCLK (PoWer CLocK) and gated off as necessary by an internal comparator which monitors PVOLTS thru pin 11 and compares it with DVOLTS (pin 1) as offset by Contrast (pin 16). The 1 microfarad capacitor on pin 10 integrates the pulsed PVOLTS for the comparator. The pin 14 capacitor is part of sample and hold circuit designed to smooth out momentary thermal spikes in

DVOLTS. SD2 (pin 7) keeps Q___ on throughout PRINT to provide a +6v holding voltage for the element SCR's; however, Q___ only conducts when the +30v Q___ is gated off. PWRGOOD (PoWeR GOOD) is gated internally with PRINT and must be active for the 2543 chip to function.

Mechanical motion of the printhead and paper is controlled by two stepper motors and a solenoid. Horizontal printhead movement occurs when the 3 phase Printhead Stepping Motor is activated by CRU inputs into U___(2444A), the DSG custom Motor Drive IC (UP BD SH. 2). This IC (see Ref. 10) is capable of driving a 4 phase motor with phase selection as follows:

INPUT		PHASE
PS1(pin 8) PSC (>1802)	PS2(pin 7) PSB (>1801)	
0	0	A (pin 4)
0	1	B (pin 5)
1	0	C (pin 1)
1	1	D (pin 6-not used)

Once the proper phase is selected for the 2444A, it is turned on by raising STEP (CRU adr >1803). The phase output control lines (pins 4, 5, 1) control the TIP126 power transistors (Q___, ___, ___) in a pulse width modulated fashion similar to the above mentioned 2543 IC (this minimizes voltage drop, therefore, heat dissipation in the transistors). The pulse is gated on by the 20.8 KHz PWCLK and gated off as necessary by the output of an internal comparitor which compares STEP (offset by Step Adjustment) and MOTOR RETURN. Pin 13 (MOTRET) provides a voltage across the 0.5 ohm resistor R___ which is proportional to current in the selected motor winding. Therefore, motor drive current is regulated between 1.3 and 1.85 amps when stepping. A detent current of .65 amps passes thru the selected winding when STEP is low. The external .22 microfarad capacitor to pin 10 is internally connected to the buffered STEP to slow its risetime and reduce mechanical motor noise.

Clamp Output (CO pin 16) is an open collector drive which follows FAST (pin 14, CRU adr >1804) and controls the motor inductive flyback voltage thru clamp diodes CR___, ___, ___ and transistor Q___ (TIP126). Flyback voltage is the negative voltage which occurs at the motor phase winding when the control transistor is gated off. The inductive motor winding tries to continue conducting current, thereby appearing as a battery until the current can decay. This effect is used to smooth out the pulse width modulated winding current by maintaining approx. -2v flyback voltage for slow decay...FAST off allows Q___ to be fully on with base current thru CR___(1N914B) and R___(6.8K) to -12v. When rapid decay is desired (phases switched), FAST is turned on to bring CO (pin 16) high which back biases CR___(1N914B) thru CR___(1N746A), thereby causing greatly reduced Q___ base current to flow thru CR___ (1N721A) and raising the Vce across Q___ and the resulting flyback voltage to

approximately -22 volts. The winding current is then rapidly discharged at a 0.75 amp per msec. rate.

The Linefeed (LF) Motor is a 4 phase 7.5 degree stepping motor which is wired to appear as a 2 phase 15 degree stepper (see Ref. 11). CRU bits >1806 (HEADLIFT) and >1807 (LINEFEED) control the stepper phases and the headlift solenoid (Note: the signal names are DSG convention but are misnomers in that both HEADLIFT and LINEFEED control the motor and solenoid). A linefeed sequence is as follows:

1. Turn on LINEFEED (>1807) for 6 milliseconds.
   --this signal is AC coupled thru C___(220 micFd. - for winding burnout protection) to Q___ (TIP121) which turns on and connects the black end of phase 1 thru Linefeed Conn. pin 1 to ground. The white end of phase 1 is AC connected thru pin 5 and C___(25 micFd.) to +30v. Phase 1 conducts first until C___ charges to 30 volts (approx. 3 msec.); then phase 2 (DC coupled red end to pin 1 and yellow end thru pin 4 and Headlift Solenoid to +30v) conducts until LINEFEED is lowered 3 milliseconds later. The head is automatically raised during the last 3 msec. and stays raised 3 additional milliseconds due to slow inductive current drain thru R___(20 ohm).

2. Immediately after turning off LINEFEED, turn on HEADLIFT (>1806) for 6 milliseconds.
   --this signal is AC coupled to Q___ which connects the red end of phase 3 thru Linefeed Connector pin 3 to ground. As with phase 1, phase 3 is AC coupled thru C___ to +30v and conducts for approximately 3 milliseconds before C___ charges and phase 4 begins conduction. Phase 4 keeps the Headlift Solenoid energized thru pin 4 and stays conducting until HEADLIFT is lowered.

3. Continue as in Step 1 and 2 until paper is advanced the desired amount.
   --NOTE: Headlift with linefeed is subject to a maximum duty cycle of 40 percent based on a maximum ON time of 30 seconds.

Headlift without linefeed is accomplished by setting both HEADLIFT and LINEFEED to "1". This turns on both Q___ and Q___ to pull current thru all linefeed motor windings thereby locking the motor in place while the headlift solenoid is energized. The RC time constant of C___ or C___ and adjacent resistors plus the 74LS259 internal pull-up provides approximately 200 msec. which means HEADLIFT and LINEFEED may require pulsing for long lifted-head operations (RC discharge time constant is approx. 100 msec.). Slew time for a full 80 columns is 195 msec. maximum when performed as detailed later.

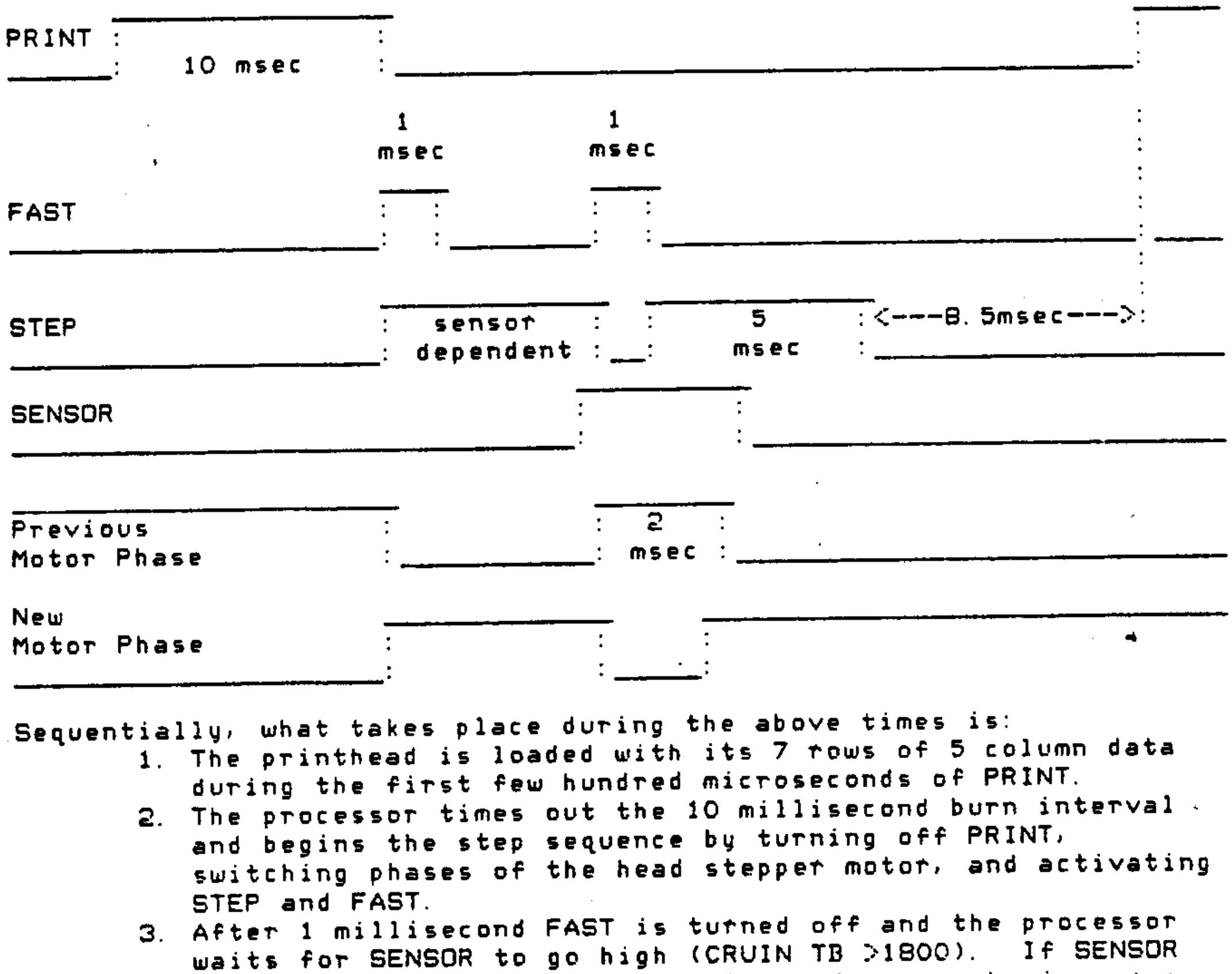
NOTE: Headlift without linefeed is subject to a maximum duty cycle of 20 percent based on a maximum ON time of 45 seconds.

Horizontal movement of the printhead can be broken into the

following functions:

1. Print and step printhead (1 character/0.1 inch).
2. Step printhead (space).
3. Step printhead backwards (backspace).
4. Slew printhead to a new position (including carriage return).

A Print and Step sequence appears as follows (the head is not lifted except when slewing more than one column):



Sequentially, what takes place during the above times is:

1. The printhead is loaded with its 7 rows of 5 column data during the first few hundred microseconds of PRINT.
2. The processor times out the 10 millisecond burn interval and begins the step sequence by turning off PRINT, switching phases of the head stepper motor, and activating STEP and FAST.
3. After 1 millisecond FAST is turned off and the processor waits for SENSOR to go high (CRUIN TB >1800). If SENSOR does not go high within 6 milliseconds, a mechanism error (mechanical jam or paper out) has occurred and no further printing should be attempted until the user intervenes (via software or system reset). Software should respond to SENSOR within 100 microseconds.
4. Upon SENSOR going high, the braking sequence begins by switching phases back to their previous state, turning off STEP, and turning on FAST for 1 millisecond.
5. FAST is turned off and STEP is turned on again for 1

additional millisecond at which time the phases are switched back to their next state, and STEP is held high for 4 more milliseconds.

6. STEP is turned off and an 8.5 millisecond settling time is provided before the next operation can begin.

NOTE: It may be necessary for software to fine tune the above sequence.

A single space of the printhead is the same as above, except PRINT is not activated and its 10 milliseconds is not included. Backspace is the same as space except that the new phase of the motor is reversed. Initial phase is established at power-up by performing a carriage return and rememering the last phase used to reach the left mechanical stop.

Slewing of the printhead has been determined by DSG to fall into one of four categories for optimum head speed control:

1. Acceleration when more than 20 columns away.
2. Constant speed control.
3. Deceleration when 12 columns from destination.
4. Operation when less than 20 columns away.

During any slew operation the head is lifted until it is one column from its destination. STEP is on throughout the entire slew operation to provide sufficient motor current for acceleration and deceleration. FAST is active for only 1 millisecond when the first 5 changes of motor phases occur during startup.

When slewing outside a 20 column region the motor is accelerated by changing the phase each time the sensor input (-SENSOR) goes high until SENSOR occurs faster than every 1.5 milliseconds--this indicates the mechanism is at constant speed (70 in./sec.). The motor phase should then be changed every 1.5 milliseconds until deceleration.

When the printhead reaches a position 12 columns from it's destination, deceleration commences and the motor phase is changed per times indicated in the following table rather than at 1.5 millisecond intervals:

DECELERATION TABLE

COLUMNS TO DESTINATION	MILLISECONDS BETWEEN PHASES
2	4.68
3	2.50
4	2.25
5	2.06
6	1.93
7	1.80
8	1.74
9	1.67
10	1.61
11	1.61

For head slew of 20 columns or less the head is accelerated until the appropriate time in the following table is reached between SENSOR inputs:

20 COLUMN OR LESS ACCELERATION TABLE

COLUMNS TO DESTINATION	MILLISECONDS BETWEEN PHASES
3	7.88
4	6.02
5	4.55
6	3.98
7	3.59
8	3.08
9	2.76
10	2.31
11	2.25
12	1.99
13	1.86
14	1.80
15	1.74
16	1.74
17	1.74
18	1.67
19	1.67
20	1.67

The above time is read once at the beginning of the slew and is used instead of the 1.5 milliseconds until a column is reached inside the 12th column of the Deceleration Table where the time is longer. This represents the point where the deceleration profile is intercepted and deceleration begins.

Miscellaneous circuits on the Printer Controller provide functions which interact with the previously discussed operations. The SENSOR flip-flop U___(74LS109) serves as a leading edge detector for the

amplified sensor signal which comes from U___(2613). The flip-flop must be cleared between SENSOR detections by resetting SENSOR ENABLE (CRU >1805) to "0", then setting it to "1" for the next input. The sensor itself is a 24-position slotted wheel (1 slot per 15 degrees or 1 character position) which is mounted to the printhead stepper motor shaft and which interrupts the light path of an opto-interrupter module. The midpoint of the interrupted light position (SENSOR low) is set at time of printer mechanism manufacture to correspond to the stepper detent or character (column) position an follows:

The Power Good IC (U___) on UP BD SH.2 is a Digital Systems Group custom chip designated the 2613 (see Ref. 12). This 16 pin IC combines several functions of the original 745 terminal logic, only some of which are used in the 99/7. Functions not used are the bell driver, the AC power shutdown, and the paper out sensor amplifier. The power good function is used to provide a TTL indication (POWER GOOD-pin 10) that Vcc (+5v) is above a set threshold after a fixed delay from power-up. The threshold is fixed by R___(2K), R___(6.2K), and an internal zener to be 4 volts. The delay is determined by the R___/C___(4.7 micFd.) time constant to be 10 milliseconds. PWRGOOD, when low, inhibits all printhead operation and STEP or FAST motor control. The other IC function used is an internal amplifier which provides a TTL logic "1" out pin 11 (SENSOR) when light is detected by the opto-interrupter module. Note: this signal is inverted by U___(74LS109) to provide a logic "0" for CRUIN of >1800 when light is detected.

DISK CONTROLLER

The Disk Controller controls up to three 5 1/4 inch minifloppy disk drives. Each disk contains either 35 or 40 tracks of 9 sectors each. A sector is a block of data 256 bytes long, and is the unit of data read from or written to the disk at one time.

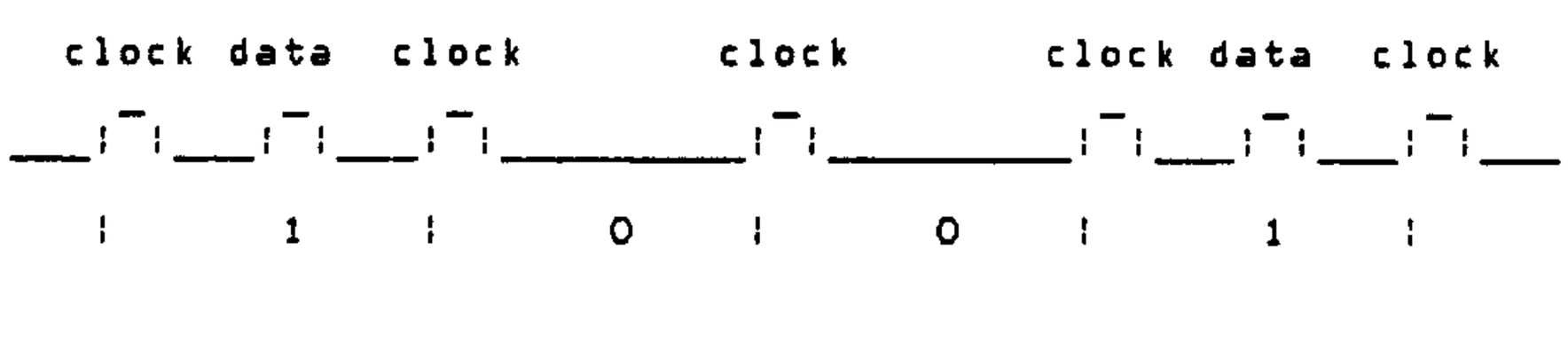
The position of the tracks are defined by the disk drive. All drives used with this disk controller define the tracks at the same place. Track 00 is the outermost track (furtherst from the center) and track 39 is the innermost track.

Soft sectoring is used in this design. This means that the position of the sectors on a track are not physically defined by the drive or the diskette, but are determined by the format of the data on the track. This allows the same disk drive and diskettes to be used for different size sectors and different numbers of sectors per track. It is up to the controller to figure out from the data how large the

sectors are and where they are located on the disk. The sectors may be in any order on the diskette and need not have any relation to the physical index hole. This controller does use the physical index hole as the start and end of the track when formatting, but a formatted disk to be read or written on this unit need not follow that convention.

The disk drive contains circuitry to control the motor speed, move the head, and drive the read/write head. The drive also supplies indication signals such as index pulse detection, track 00 indication, and diskette write protect indication. No intelligence is contained in the drive itself.

Data is recorded on the disk using an FM encoding scheme (single density). This is a highly reliable self clocking code which is resistant to speed variations and phase shifts. Each bit cell contains a clock pulse and an optional data pulse. The data pulse is absent if the bit is a 0 and present if the bit is a 1 as shown in the following diagram:



There are special bytes called Address Marks which do not follow the standard FM encoding scheme. These bytes have 3 clock pulses missing in the middle of the byte. Address Marks are found at the beginning of ID fields and data fields. They serve two purposes: to indicate to the controller that an ID field or data field has been encountered, and to get the controller in byte sync (indicate the end of one byte and the beginning of the next byte). The data and clock bits of the Address Marks have been carefully chosen so that these bytes cannot appear in unwanted places by accident as a result of writing data.

Disk format is shown in the following figure. This format is written at disk initialization time. When a sector is updated, only the section between the words "WRITE GATE ON" and "WRITE GATE OFF" is written. The format starts off with a 16 byte index gap. This is followed by the first sector. Every sector contains an ID field and a DATA field. The ID field starts off with 6 bytes of zeros to sync the data separator to the bit level. Zeros contain only clock pulses, so an unsynced data separator connot confuse clock and data pulses. The sync bytes are followed by an ID ADDRESS MARK which indicates to the controller that this is the start of the ID field. The ID field contains sector information such as the track address, sector address and sector length. It is terminated with two CRC bytes for error checking.

The ID field is followed by 11 bytes of gap to separate the ID field

(which is written during initialization only) from the DATA field (which is rewritten every time the sector is updated). This gap may vary slightly in length when the sector is rewritten due to motor speed variations.

The data field starts with 6 sync bytes and a DATA ADDRESS MARK which serve the same purposes as for the ID field. The 256 bytes of user data follow, and this is followed by two bytes of CRC for error detection. One byte of FF finishes the DATA field. This byte isolates the write gate turn off transients from the useful data.

The DATA field is separated from the next ID field by 44 bytes of gap. This gap will vary in length by as much as 6 bytes due to to allowable motor speed differences between the drive used the initialize the disk and the drive where the DATA field is rewritten. The main purpose of this gap, however, is to protect the next ID field from the erase head while writing the previous DATA field. The erase mechanism remains on for some time after the DATA field is written. This erasure is intended for the area between tracks only, however, repeated erasure will weaken the track data.

The DATA gap is followed by the sync bytes of the next ID field. After the last sector, 103 bytes of additional gap is written. This gap may vary in length by 32 bytes from nominal due to allowable motor speed variances when the disk is initialized.

DISK FORMAT
9 SECTOR 5 1/4" SOFT SECTOR

	DESCRIPTION	# OF BYTES	VALUE	
	INDEX GAP (G1)	16	00	
	SYNC BYTES	6	00	
	ID ADDRESS MARK	1	FE	(CK=C7)
	TRACK ADDRESS	1	TRACK # (0 TO 39)	
E	ZEROS	1	00	
A	SECTOR ADDRESS	1	SECTOR # (0 TO 9)	
C	SECTOR LENGTH	1	01	
H	CRC	2	CRC VALUE	
S	G2	11	FF	
E	WRITE GATE ON			
C	SYNC	6	00	
T	DATA AM	1	FB (CK=C7)	
O	DATA	256	USER DATA	
R	CRC	2	CRC VALUE	
	WG OFF	1	FF	
	WRITE GATE OFF			
	G3	44	FF	
	G4	103	FF	
	TOTAL	3125		

The design of the controller revolves around the Western Digital FD1771 floppy disk controller chip (U___). The FD1771 receives commands from the CPU such as Seek, Read Sector, Write Sector, and Write Track. The FD1771 controls the movement of the disk head, searches a track for the correct sector, and converts parallel data from the processor to serial data for the disk drive and vise versa. CRC characters are generated and checked by the FD1771 also. The following is a description of a read or write command performed by the FD1771. Assume that the head is already on the proper track, and the track and sector registers are loaded with the desired values.

When a read or write command is issued, the FD1771 begins looking for an ID ADDRESS MARK. This is a unique pattern of data and clock bits and cannot show up in a data area by accident. When the ID ADDRESS MARK is encountered, the track address and sector address are read from the ID field and compared to the track and sector registers in the FD1771. If either the track address or the sector address is incorrect, the FD1771 skips this ID field and looks for the next ID ADDRESS MARK. If both the track and sector addresses are correct, the CRC bytes are read to detect any read errors in the ID field. If the CRC in incorrect, the FD1771 skips this ID field and

looks for the next ID ADDRESS MARK. The FD1771 will continue to look for an ID field with a correct track address, sector address, and CRC for 3 revolutions of the disk, and then give up and issue an error. The FD1771 will make no attempt to move the head to the proper track if the track address of the ID field does not match the track register. This operation must be performed by the CPU by issuing a SEEK command.

When the proper ID field is encountered and it's CRC is determined to be correct, the actual read or write process begins. In the case of a read, the FD1771 looks for the DATA ADDRESS MARK. It must occur within an area of 12 to 28 bytes after the end of the last CRC byte or an error will be issued. After finding the DATA ADDRESS MARK, the data field is read (256 bytes in this case). The data is passed on to the CPU a byte at a time as explained later.

The FD1771 is double buffered, which means that one byte is stored in the data register while the next byte is being accumulated in the shift register. When a byte becomes available, the CPU has one byte time to read it (64 microseconds in this case). If the CPU does not read it within that time, the next byte will finish being shifted in and overwrite the previous byte. If this occurs, an error flag is set.

After the last data byte is received, the two CRC bytes are read and compared to the CRC which was calculated as each byte was input. If a CRC error is detected, an error flag is set. The command then terminates and the FD1771 informs the processor that it is finished.

In the case of a write, the FD1771 waits 11 byte times, then begins writing. Six sync bytes are written to allow the data seperator circuits to get in sync before writing the ADDRESS MARK. The DATA ADDRESS MARK is then written followed by the 256 bytes of data. The data is received from the CPU a byte at a time using the same double buffered scheme as for a read. The data bytes are followed by two CRC bytes which are calculated as the data bytes are written. One byte of FF is written after the CRC bytes before the write is terminated.

CRU addresses utilized by the disk controller are as follows:

CRU ADR	DEVICE OUTPUT	DISK CONN. PIN	FUNCTION	SIGNAL
1100	U___-7	--	DSR ROM SELECT	(DISK ROM)
1102	U___-5	16	TURNS DRIVE MOTOR(s) ON	(MOTOR ON)
1104	U___-6	--	WAIT STATE ENABLE BIT	(WAITEN)
1106	U___-7	--	HEAD LOAD TIMING (not used, set to 1)	(HLT)
1108	U___-9	10	SELECTS DRIVE NO. 1	(DS1)
110A	U___-10	12	SELECTS DRIVE NO. 2	(DS2)
110C	U___-11	14	SELECTS DRIVE NO. 3	(DS3)
110E	U___-12	32	SELECTS BOTTOM HEAD	(BOTTOM HEAD)
11XX	U___-	CRUIN	HEAD LOAD STATUS (not used)	(HLD)

>1100 is accessed by the console to activate the peripheral DSR. A low to high transition on >1102 turns on the motors in all disk drives. The hardware turns off the motors 5 seconds after the most recent low to high transition when one-shot U___ times out. >1104 enables wait state logic used with the 1771. This bit is only set during data block moves between the CPU and the FD1771 for syncronization purposes. >1106 controls the HEAD LOAD TIMING input of the FD1771. Since the head load logic of the FD1771 is no longer used in this degign, this output is set to a 1 during any disk operations. >1108,A,C select which drive is currently being accessed. Only one should be set at any time. >110E ,when set to "1", will select the bottom head of a double-head drive mechanism Single-head drives are properly selected with the default (power-up) value of "0" on this bit.

Only one CRU input bit may be read in this design. It is not uniquely decoded and will show up at any CRU address within the peripheral CRU address space. In the interest of future expandablity, however, it should only be accessed at address 1100. The bit is used to read the status of the head load output of the FD1771. Since this function of the FD1771 is no longer used in this design, this bit is not accessed, but is available for future needs.

The memory mapped sections of the disk controller fall within the peripheral address space (4000-5FFF) which is defined by the MBE signal on the bus. All accesses to this address space will be ignored unless the DSR bit (CRU address 1100) is set to a one. The address space is split up into two sections, one for the DSR ROMs and one for the FD1771. The memory blocks are split up as follows:

MEMORY SPACE	DESCRIPTION
4000-4FFF	LOWER DSR ROM
5000-5EFF	UPPER DSR ROM
5FF0-5FFF	FD1771 (FURTHER DEFINED BELOW)

FD1771 ADDRESS MAPPING

5FF0	READ STATUS
5FF2	READ TRACK REGISTER
5FF4	READ SECTOR REGISTER
5FF6	READ DATA REGISTER
5FF8	WRITE COMMAND
5FFA	WRITE TRACK REGISTER
5FFC	WRITE SECTOR REGISTER
5FFE	WRITE DATA REGISTER

The FD1771 read and write address spaces are fully decoded on UP BD SH.3 as FDSEL (Floppy Disk SELect) and RESEL (REad SELect). Note: additional decoding on the 99/7 has freed up 5E00-5EFF for use by the DSR ROM.

Several circuits are needed to make the timing of the CPU meet the requirements of the FD1771. U___A (UP BD SH.4) is used to delay the Read Enable pulse until the chip select and address inputs have time to set up. U___(74LS74) is used to cut off the end of the Write Enable pulse to meet the data hold times of the FD1771.

The WAIT signal from U___B is used to syncronize the CPU to the FD1771 during data block transfers. This logic can be enabled and disabled by the CPU. When the logic is disabled, no wait states are generated. When the logic is enabled, the processor enters continious wait states (due to PER RDY low) whenever the FD1771 is accessed. The wait state condition is terminated when the clear input of flip-flop U___B is active. This may be triggered by one of four ways: a hardware RESET from the 99/7, interrupt request (RQINT) from the FD1771 going active, data request (DRQ) from the FD1771 going active, or MOTOR ON going inactive. Under normal conditions DRQ terminates the wait condition indicating that data is availiable (on a Read) or data is requested (on a Write). If a sector cannot be located by the FD1771, RQINT becomes active, terminating the wait states. MOTOR ON must be be used to terminate the wait states only if there is no diskette in the drive, or the drive being accessed is not present. If this happens, there are no index pulses sent to the FD1771, so it never quits trying to locate the sector.

The controller is interfaced to the disk drive via a 34 pin ribblon cable. Pin definitions are as follows:

DISK DRIVE SIGNALS

PIN	SIGNAL NAME	DIRECTION	FUNCTION
8	INDEX PULSE	C < D	LOW FOR PHYSICAL INDEX FROM SELECTED DRIVE
10	DRIVE SELECT 1	C > D	LOW TO SELECT DRIVE 1
12	DRIVE SELECT 2	C > D	LOW TO SELECT DRIVE 2
14	DRIVE SELECT 3	C > D	LOW TO SELECT DRIVE 3
16	MOTOR ON	C > D	LOW TURNS ALL MOTORS ON
18	DIRECTION	C > D	LOW SENDS HEAD OUT TO EDGE HIGH SENDS HEAD IN
20	STEP	C > D	NEGATIVE PULSE STEPS HEAD OF SELECTED DRIVE
22	WRITE DATA	C > D	DATA TO SELECTED DRIVE
24	WRITE GATE	C > D	LOW SELECTS WRITING TO SELECTED DISK
26	TRACK 00	C < D	LOW INDICATES SELECTED DRIVE IS ON TRACK 00
28	WRITE PROTECT	C < D	LOW INDICATES DISK IN SELECTED DRIVE IS WRITE PROTECTED
30	READ DATA	C < D	DATA FROM SELECTED DRIVE

All signals are active low. All signals from the controller to the drive are driven with 7438 buffers and all signals from the drive to the controller are terminated with 150 ohm resistors and received with 74LS14 schmitt trigger inverters.

All the signals except the three drive selects, BOTTOM HEAD, MOTOR ON, and READ DATA are handled directly by the FD1771. The FD1771 has the option to handle the READ DATA signal directly by using it's internal data separator, but greater reliability is achieved by using an external data separator (described below) and supplying the FD1771 with separated clock and data signals.

The FD771 is set up to interface to one disk drive. Selecting which disk drive is being accessed and remembering which track each drive is on must be performed by the CPU. The CPU must turn on only one drive select output port at any one time. The drive select output ports are AND'd with the MOTOR ON signal so that the drive will not be selected when the disk system is idle. This saves head and media life since the drive select signal also loads the head on a minifloppy. The MOTOR ON signal was used instead of the HEAD LOAD output of the FD1771 because it was determined that the FD1771 lifts the head too soon after the completion of a command (2 index hole times).

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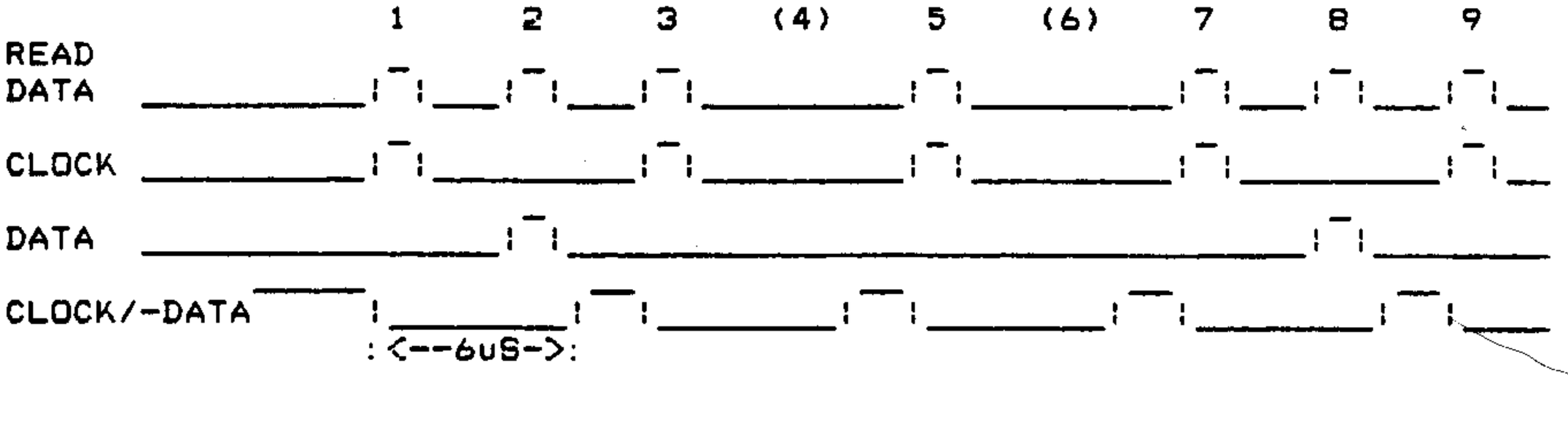
The function of the data separator is to separate the Clock and Data pulses in the FM encoded data stream from the disk drive. The data first passes through a 74LS14 inverter used as a line receiver, then goes into U___A (74LS123) to reduce the pulse width to 500 nS. The data then goes into a double R/S latch formed by all four gates of U___(74LS00). The only other input to this latch circuitry is a CLOCK/-DATA signal from U___B which decides whether the incoming pulse is a DATA or a CLOCK pulse. The outputs of the R/S circuit are the actual DATA and CLOCK pulses. Basically, on the leading edge of an incoming READ DATA pulse, the CLOCK/-DATA signal is sampled. If it is low, the pulse is sent to the DATA output. If it is high, the pulse is sent to the CLOCK output. A latching circuit is used so that there will not be both a CLOCK and DATA pulse generated if the CLOCK/-DATA signal changes state during the clock pulse (as it quite often does).

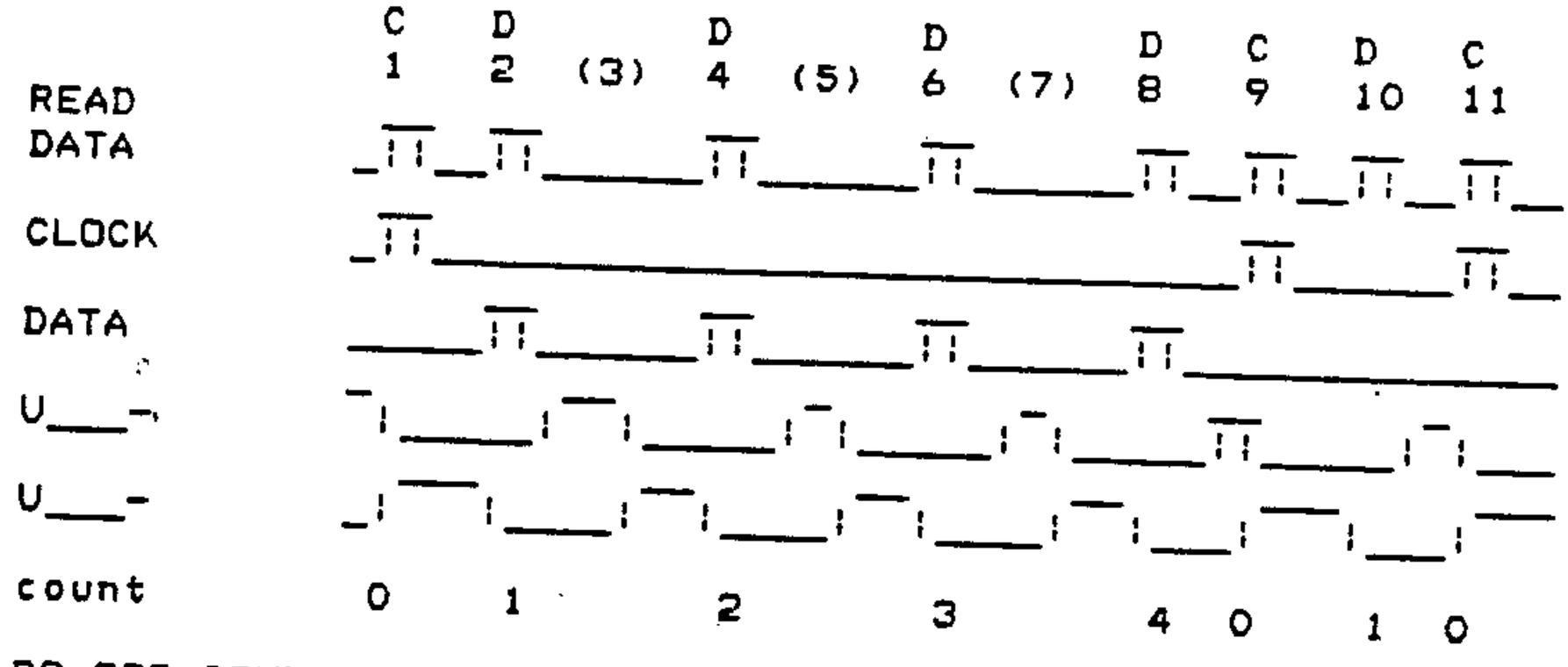
The CLOCK/-DATA signal is generated by a 74LS123 one-shot (U___A). The one-shot is triggered upon receipt of: the leading edge of a CLOCK pulse, or U___ B timing out. U___A has a timeout of 6uS which means that any incoming pulse received within 6uS of U___A being triggered will be interpreted as a DATA pulse, and any incoming pulse received after that will be interpreted as a CLOCK pulse.

The following timing diagram illustrates how DATA and CLOCK are separated. The data separator is assumed to be in sync in this example. Pulse 1 is a CLOCK pulse, and causes CLOCK/-DATA to go low for 6uS. Pulse 2 is within the 6uS window, and becomes a DATA pulse. Pulse 3 is at 8uS, after the one-shot has timed out, so it becomes a CLOCK pulse and retriggers the one-shot. There is no pulse at position 4, which would have been another DATA pulse. A missing DATA pulse means that the data bit is a zero. Pulse 5 comes after the 6uS time-out, so it is another clock pulse.



The circuitry described so far would be sufficient for a data separator if ADDRESS MARKS were not used. The missing CLOCK pulses in the ADDRESS MARKS will throw the data separator out of sync. U___A (74LS123) U___, U___(74LS74) keep the data separator in sync for up to 3 missing clock pulses. U___A is triggered by the leading edge of a data pulse. If no CLOCK pulse has been detected within 5.4

uS of the DATA pulse, a CLOCK pulse is faked by U___. This fake CLOCK pulse is NOT sent to the FD1771, but is used only to trigge U___A. U___, U___ count the number of consecutive DATA pulses whic are received without receiving any CLOCK pulses. If this numbe reaches 4 (which indicates 3 missing CLOCK pulses) the data separator is resynced so that the next pulse received will become a CLOCK pulse regardless of it's timing (see below).



RS-232 CONTROLLER

The RS-232 controller circuit is contained on UP BD SH. 5 schematic with its CRU enabling logic on UP BD SH. 3. CRU addresses used by the RS-232 are as follows:

CRU ADR	DEVICE OUTPUT	FUNCTION	SIGNAL
1300	U___-10	DSR ROM ENABLE	(RS232 ROM)
134/5X	U___-5	TMS 9902 ENABLE FOR PORT 1/MODEM	(-CE9902A)
138/9X	U___-6	TMS 9902 ENABLE FOR PORT 2	(-CE9902B)

Two TMS 9902 Asynchronous Communications Controller IC's perform the bulk of the RS-232 transmit/receive functions. Details of these chips are contained in Reference 13. These 18 pin chips are specifically designed to interface to the CRU bus; therefore 5 pins of the chip monitor CPU address lines A10-A14 to further decode upto 32 additional CRU bits. Consequently the TMS 9902 for Port 1/Modem control utilizes CRU addresses >1340->135F and the Port 2 TMS 9902 uses >1380->139F. TMS 9902 internal assignments for these bits are contained in Ref. 13. The interrupt outputs (-INT pin 1) of both 9902's are OR'd thru the 74LS00 gate to drive system -EXTINT (EXTernal INTerrupt) via and open-collector driver. Either 9902 can interrupt the CPU (level 1 interrupt) via the 9901 IC. As described in Ref. 13, the 9902 activates its interrupt for internal transmit buffer empty, receive buffer full, external device (or Modem) ready, and internal timer timed-out. Software must poll both 9902 chips, as

well as system Over Temperature Warning (previously described) and the mezzanine board (if used), to determine which device generated the External Interrupt.

As shown on UP BD SH. 5, only one 25 pin RS-232 type of connector is located in the 99/7. Pins have been selected in the connector so that Port 1 conforms to the EIA defined connector pinout. Therefore, a user who needs only one RS-232 interface can plug directly into the connector (assuming his external cable also conforms to the EIA standard). If the user desires two RS-232 ports, or wants to use the internal Modem plus a RS-232 port, he must use a Y-configured cable as shown on the schematic. The Y-cable allows both Port 1 and Port 2 to be used. Port 2 is internally connected to the EIA-defined secondary pins of the 25 pin connector. The Y-cable then translates Port 2 to the primary pinout standard.

The RS-232 line drivers are designed around the quad TL084 operational amplifier (U___) and will meet the EIA defined +/-12 volt swing at 9600 baud. The line receivers are utilize the SN75189 (U___) line receiver package and also meet EIA standards at 9600 baud.

As shown on UP BD SH. 5, the Modem circuit (described later) can be switched with S___(Modem Select Switch) to operate thru the Port 1 TMS 9902. S___ is accessable to the user thru the right hand console side panel. When switched to Modem, S___ disables the Port 1 RS-232 drivers and receivers with MODSEL (MODem SELect) and enables the MC6860 modem IC thru its -DTR pin 20. The Modem, therefore, appears identical to the external 99/4 modem as far as the software is concerned.

MODEM

The MODEM circuit consists of a modem IC (U___), filter IC (U___), and the acoustic muff couplers as shown on UP BD SH. 5. The MODEM interfaces to the CPU thru RS-232 port 1 TMS 9902 controller IC when the Modem Select Switch S___ is open. The Port 1 RS-232 drivers are gated off. Software has no knowledge that the MODEM has been selected, and MODEM communication appears as 300 Baud RS-232 Port 1 operation (see above RS-232 discussion).

The acoustic coupler in the 99/7 terminal provides the interface between the terminal and another time sharing computer or the another 99/7 terminal through a standard commercial telephone line. It can send and receive messages and data, transfer programs between 99/7's, and access information from a consumer data service center. By using a known FSK (Frequency Shift Keyed) technique, the device is designed to be compatible to the Bell 103 type modem. It will transfer data at the rate of 300 Baud, full duplex, either in originate or answer mode (as selected by the Orig/Ans keyboard rocker switch - UP BD SH. 6).

The modulator-demodulator is in a MC6860 NMOS chip (U___). Serial data from the TMS9902 is converted to FSK data by the modulator. The

output signal of this chip is a digitally synthesized sine wave. The output is coupled to the speaker muff via the filter IC U___. When in originate mode a Mark (logic one) from 9902 produces a 1270 Hz tone and a Space (logic zero) produces a 1070 Hz tone. When in answer mode a Mark is represented by a 2225 Hz tone and a Space is represented by a 2025 Hz tone.

The demodulator section of the MC6860 takes the received FSK square wave from the filter and converts it to serial Mark/Space data for the 9902. In originate mode a 2225 Hz tone is converted to a logic one and a 2025 Hz tone is converted to a logic zero. In answer mode, the receiving signals 1270 Hz and 1070 Hz represent Mark and Space , respectively.

The frequencies of modulator and demodulator are controlled by the user accessible Originate/Answer switch. When the switch is on Originate, it forces MC6860 pin 21 to a logic low and pin 19 to a logic high. This selects the proper modulator and demodulator frequencies for the originate mode. The following table shows the proper frequencies for Mark and Space:

Mode	Transmit Frequencies		Receive Frequencies	
	Space	Mark	Space	Mark
Originate	1070	1270	2025	2225
Answer	2025	2225	1070	1270

The microphone is tied to an external 68 pf capacitor and a 220 Kohm resistor in parallel to ground, to filter out high frequency noise associated with the acoustic coupler. The incoming analog signal is fed into pin 6 of U___(CH1230 filter). Internal to U___ the output of a microphone amplifier with a fixed voltage gain of 14 db is fed into a three stage bandpass filter. The center frequency of the bandpass filter is chosen by the mode switch (originate or answer). A logic "1" input, representing originate mode, on pin 1 of CH1230 will select 2125 Hz as the center frequency of the bandpass filter. A logic "0" input, representing answer mode, forces the center frequency to be 1170 Hz. The -3 db bandwidth of the bandpass filter is about 300 Hz. The other significant characteristics of the bandpass filter is a 50 db, or more, adjacent channel rejection and a 20 db voltage gain for the pass band.

The output of the bandpass filter is sent to a soft limiter and a carrier buffer circuit for an accurate limiting. Both of these circuits are located inside of the CH1230. The FSK square wave output of CH1230 at pin 14 is fed to MC6860 pin 17 for demodulation processing.

The threshold detection circuit is designed to toggle from +5 volts to 0 volts at a level of -66 db. A logic zero input to MC6860 pin 7

indicates the presence of the receive carrier; therefore, the clear to send output of MC6860 pin 23 will go to a logic "0" (-CD) and cause the Carrier Detect keyboard LED to be turned on with -CARDET. A loss of -CD signal results from a loss of threshold for 51 msec. or longer. The transmit carrier of the originate modem is then clamped off and a constant Mark is transmitted from the answer modem.

One of the problems in designing a modem, especially with an acoustic coupler, is the interference caused by the second harmonic of the transmit signal when the modem is in the originate mode. In this mode, the transmit signal is in the low band and its second harmonic falls in or near the pass band of the receiving signal band; therefore, a proper transmit level is required to minimize this interference. This is accomplished by using U___(75450) and R___(22Kohm) to drop the Transmit Carrier signal level when U___(MC6860) is in Originate mode. Since the second harmonic interference of an Answer mode modem does not cause any problem, the output transmit level can be greater.

The 99/7 modem is capable of being programmed in a self test mode. When MC6860 pin 16 is held low, the demodulator frequency is switched to the modulator frequency and demodulates the transmitted FSK signal. Channel establishment, which occured during the initial handshake, is not lost during self test; thereby permitting the receive filters to pass the local transmit carrier. To use this feature, -MODTST must be set to logic "0" by setting TMS 9901 (UP BD SH. 6) outputs P0, P1, P2 to 111 and the transmit muff must be coupled to the receive muff by placing a disconneted (avoids phone system interference) telephone handset across the muffs.

POWER SUPPLY

The 99/7 POWER SUPPLY converts AC input power to the regulated DC output power required to drive all circuits within the console. The power supply is designed to operate without degrading performance over the full range of steady-state and transient conditions. Output specifications are as follows:

	+5v	-5v	+12v	-12v	+30v	
Nom. Current.....	2.5	0.1	0.8	0.1	1.0	amp
Peak Current.....	3.0	0.2	1.0	0.3	3.0	amp
Ripple						
-at Pwr. Sup. Outputs..						+/-Mv
-after Up Bd. filter..	50	50	50	50	50	+/-Mv
Regulation						
-load.....	3	1	1	1	1	+/-%
with load variation.	2-3	.05-.2	.5-1.0	.03-.3	*	amp
-line (90-130VAC).....	1	1	1	1	1	+/-%

* +30v reg. measured with +5v varying +/-20%

As shown in the Power Supply schematic the supply is a multiple output, self-oscillating converter regulator. A single ferrite core transformer T1 provides drive to the power switch transistor Q5, multiple output voltages, input-output isolation, and output voltage regulation. The power supply operates in the flyback mode; that is, energy stored in the transformer is delivered to the loads during the off time of the power transistor. Thus, the high efficient power supply is achievable. The required Q5 base drive power at the optimum impedance level is provided directly from the transformer.

In operation input AC power, after passing through a RFI filter is rectified by diode bridge D12, D13, D14 and D15. The rectified DC current then passes through thermistors RT1 and RT2 (which reduce initial line voltage input for soft-starting) and resistors R19, R20 before storage across filter capacitor C9, from which the input or primary side dc current is supplied.

The power supply circuit is self-oscillating; the positive feedback path passes from the power transformer primary (terminals 4 and 3) to the base drive winding (terminals 6 and 5). The base drive signal is coupled through C5 and D9, then through current setting resistor R17 to the base of power transistor Q5. Oscillation begins when the primary side DC appears. A current set by R16 and R17 at the base drive of power transistor Q5 will cause Q5 to be biased on. The collector current of Q5 begins to rise linearly due to the inductive load at the collector of Q5. The base current established through R17 ensures that Q5 will saturate. When the voltage drop across R18 produced by the emitter current of Q5 has risen to approximately 1.2 volts, Q4 begins to conduct, shunting base drive from the base of Q5 which causes it to lose saturation. As soon as its collector voltage begins to rise, Q5 is rapidly switched off by regenerative feedback. Falling collector current causes rising collector voltage, resulting in falling base drive voltage and falling base current. The collector voltage of Q5 flies back above the input DC supply voltage

until the rectifiers in the transformer secondary circuits become forward biased, and currents flow into the output filter capacitors and output load resistances. Oscillation varies between 30KHz and 50KHz depending on line voltage and load (lower line voltage or less load causes lower frequency).

The energy stored in the magnetic field of the transformer during the on-time of Q5 is transferred to the output during the off-time of Q5. Secondary currents continue to decrease linearly with time until the transformer flux has fallen essentially to zero. The transformer terminal voltages remain at their flyback values during the entire period of secondary current flow. During the flyback interval C5 acquires a charge of about 1 volt from current drawn from R17 which is clamped by the base-collector junction of Q4.

Transistors Q1, Q2, and Q3, along with op-amp U1 and associated resistors and diodes and regulator-winding transformer (terminals 2 and 1), constitute the voltage regulator portion of the power supply. Until the output voltages reach their correct values, the power transistor collector current ramps up to its current limit as set by Q4 each cycle, transferring the maximum safe amount of energy each cycle to the filter capacitors and output loads. The capacitors C1 and C2 are charged to the average value of the flyback square wave voltage from the sense winding (less a diode drop) during each cycle. As soon as the voltage is developed across C1, the negative input of U1, because of the voltage divider formed by R3, R4, and R5, becomes negative with respect to its positive input which, since zener diode ZD1 passes essentially zero current until its breakdown voltage is approached, is held at the full output voltage of C2 through R7 and R8. This assures that the op-amp will remain in positive saturation and Q1 will be off.

As the regulator outputs rise toward their correct values and the voltage across C1 increases proportionally, the voltage at the U1 positive input is clamped as ZD1 begins conducting. Voltage then appears across R7 because of current in R8. The voltage on the negative input of U1 approaches that of its positive input and the voltage at U1 pin 6 drops. As its base voltage falls below the output of C2 by two diode drops, Q1 begins to conduct, acting essentially as a controlled constant current source whose output current flows into oscillator timing capacitor C4. Voltage regulation commences with Q1 conduction.

is negative. This makes D6 conduct and thereby clamps the timing capacitor to ground through the base-collector diode of Q2, sinking the output of current source Q1. When the power transistor Q5 switches on after flyback ends, R9 is taken positive by the base drive winding, thus causing Q2 to operate as an emitter-follower, buffering the timing capacitor C4. The voltage across C4 then begins to ramp up to a rate proportional to the current from Q1. When the increasing voltage across C4 reaches approximately two diode drops, the output of buffer Q2 begins to rapidly energize Q3, which shunts drive current from Q5 and causes its regenerative turnoff just as does current limiter Q4. The action of regulator loop thus controls

the power transistor on-time and thereby the peak current flowing in the transformer primary.

The voltages across C2 and C1 are held constant by U1 operating at its full dc open loop gain to maintain zero differential input voltage. Constant voltages across C2 and C1 imply that the flyback voltage remains constant, and since all windings are tightly coupled the flyback or output voltage from all windings remains constant. Therefore, the line regulation is achievable within a wide range of line variation.

When the load increases, greater current is required of the supply and the power transistor Q5 must remain on for longer periods of time. To accomplish this, U1 senses a lower flyback voltage due to the increase of load, and lowers the output current of Q1, which causes C4 to take longer to charge, the longer that Q5 is on each cycle and the more energy is input to the load. Conversely, when the load decreases, less current is required of the supply. The power transistor Q5 must remain on for shorter period of time. To accomplish this, U1 senses a higher flyback voltage and increases the output current of Q1, which causes C4 to charge faster. The faster C4 charges, the less time Q5 is on each cycle, and the less energy is input to the load.

The failure protection circuit provides protection to the power supply and its load against output overvoltage or sustained overcurrent. When the short circuit or overcurrent occur at the output circuit, the collector current of power transistor Q5 increases to the limit beyound the current limit of F3. The open circuit of F3 protects the rest of circuit for being further damaged. The overvoltage protection is provided by ZD2 and F1. This circuit senses the flyback voltage of the power supply, the overvoltage of primary side will induce a higher flyback voltage. When the flyback voltage increase enough to turn on ZD2 and the current through F1 is more than 125ma, the blowing of F1 will take place. As soon as the open of F1 occurs, Q4 is biased on and Q5 is biased off.

99/7 system overtemperature protection is provided by shutting down the power supply when a temperature-operated reed switch opens on the Up Board (UP BD SH. 10). The opening of this switch causes -TRIP to go low (from ground to -5v) which triggers the optically-isolated SCR of the GE H11C3 isolator. This SCR shorts out R30 (51K), thereby turning on Q4 which turns off Q5 and shuts down the power supply. The SCR will stay conducting until the AC ON/OFF switch is turned OFF. Therefore, user intervention is required to restore system operation following an overtemperature condition.