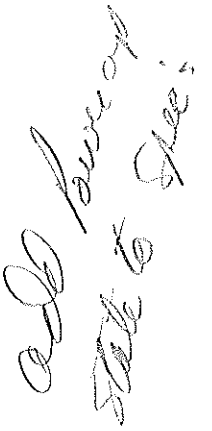

99/4B CPU PCB

SPEC DWG. #0000001

10/15/81

7/06/81

* First pass effort.

10/02/81

* Updated to reflect S/W Review requirements.

10/5/81

* Added CRU bit for mapper enable, paragraph on LED, general spelling and clarification.

10/12/81

* Added paragraph on MEMEN control and memory protect.

10/15/81

* Added paragraphs on DMAC, PCB disable for testing, and Single Instruct capability.

SECTION 1

CPU PCB ELECTRICAL DEFINITION

1.1 GENERAL

* Bus drivers and recievers shall be physically located close to the busses they are connected to. Priority shall be given to the System Bus buffers.

* Memory/CRU space decodes shall comprehend PLA decoding as a cost reduction path.

* Adequate decoupling shall be provided on the logic.

* Ground return etch paths shall be taken in the shortest practical path directly to the chips that drive (or receive) the System Busses.

1.2 DESIGN VERIFICATION

Characterization with respect to System level propogation delays shall be done on all of the QUAL units and others as is required. If any negative deviations from design values are found, they shall drive any design changes required.

1.3 TEST CONSIDERATIONS

Signature Analysis shall be designed in as the primary fault isolation tool, and test specifications for this PCB shall written after both design and prototype debug have been completed.

1.4 CPU PCB ORGAINZATION

The 99/4B CPU PCB shall be organized in five distinct functional blocks: 1) the uP, 2) the BOOT ROM, 3) the 16-bit to

19-bit Memory Mapper, 4) the logic to separate the TMS 9900 like control signals from those of the TMS 9995, and 5) misc logic and System Bus buffers.

1.4.1 CPU. The CPU shall be a TMS 9995 uP clocked with a derivative of the 10.738635 MHz System Clock. Since the uP clock ultimately clocks other functions (such as the 9902 UART), it shall not be manipulated in place of READY.

1.4.2 BOOTROM. The BOOTROM chip select shall be a function of the RESET configuration bit, and Physical Address locations >00000, and >7C000. The RESET configuration bit shall be a CRU Output bit located in the CRU space at >00004, and when reset (due to either a System RESET or a SBZ operation), the logical condition is met to enable the BOOTROM at >00000. The BOOTROM shall always respond at >7C000.

A SBO @ >00004 shall inhibit the BOOTROM from responding at the >00000 base, but as was previously mentioned, it will always respond at >7C000.

1.4.3 Memory Mapper. The Memory Mapper shall have the following characteristics.

* Shall map the 16-bit uP Logical Address space into the 19-bit Physical Address space.

* Shall pass a CRU Address unmodified.

* Shall be disabled ~~when~~ by a CRU SBZ instruction, and re enabled by a SBO at the same CRU address.

* Each Page Base Register (PBR) shall be 8-bits wide, and 16 PBRs shall be provided.

* The Physical Address shall be formed such that the least significant 11 bits of the TMS9995 (Logical Address or LAS)) are also the least significant 11 bits of the Physical Address Space (PAS). The most significant 8 bits of the PAS shall be the sum of the single LAS bit 4 and the 8-bit Page Base Register value. The most significant 4 bits of the Logical Address shall be used to select the PBR (of 16 possible).

* The PBR file shall be READ FROM and WRITTEN TO by CRU operations.

* The CRU space from >04000 to >05FFE shall be allocated to the PBR file.

* A READ PBR shall be accomplished with a STCR Ri,8 instruction. R12 shall be formatted as follows.

R12 = |010Z|ZZZ0|0000|0000|.

ZZZZ is the 4-bit PBR field

* The WRITE PBR shall be accomplished with either a SBZ or a SBO instruction with R12 formatted as follows:

|010Z|ZZZX|XXXX|XXX0|,

ZZZZ is the 4-bit PBR field,
XXXXXXXX is data to be stored.

The Physical Address (PA) is obtained from the Logical Address (LA) and the PBR as follows.

LA (9995) LS 12 bits								S	T	T	T	T	T	T	T	T	T	T	T
PBR Data				U	U	U	U								
PA	V	V	V	V	V	V	V	V	T	T	T	T	T	T	T	T	T	T	T

* Note that the MS 4 bits of the LA select one of sixteen PBRs.

1.4.4 Control Signal Separation. The following control signals shall be separated and used to drive the system busses: 1) CRUCLK*, and 2) WE*.

1.4.4.1 Memory Cycle Suppression. All memory control signals shall be trapped and not asserted on the System level for internal TMS9995 memory accesses. This logic shall trap the following two disjoint and unequal spaces: 1) from Logical Address >F000 through >F0FF, and 2) from Logical Address >FFF8 through >FFFF. Note that these addresses will be Black Holes in the Physical Address space that the LAS containing this memory is mapped into.

1.4.4.2 MEMEN* control. MEMEN* at the system level shall be controlled such that the System Address lines and DBIN are stable when MEMEN* goes LOW. Additionally, MEMEN* shall be controlled such that pseudo static ROMs may be used.

1.4.4.3 CRU Cycle Suppression. All CRU control signals shall be trapped and not asserted on the System level for internal TMS9995 CRU accesses. This logic shall trap the following disjoint 16-line and 1-line CRU addresses: 1) from LAS >1EE0 through >1EFE, and 2) >1FDA.

1.5 WAIT CYCLES

The TMS 9995 shall execute at least one WAIT state for each Memory and CRU cycle. The clock to the TMS 9995 shall NOT be manipulated to lengthen these cycles.

1.6 MEMORY PROTECTION

A CRU controlled feature shall be included to protect two segments of the Logical Address Space from being written into when the option is enabled. When the CRU Output bit is ON, writing into any location in the LAS ranging from >0000 through >01FF and from >F800 through >FFFF shall be inhibited. Normal writing shall occur when the CRU Output bit has been set OFF.

1.7 DMA CONTROL

Logic shall be provided to give DMA capabilities. Memory oriented signals generated by the DMAC shall be identical in timing to those of the TMS 9995.

1.8 SINGLE INSTRUCT CONTROL

Logic shall be included to provide Single Instruct operation. This logic shall be under S/W control by way of a CRU Output bit, and shall interface to the TMS 9995 through the NMI input.

1.9 PCB ENABLE

A single line on the System I/O Bus shall be used to disable (when active LOW) the CPU PCB for burn in purposes. It shall be acceptable to parallel this pin with the DMA control (HOLD*) if that function releases all of the System Bus from CPU PCB

control. Otherwise, additional logic shall be provided for Burn In use.

1.10 LED INDICATOR

A LED shall be provided and controlled by a CRU Output bit that may be used under Software control to indicate PCB activity as well as GOOD/BAD status. The exact control of this LED shall be defined in the Software Specifications.

1.11 SYSTEM BUS PIN DEFINITION

PIN #	MNEMONIC	FUNCTION
1		+12V 3-T Regulator supply voltage
2		+12V 3-T Regulator supply voltage
3		-12V 3-T Regulator supply voltage
4		-12V 3-T Regulator supply voltage
5	CRUIN	CRU INPUT sense line
6	MEMEN.A*	active LOW memory request
7	GND	Logic Ground
8	WE.A*	active LOW Write Enable
9	CRUCLK.A*	active LOW CRU Output Clock
10	DBIN.A	Data Bus Dir'tn, HIGH is CPU READ
11	GND	Logic Ground
12	CLKOUT*	Active LOW CPU Clock
13	GND	Logic Ground
14	AMC.A	Address Bit, (MSB, 99/4B)
15	AMB.A	Address Bit
16	AMA.A	Address Bit
17	A00.A	Address Bit, (MSB, Johnny Box)
18	A01.A	Address Bit
19	A02.A	Address Bit
20	A03.A	Address Bit
21	A04.A	Address Bit
22	A05.A	Address Bit
23	A06.A	Address Bit
24	A07.A	Address Bit
25	A08.A	Address Bit
26	A09.A	Address Bit
27	A10.A	Address Bit
28	A11.A	Address Bit
29	A12.A	Address Bit
30	A13.A	Address Bit
31	A14.A	Address Bit
32	A15/COUT.A	Address Bit, LSB
33	GND	Logic Ground
34	D0	System DATA Bus, MSB
35	D1	System DATA Bus
36	D2	System DATA Bus
37	D3	System DATA Bus
38	D4	System DATA Bus
39	D5	System DATA Bus
40	D6	System DATA Bus
41	D7	System DATA Bus, LSB
42	GND	Logic Ground

System Bus Pin Definitions, Continued

PIN #	MNEMONIC	FUNCTION
43	INTA*	Interrupt Level A common line
44	INTB*	Interrupt Level B common line
45	SENILA*	Sense request for Interrupt Level A
46	SENILB*	Sense request for Interrupt Level B
47	HOLD*	active LOW HOLD request for DMA
48	IAQHDA	active HI IAQ/ HOLD Acknowledge
49	RBDEVAK	not ~~assigned~~ used
50	PCBEN	active HIGH PCB enable for Burn In
51	BOOTPG*	BOOT ROM control, 0=respond @>00000
52	AUDIO	Audio input
53	GND	Logic Ground
54	SCLK	10.738635 MHz System Clock
55	GND	Logic Ground
56	RESET*	active LOW System driven RESET
57	GND	Logic Ground
58	READY.A	READY for Memory/CRU control
59		+5V 3-T Regulator supply voltage
60		+5V 3-T Regulator supply voltage