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SECTION 1

INTRODUCTION

1.1 DESCRIPTION

THE CF40051 I/O CONTROLLER (IOC) IS A TAL004, LOW-POWER-SHOTTKY-TTL BIPOLAR GATE ARRAY FOR USE IN THE GROUND SQUIRREL SYSTEM. THE IOC PROVIDES THE INTERFACE BETWEEN THE CPU AND THE KEYBOARD, THE ALC PERPHERIAL BUS, AND THE CASSETTE CIRCUITRY; SYSTEM MEMORY SELECT FOR BOTH THE CPU AND THE VIDEO DISPLAY CONTROLLER (VDC); A DIVIDE BY TWO OF THE 10.7MHZ OSCILLLATOR SIGNAL; AND A RESET SYNCHRONIZED TO CPU CLK.

THE IOC INTERFACE IS TO EITHER SYSTEM MEMORY CONTROL OR CRU-DATA TO/FROM EXTERNAL DEVICES. THE INTERMODE AND INTRAMODE SELECTION IS OBTAINED FROM ADDRESS DECODE AND TWO DATA CONTROL SIGNALS FROM THE CPU.

THE CRU INTERFACE ENABLES SERIAL DATA FROM THE CPU TO THE EXTERNAL DEVICES OR FROM THE EXTERNAL DEVICE TO THE CPU. THE EXTERNAL INTERFACES ARE CRU-OUT DATA TO 1-OF-6 OUTPUTS FOR THE KEYBOARD, WITH THE CRU-IN SCANNING DONE EXTERNAL TO THE IOC, SERIAL CRU-OUT TO THE CASSETTE OR SERIAL CRU-IN DATA FROM THE CASSETTE, AND ALC-BUS WITH A SERIAL CRU TO PARALLEL 4-BIT DATA I/O BUS, A HANDSHAKE I/O LINE, AND A BUS-AVAILABLE I/O LINE.

THE SYSTEM MEMORY CONTROL IS BY THREE CHIP SELECTS, THEY SELECT A 16K BLOCK OF ROM, A 8K BLOCK OF ROM , OR A 4K BLOCK OF RAM. THESE BLOCKS OF MEMORY CAN BE ACCESSED BY EITHER THE CPU OR THE VDC AS DETERMINED BY THE TWO DATA CONTROL SIGNALS.

1.2 FEATURES

* SINGLE 5 VOLT SUPPLY
* 40-PIN DUAL IN LINE PACKAGE
* MEMORY CHIP SELECTS FOR CPU AND VDC
* SERIAL CRU INTERFACE
  - KEYBOARD
  - CASSETTE RECORDER
  - HEX PERPHERIAL BUS
* SYNCHRONIZED RESET
* DIVIDE BY TWO

SECTION 2

FUNCTIONAL DESCRIPTION

2.1 FUNCTIONAL BLOCKS

2.1.1 CHIP SELECTS.

THERE ARE 3 CHIP SELECT OUTPUTS; CS0, CS1, AND CS2 WHICH ARE DECODES OF THE ADDRESS LINES A15, A14, AND A13. CS0 DECODES ON >0XXX TO SELECT THE FIRST 16K BLOCK OF ROM. CS1 DECODES ON >4XXX TO SELECT A SECOND 8K BLOCK OF ROM. CS2 DECODES ON >EXXX AND IS THE SELECT FOR 4K OF RAM.

THE CHIP SELECT OUTPUTS ARE ENABLED WHENEVER THERE IS A MEMORY ACCESS INITIATED BY EITHER THE CPU OR THE VIDEO DISPLAY CONTROLLER. THE DISTINCTION IS MADE BY HOLDA AND MEMEN SIGNALS ACCORDING TO THE FOLLOWING:

ENABLED	HOLDA	MEMEN	CONTROL
YES	LOW	LOW	CPU
NO	LOW	HIGH	
YES	HIGH	LOW	CPU
YES	HIGH	HIGH	VDC

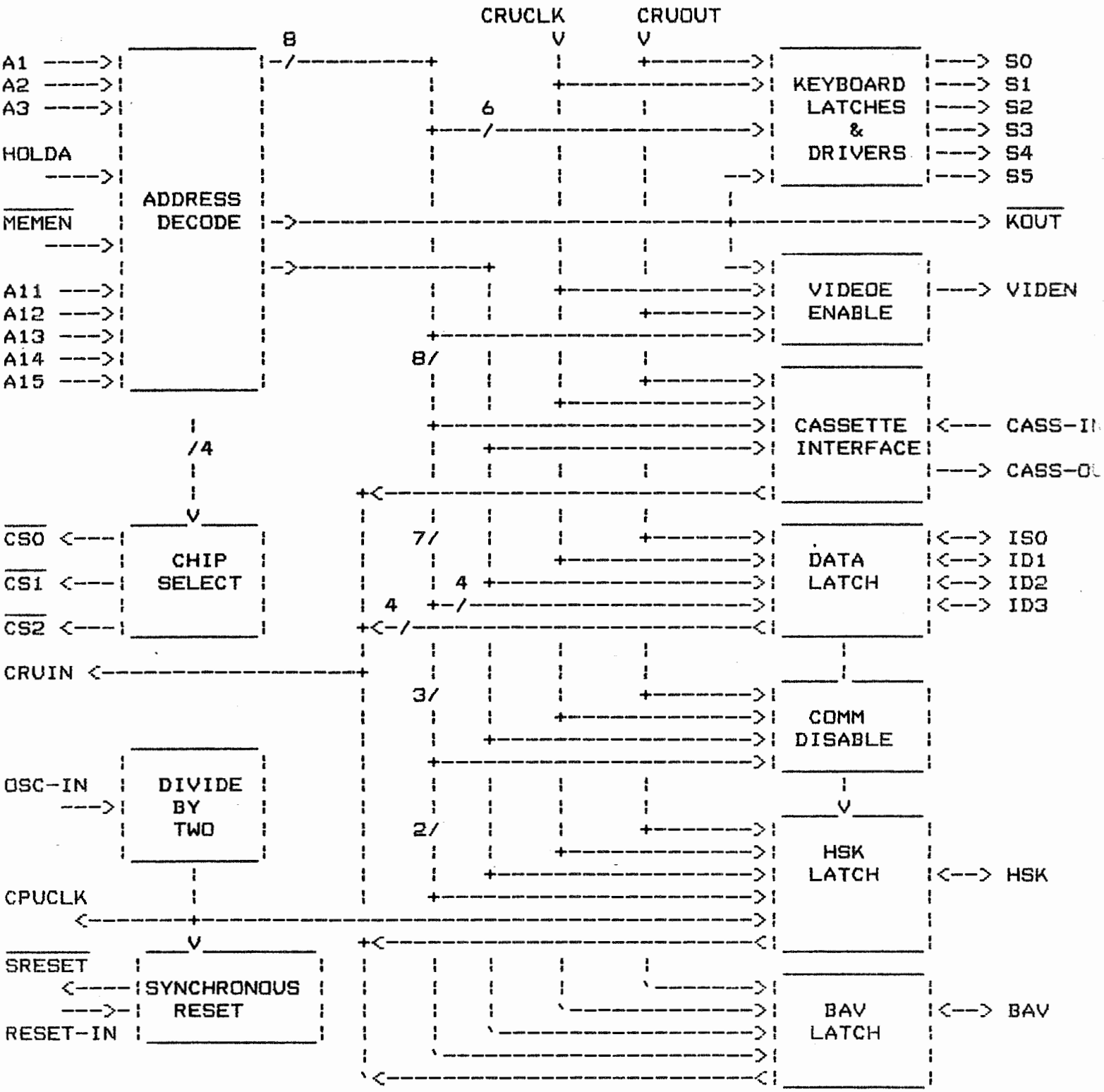

FIGURE 2-1
IOC BLOCK DIAGRAM

2.1.2 CRU ADDRESS DECODE.

THE CRU DEVICES ARE CONTROLLED BY ADDRESSS A15 THROUGH A11 (THE MSBS), AND A3, A2, AND A1 (THE LSBS).

NOTE

THE A0 BIT IS NOT DECODED SINCE IT CARRIES CRUOUT DATA IN THE CRU MODE.

THE CRU ADDRESS'S DECODED ARE >E000 TO >E00E, AND >E800 TO >E80E. THE CRU INTERFACE TO EXTERNAL DEVICES IS ENABLED WHEN HOLDA=LOW AND MEMEN=HIGH. THE FUNCTION OF EACH OF THE INDIVIDUAL ADDRESSS WILL BE DEFINED IN THE FOLLOWING SECTIONS.

2.1.3 KEYBOARD CONTROL.

THE KEYBOARD INTERFACE CONSISTS OF SIX OUTPUTS TO SCAN FOR KEY CLOSURES. THE OUTPUTS ARE OPEN COLLECTOR DEVICES WITH INTERNAL PULL-UP RESISTORS TO PREVENT THE POSSIBILITY OF SHORTING A DRIVEN OUTPUT ACROSS THE KEYBOARD. SHORTING COULD OCCUR IF TWO OR MORE KEYS WERE PUSHED SIMULTANEOUSLY, AND ONE OUTPUT COULD BE DRIVEN HIGH AND ONE WAS DRIVEN LOW.

THE SIX OUTPUTS CAN BE SET OR RESET WHEN THE CRUOUT DATA FROM THE CPU IS HIGH OR LOW, RESPECTIVELY. OUTPUT CONTROL IS PROVIDED BY THE CRU ADDRESS DECODE. ADDRESSS >E000 , >E002, >E004, >E006, >E008, AND >E00A ENABLE THE CRUOUT DATA TO BE LATCHED ON THE FALLING EDGE OF CRUCLK TO OUTPUTS S0, S1, S2, S3, S4, AND S5, RESPECTIVELY.

ALL OUTPUTS WILL BE CLEARED TO A LOW LEVEL ON POWER UP CLEAR (PUC). AT ALL OTHER TIMES THE OUTPUTS WILL BE AT THE LAST LATCHED STATE UNTIL CHANGED.

A LOW TRUE OUTPUT IS PROVIDED AS AN ENABLE TO AN EXTERNAL KEYBOARD-TO-CRUIN INTERFACE. THE CONTROL SIGNAL IS VALID DURING CRU BASED OPERATIONS FOR ADDRESSS >E000 TO >E00E.

2.1.4 VIDEO ENABLE.

A VIDEO ENABLE SIGNAL IS PROVIDED AS A CRU CONTROL OF THE VDC CHIP. THE OUTPUT IS AN OPEN COLLECTOR OUTPUT WITH AN INTERNAL PULL-UP RESISTOR. THE OUTPUT CAN BE SET OR RESET WHEN THE CRUOUT DATA IS HIGH OR LOW ,REPECTIVELY. THE OUTPUT WILL BE LATCHED ON CRU ADDRESS >E00E AND THE FALLING EDGE OF CRUCLK, AND WILL BE HELD UNTIL THE NEXT SET OR RESET.

THE VIDEO ENABLE OUTPUT WILL BE CLEARED LOW UPON POWER UP CLEAR AND REMAIN LOW UNTIL A SET OPERATION IS COMPLETED. THIS LOW STATE WILL DISABLE THE VDC AND MUST BE SET HIGH WHEN VIDEO IS TO BE DISPLAYED.

2.1.5 CASSETTE INTERFACE.

THE CASSETTE INTERFACE CIRCUTS ENABLES THE CRUOUT DATA TO BE LATCHED TO THE CASSETTE OUTPUT WHEN THE CRU ADDRESS >E80E IS VALID AND THE FALLING EDGE OF CRUCLK OCCURS. IT WILL BE SET OR RESET IF THE CRUOUT DATA IS HIGH OR LOW, RESPECTIVELY. THE DATA OUT WILL BE LATCHED AND HELD AT ITS LAST STATE UNTIL CHANGED BY THE NEXT SET OR RESET.

THE CASSETTE OUTPUT WILL BE CLEARED TO A LOW UPON POWER-UP-CLEAR.

THE CASSETTE-IN DATA IS ENABLED TO CRU-IN ON ADDRESS >E80E ALSO. THE CRU-IN WILL BE ACTIVE, WITH CASSETTE-IN, AT ALL TIMES WHEN ADDRESS >E8XX IS VALID, AND IT IS UP TO THE CPU WHEN TO READ THE DATA.

NOTE

THERE ARE NO INTERRUPTS GENERATED FROM THE CASSETTE INPUT DATA. IT MUST BE HANDLED ON A POLLED BASIS.

2.1.6 ALC-BUS INTERFACE.

THE ALC-BUS INTERFACE CONSISTS OF SIX INPUT/OUTPUTS; A 4-BIT DATA I/O (ID0-ID3), A HANDSHAKE I/O (HSK), AND A BUS-AVAILABLE I/O (BAV). ALL SIX OUTPUTS ARE TRI-STATE BUFFERS THAT ACT AS OPEN COLLECTOR OUTPUTS IN THAT THEY CAN PULL THE OUTPUT LOW BUT NOT HIGH.

NOTE

PULLUP RESISTORS ARE NOT PRESENT INTERNALY AND MUST BE PROVIDED EXTERNALLY TO PULL THE BUS HIGH.

THE I/O'S ARE CONTROLLED BY CRU ADDRESS'S AS FOLLOWS; >E800, >E802, >E804, AND >E806 FOR THE DATA I/O'S, ID0-ID3 RESPECTIVELY, >E808 FOR HANDSHAKE, AND >E80A FOR BUS AVAILABLE. IN ADDITION ADDRESS >E80C IS AVAILABLE AS A COMMUNICATION DISABLE.

THE SIX INPUTS ARE ENABLED TO THE CRUIN WHEN ITS PARTICULAR ADDRESS IS VALID AND WILL REMAIN DYNAMICALLY ACTIVE AS LONG AS ITS ADDRESS REMAINS VALID.

2.1.6.1 BUS AVAILABLE I/O.

THE BAV OUTPUT IS A LATCHED OUTPUT OF THE CRUOUT DATA. CRUOUT DATA HIGH/LOW WILL SET/RESET, RESPECTIVELY, THE BAV OUTPUT WHEN THE CRU ADDRESS >E80A IS VALID AND CRUCLK TRANSITIONS LOW.

THE BAV OUTPUT WILL BE CLEARED TO A HIGH-Z ON POWER UP.

2.1.6.2 DATA I/O.

THE FOUR DATA OUTPUTS (IDO-ID3) ARE LATCHED OUTPUTS FOR THE CRUOUT DATA. THE DATA IN THE LATCHES IS ENABLED TO THE OUTPUT DEVICE ONLY WHEN HSK IS LOW. DATA MAY BE WRITTEN TO THE LATCH BEFORE HSK GOES LOW, WHICH IS NORMALLY THE CASE, BUT WILL NOT BE OUTPUTTED. NEW DATA IS LATCHED IN WHENEVER ITS ADDRESS IS VALID AND THE FALLING EDGE OF CRUCLK OCCURS, PROVIDED ONE OF THE CLEAR CONDITIONS IS NOT PRESENT.

THE CLEAR CONDITIONS (OUTPUT TO A HIGH-Z) ARE POWER UP AND ANY OF THE FOLLOWING;

1. BAV IS HIGH
2. COMMDISABLE LATCH IS RESET
3. COMMDISABLE LATCH HAS BEEN RESET THEN SET AND BAV IS STILL LOW
4. ONE CPUCLK CYCLE AFTER HSK TRANSITIONS LOW TO HIGH

2.1.6.3 HANDSHAKE.

THE HSK-OUT LATCH WILL BE SET OR RESET, WITH CRUOUT DATA HIGH OR LOW, WHEN THE CRU ADDRESS >E80A IS VALID AND THE FALLING EDGE OF CRUCLK OCCURS. THE OUTPUT WILL REMAIN AT THE LAST STATE UNTIL THE NEXT SET/RESET OCCURS.

HSK-OUT WILL BE CLEARED TO A HIGH-Z ON POWER UP.

A LOW ON THE HSK INPUT, IF HSK-OUT LATCH IS RESET, WILL BE LATCHED AFTER DEBOUNCE AND HELD UNTIL RELEASED BY A SET-RESET OF THE HSK-OUT LATCH (ADDRESS >E808). THE INPUT IS DEBOUNCED FOR 5.5 OR 6.5 CPUCLK CYCLES (APPROXIMATELY 1.0 TO 1.2 MICROSECONDS) BEFORE LATCHING. THE DEBOUNCE CIRCUIT WILL PREVENT FALSE LATCHES OF HSK.

THE HSK-IN LATCH IS CLEARED ON POWER UP, AND WILL BE CLEARED AND HELD CLEARED WITH THE CONDITIONS LISTED IN ITEMS 1,2, AND 3 OF THE PRECEEDING SUBSECTION.

2.1.6.4 COMMUNICATION DISABLE.

THE COMMDISABLE LATCH ALLOWS THE MAIN PROCESSOR UNIT TO COMPLETELY IGNORE BUS COMMUNICATIONS, IF IT SO DESIRES, BY HOLDING THE HSK-IN LATCH CLEARED. THIS MAY BE DONE UNDER TWO CONDITIONS, FIRST WHERE THE CPU WANTS TO IGNORE ALL FURTHER COMMUNICATIONS, AND SECOND WHERE THE CPU DOES NOT WANT TO PARTICIPATE IN ANY FURTHER COMMUNICATIONS WITHIN THE PRESENT BAV CYCLE.

UNDER THE FIRST CONDITION, TO IGNORE ALL COMMUNICATION, THE COMMDISABLE LATCH AT CRU ADDRESS >E80C IS RESET AND HELD RESET UNTIL CHANGED BY THE MAIN PROCESSOR.

UNDER THE SECOND CONDITION, NO COMMUNICATION DURING THE ONGOING BAV CYCLE, THE COMMDISABLE LATCH WOULD BE RESET THEN SET IMMEDIATELY. THIS CONDITION WILL HOLD THE HSK-IN LATCH CLEARED UNTIL THE NEXT BAV CYCLE BEGINS.

THE COMMDISABLE LATCH WILL BE SET OR RESET, WITH HIGH OR LOW CRUOUT DATA RESPECTIVELY, WHEN THE CRU ADDRESS >E80C IS VALID AND THE FALLING EDGE OF CRUCLK OCCURS.

THE LATCH WILL BE CLEARED TO THE DISABLE MODE (COMMDISABLE LATCH RESET) AT POWER UP, AND MUST BE SET HIGH BEFORE ANY COMMUNICATION CAN TAKE PLACE.

2.2 DIVIDE BY TWO

THE DIVIDER HALVES THE 10.7 MHZ OSCILLATOR INPUT FREQUENCY AND OUTPUTS IT ON CPUCLK. THERE IS NO INITILIZATION OF THE DIVIDER ON POWER UP, BUT CPUCLK WILL CHANGE ON THE RISING EDGE OF OSCIN.

2.3 SYNCHRONOUS RESET

THE SYNCHRONOUS RESET HAS A SCHMITT INPUT WHICH MUST BE LOW AT POWER UP. THE RESET OUTPUT WILL THEN BE LOW AT POWER UP AND WILL GO INACTIVE HIGH ON THE FIRST LOW TRANSITION OF CPUCLK AFTER THE RESET INPUT GOES ABOVE THE SCHMITT TRANSITION LEVEL.

SECTION 3

IOC PIN ASSIGNMENTS

SIGNATURE	PIN#	I/O	DESCRIPTION
OSCIN	1	IN	10.7 MHZ INPUT
CPUCLK	2	OUT	5.35 MHZ OUTPUT
RESETI	3	IN	RESET INPUT
SRESETB	4	I/O	SYNCHRONIZED RESET
BAV	5	I/O	BUS-AVAILABLE
HSK	6	I/O	HANDSHAKE
ID3	7	I/O	DATA I/O
ID2	8	I/O	DATA I/O
ID1	9	I/O	DATA I/O
GND	10	IN	POWER
ID0	11	I/O	DATA I/O
VIDEN	12	OUT	VIDEO ENABLE
S5	13	OUT	KEYBOARD SCAN
S4	14	OUT	KEYBOARD SCAN
S3	15	OUT	KEYBOARD SCAN
S2	16	OUT	KEYBOARD SCAN
S1	17	OUT	KEYBOARD SCAN
S0	18	OUT	KEYBOARD SCAN
CASSOUT	19	OUT	CASSETTE INTERFACE
CRUCLKB	20	IN	CRU CLOCK
VCC	21	IN	POWER
CRUOUT	22	IN	SERIAL CRU DATA
CASSIN	23	IN	CASSETTE RECORDER DATA
KOUTB	24	OUT	KEYOARD INTERFACE CONTROL
HOLDAB	25	IN	HOLD ACKNOWLEDGE
A1	26	IN	ADDRESS
A2	27	IN	ADDRESS
A3	28	IN	ADDRESS
MEMENB	29	IN	MEMORY ENABLE
A11	30	IN	ADDRESS
GRD	31	IN	POWER
A12	32	IN	ADDRESS
A13	33	IN	ADDRESS
A14	34	IN	ADDRESS
A15	35	IN	ADDRESS
CS0B	36	OUT	16K ROM CHIP SELECT
CS1B	37	OUT	8K ROM CHIP SELECT
CS2B	38	OUT	4K RAM CHIP SELECT
CRUIN	39	IN	SERIAL CRU DATA
VCC	40	IN	POWER

SECTION 4

ELECTRICAL SPECIFICATION

4.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE AIR TEMPERATURE RANGE

Supply Voltage, Vcc	7 V
Input Voltages	7 V
Continuous Power Dissipation	??
Operating Free-Air Temperature	0C TO 70C
Storage Temperature	-65C TO 150C

4.2 RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
VCC Supply Voltage	4.75	5.0	5.75	V
IOH High Level Output Current			-400	uA
IOL Low Level Input Current			8	mA
Ta Operating Free Air Temp	0		70	C

4.3 OPERATING CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ICC Supply Current	outputs open			??	mA
VOH High Level Output Voltage	IOH =-400uA VCC = 4.75V	2.7	3.35		V
VOL Low Level Output Voltage	IOL = 8.0mA VCC = 4.75V		0.35	0.5	V
IOS Short Circuit Output Current	VCC = 5.25V	-20	-60	-100	mA
VIH High Level Input Voltage		2.0			V
VIL Low level Input Voltage				0.8	V
VIK Input Clamp Voltage	IK = -18mA			-1.5	V
VT+ Schmitt Input Positive Going Threshold Voltage		1.4	1.68	1.9	V
VT- Schmitt Input Negative Going Threshold Voltage		0.5	0.84	1.0	V
IIH High Level Input Current	Vcc = 5.25V VI = 2.7 V			40	uA
IIL Low Level Input Current	Vcc = 5.25V VI = 0.4 V			-200	uA
II Input Current	Vcc = 5.25V VI = 7.0 V			100	uA
Ci Input Capacitance				15	pF

4.4 TIMING CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	MAX	UNIT
ts1 * Settup time CRUOUT prior to CRUCLK	0		nS
ts2 Settup time HOLDA to VALID ADDRESS	0		nS
ts3 Settup time MEMEN to VALID ADDRESS	0		nS
td1 Delay time VALID ADDRESS to CS0		45	nS
td2 Delay time VALID ADDRSES to CS1		45	nS
td3 Delay time VALID ADDRESS to CS2		55	nS
td4 ** Delay time HSK to DATA TRUE		50	nS

* Time is referenced to the falling edge of CRUCLK
** Time is referenced to the falling edge of HSK

4.5 TIMING DIAGRAMS