PARALLEL I/O FOR THE CORTEX

Now your Cortex can have a Centronics port, two joystick ports and 22 lines of programmable I/O. The brains behind this operation is Richard Roberts of MicroProcessor Engineering.

The Cortex project was initially featured in ETI in November and December 1982 and January 1983. The currently available Cortex II has a circuit and PCB which are the same as those featured in these articles in all major respects. The E-bus circuit is dealt with in ETI, December 1982 and is designed around the 74LS2001 chip which handles the bus arbitration and control logic. This is IC89 on the main board. Other chips involved in the E-bus interface which may not be present on existing Cortex boards are ICs 90 to 99.

The 74LS2001 is unavailable unless you have very good connections, so we have included a small circuit (Fig. 1) which can be built on a header and used to replace the 2001. It works for both the CRU (Communications Register Unit) I/O and memory expansion, and requires no modifications to the Cortex main board. The circuit does not allow for multiprocessors or bus time-out as it stands, but these features can be added. For those who are interested, a complete description of the E-bus, together with many examples of its use, can be found in 'E-bus System Design', Texas Instruments, Part No. MP402.

The 2001 replacement uses a 74LS74 dual latch to synchronise the E-bus READY line to the Cortex. One section of a 74LS04 hex inverter is used to invert the bus request signal to generate a bus enable.

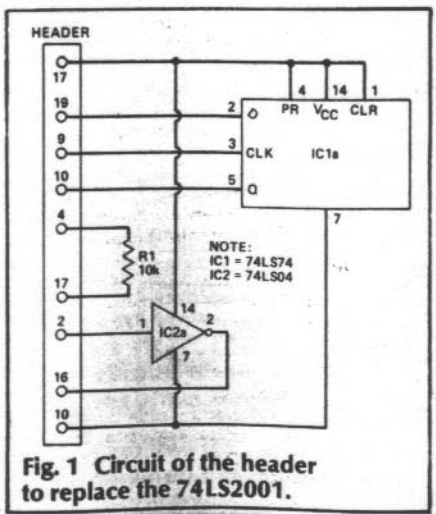


Fig. 1 Circuit of the header to replace the 74LS2001.

Construction Of The Header

As this is such a simple circuit, we have not produced a PCB, but advise the use of a small piece of veroboard. Construction should begin by cutting spots as shown in Fig. 2. Then push 20 wire wrap pins, or a 20-way wire wrap DIP socket, into the header position (top left). Solder these and the two pin IC sockets into place, fix R1 across pins 4 and 17 of the header and then insert and solder the wire links. Finally, push the ICs into their sockets.

Installing The E-bus

Plug the header into the 74SL2001 position — the 20-pin IC socket on the main board marked IC89. For the E-bus to work, the links to ground by IC94 should be cut. Use a sharp knife to break each of the four tracks from pins 2, 4, 6 and 8 of this IC. If you have fitted the memory mapper (IC26), the four wire links below it should be removed. If any other E-bus components (ICs 90 to 99, in particular) have not been fitted then now is the time to fit them.

Switch on, and you should have a working E-bus interface. If the Cortex signs on, then it is likely that the E-bus will be functioning correctly. Any faults will probably be due to miswiring on the header (check the wire wrap pins), or to solder splashes on the main board. The E-bus can be connected to a backplane for easy insertion and removal of cards, such as the one featured here. Suitable backplanes are widely available. They should be designed for 32+32 way Eurocards (DIN 41612) and the backplane will fit a 64-way right-angled male A+C plug attached to the main board of the Cortex. The backplane sockets should be female for use with the following and subsequent expansion boards. Alternatively, 64-way rightangled female A+C sockets are available, respectively of IC7 and the Cortex board for direct connection

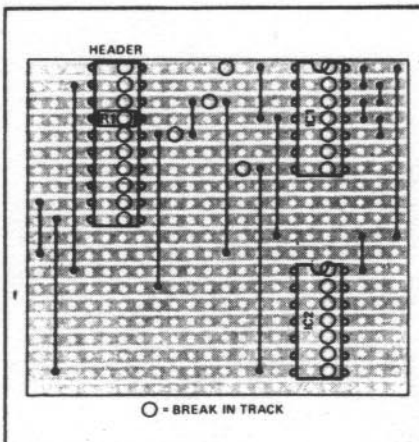


Fig. 2 Veroboard layout for the header.

of the parallel I/O board through the access port in the case.

Construction

The PCB designed to accomodate the interface is a standard double-sided through-hole plated Eurocard. Check the PCB for any shorts, especially on the component side. Fit all the IC sockets and DIN 41612 connector followed by all the passive components. If you are going to use the board only as a Centronics interface for the Cortex ,link out the fifth switch position on SW1 (address line A4, connector pin A15), otherwise fit SW1. Now fit the two D-connectors and the two IDC strips. Refer to the photograph and overlay diagram (Fig. 4) for guidance. If you are planning to use a card front, use wire wrap pins in place of the D - connectors and wrap them, along with the Centronics port, onto connectors on the panel. Last of all, fit the ICs. None require any

HOW IT WORKS

The circuit used in the parallel board's CRU interface (Fig. 3) is designed to be generally applicable when attaching devices to the Cortex E-bus. Address decoding is performed by ICs 2,3 and 5 — remembering that with TI 9900 series devices the least significant bit is A15. A six way DIP switch connected to the appropriate inputs of ICs 2 and 3 ensures that the board can be mapped according to the following table:

SWITCH No.	Address Line	Address
1	A8	0080h
2	A7	0100h
3	A6	0200h
4	A5	0400h
5	A4	0800h
6	A3	1000h

To map the board at 800h (as for a Cortex Centronics port), only switch 5 should be on.

Two NAND gates in IC6 and two inverters from IC4 give the two active low signals SELA and SELB which go to the chip enable pins of IC7 and IC8 respectively (the TMS9901 input/output devices). A third inverter from IC4 is used to produce CRUCLK from CRUCLK on the E-bus.

CRU is gated on to the bus with a three-state buffer latched with BRDSEL (IC1b). The interrupt request (INTREQ) line from the 9901s is converted to the required open collector signal by IC1a.

Output to the printer is taken from IC7. P0 to P7 are the data bits, P9 provides the BUSY input and the inverted output of P8 is the STROBE signal. A pull-down resistor is placed on the BUSY line to produce a 'non-busy' signal when no printer is connected. If your printer requires an active low BUSY and an active high STROBE, refer to the section on testing.

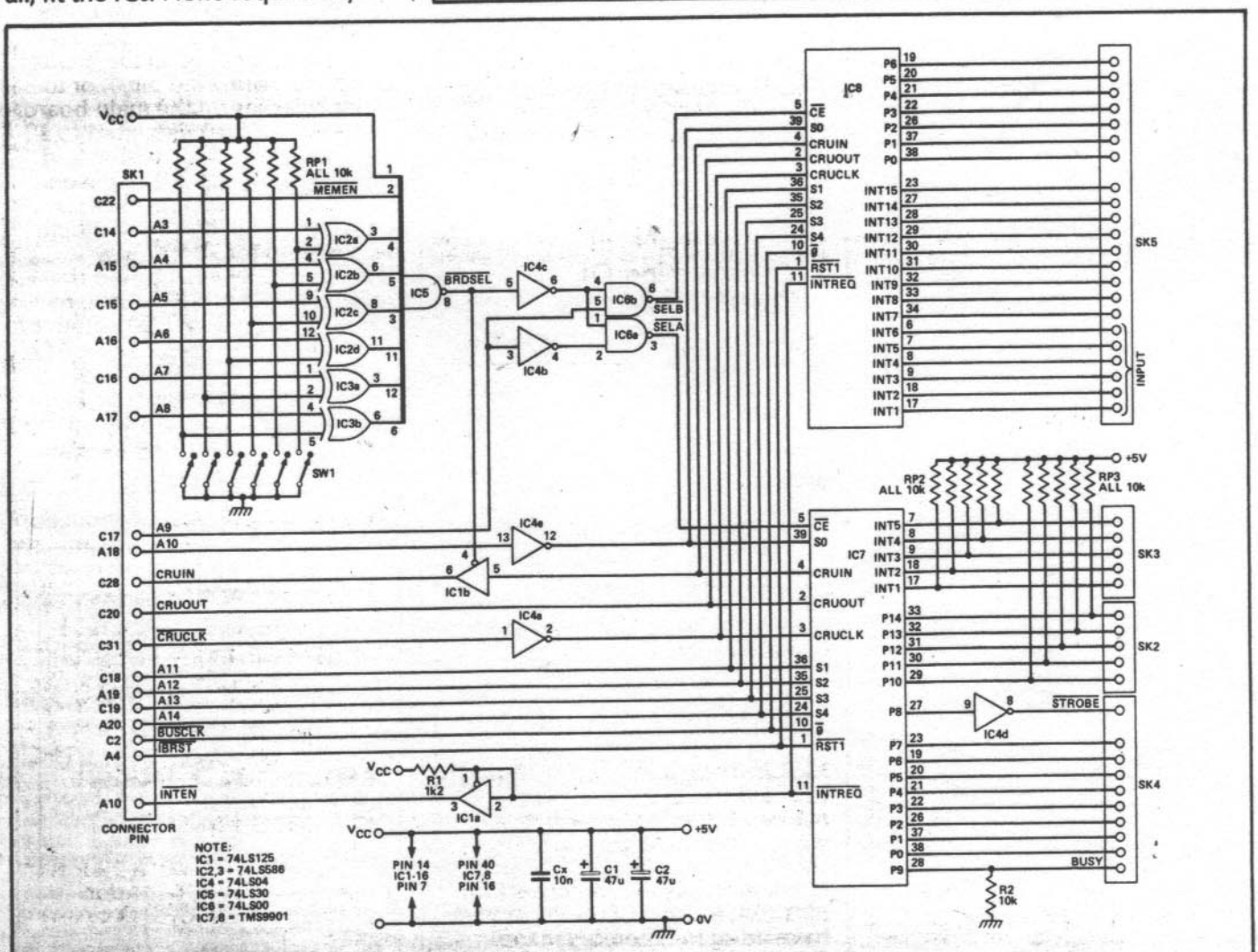


Fig. 3 Circuit diagram of the Parallel I/O board.

special anti-static handling and IC 8 is only necessary if you want the separate I/O lines.

Testing

When you plug the board into the Cortex, remember that the Cortex doesn't look like an E-bus back-plane but an E-bus board. On power-up the Cortex should act as normal. If it doesn't, your problem will most likely be a short on the address or bus control lines. If everything's okay (and assuming that you have mapped the board at 0800h), type UNIT 4 followed by a carriage return and there should be no visible response. Power down, plug the printer cable in and put the printer on line. Type UNIT 4 followed by a carriage return again and now, if you press any key followed by a carriage return, it should be echoed to the printer. If this fails check that your printer requires an active low STROBE signal and an active high BUSY signal.

If this is not the case, you will have to swap round P8 and P9 leads from pins 27 and 28, respectively of IC7 and the STROBE and BUSY lines on socket SK4. The easiest way to do this would be to cut the tracks near pins 27 and 28 of IC7 and near pins 1 and 11 of SK4 and then use short wire links to connect up the tracks in the new configuration.

The joysticks can be tested as outlined below. After you have the Centronics port working, any faults will probably be due to minor errors in the wiring or soldering.

Programming

The software to drive the Centronics port is already in the Cortex PROMs, which makes it very easy to use, The command, UNIT 4, enables the Centronics port and UNIT-4 disables it. The board must be mapped at 0800h to work with the PROM-based software.

Software to drive the joysticks is quite simple to write using the BASE and CRB commands. BASE is used to set the address of the port for use with the CRB function, which returns a value from a specified offset address. The port is wired so that the following offsets are low (value returned by CRB=0) when the relevant Joystick is active:

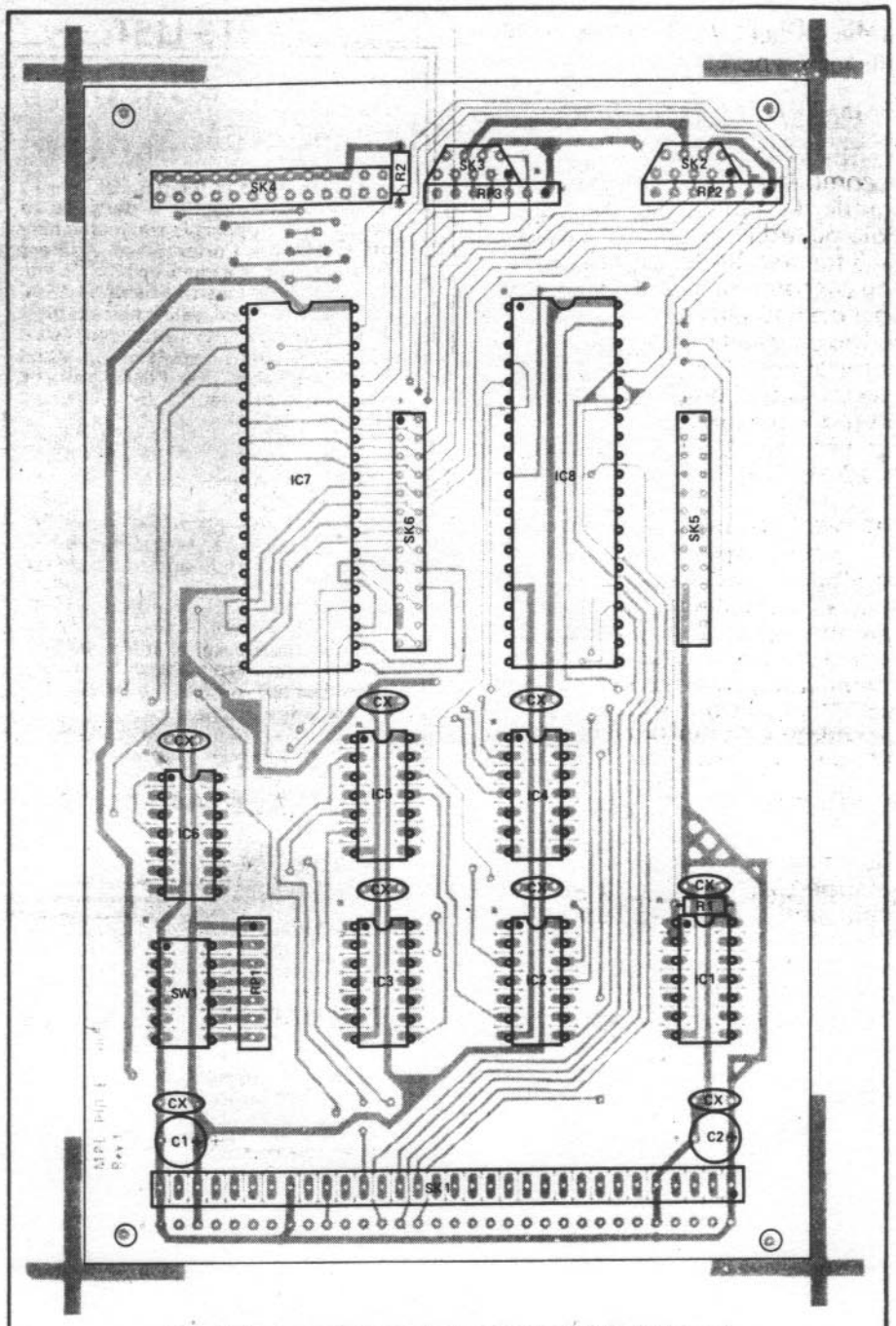


Fig. 4 Component overlay for the Parallel I/O board.

Offset	Function	Joystick
10	Right	1
11	Left	1
12	Down	1
13	Up	1
14	Fire	1
17	Fire	2
18	Up	2
19	Down	2
20	Left	2
21	Right	2

The offsets are arguments for the CRB function, so a very simple picture drawer could use the following program with a joystick in port 1:

```
100   BASE 0800H
110   X=100
120   Y=100
130   IF CRB(13)=0 THEN X=X-1
140   IF CRB(12)=0 THEN X=X+1
150   IF CRB(11)=0 THEN Y=Y-1
160   IF CRB(10)=0 THEN Y=Y+1
170   IF    CRB(14)=0    THEN
GRAPH: X=100: Y=100
180   PLOT X,Y
190   GOTO 130
```

Line 100 sets the base address and lines 130 to 170 test for movement of the joystick or fire button.

Of the uncommitted I/O lines available from the second

TMS9901, 16 can be used as input only. Applying an input current to an output pin can damage the TMS9901. The signal SELB is activated by address line A 9 going high and, therefore, the second 9901 is addressed 40h above the base set on the board. All lines can be read like the joystick ports after changing the BASE address to 0840h. Bits can be set or reset by the CRB command. To set each of the 16 outputs in turn, run;

```
100  BASE 0840H
110  FOR I=1 To16
120  CRB (I) = 1
130  NEXT I
```

For complete details of how to use the TMS9901, consult 'TMS9901 Programmable Systems Interface', Texas Instruments (part no. MP003).

Extensions

If you want further Centronics, or other, ports on your Cortex, you can patch a 16 word (32 byte) long address table at memory location 84h. Each 32-bit word holds either the address of a CRU mapped TMS9902 serial interface chip, or the address of a machine code program. If the lowest significant bit is set in this word, then the address is that of a TMS9902. If the MSB is set, then any output on that unit will have a delay on return characters. On current Cortex PROMs, the table is as follows:

Address	Unit	Value	Event	Notes
84h	01	808h	I/O to screen	mc routine
86h	02	081h	I/O to RS232	TMS9902
88h	03	181h	I/O to cassette	TMS9902
8Ah	04	754h	Centronics I/O	mc routine
8Ch	05	000h	not used	★
8Eh	06	000h	not used	★
90h	07	000h	not used	★
92h	08	000h	not used	★
94h	09	000h	not used	★
96h	10	000h	not used	★
98h	11	000h	not used	★
9Ah	12	000h	not used	★
9Ch	13	000h	not used	★
9Eh	14	000h	not used	★
A0h	15	000h	not used	★
A2h	16	000h	not used	★

If you want your Centronics printer on unit 5 instead of unit 4, for example, change memory location 8Ch to 754h, Typing UNIT 5 followed by a carriage return will now activate your printer port.

Connections

The following section gives the pin outs for sockets SK1 to SK6.

PARTS LIST

(MAIN BOARD)

RESISTORS (all 1/3W, 5%)
R1 1k2
R2 10k
RP1,2,3 7-pin 10k SIL resistor pack

CAPACITORS
C1, 2 47µ, 16V electrolytic
Cx 10n, 0.2 pitch decoupling

SEMICONDUCTORS
IC1 74LS125
IC2, 3 74LS86
IC4 74LS04
IC5 74LS30
IC6 74LS 00
IC7, 8 TMS9901

MISCELLANEOUS
SK1 64-way right-angled, male A+C DIN 41612 card connector
SK2, 3 9-pin right-angled, male D connector
SK4 13x2 right-angled IDC connector
SK5,6 13x2 straight IDC connector
SW1 6-way DIL switch
two 40 pin DIL sockets, six 14 pin DIL sockets, printer cable, PCB.

PARTS LIST (2001 REPLACEMENT)

RESISTOR
R1 10k

SEMICONDUCTORS
IC1 74LS74
IC2 74LS04

MISCELLANEOUS

Veroboard, wire-wrap pins or wire-wrap socket (20-way), two 14-pin DIL sockets, wire for links

BUYLINES

The TMS9901 should be widely available, as should all other chips. Connectors and printer leads are available from Maplin, Watford, Technomatic, Cricklewood, etc. The PCBs are available exclusively from MicroProcessor Engineering Ltd., 21 Hanley Road, Shirely, Southampton SO1 5AP (tel: 0703 780084) at a price of £13.00 for the bare board, £36.00 partially populated or £48.00 fully populated.

(N/C means not connected or reserved).

SK1 PIN	A-ROW Function	C-ROW
1	GND	GND
2	PRES	BUSCLK
3	+12V	-12V
4	IORST	NMI
5	+5V	+5V
6	+BATT	N/C
7	N/C	N/C
8	N/C	N/C
9	N/C	N/C
10	INTEN	ALATCH
11	XA0	XA1
12	XA2	XA3
13	A/D/INT 0	A/D/INT 1
14	A/D/INT 2	A/D/INT 3
15	A/D/INT 4	A/D/INT 5
16	A/D/INT 6	A/D 7
17	A/D 8	A/D 9
18	A/D 10	A/D 11
19	A/D 12	A/D 13
20	A/D 14	A/D 15/CRUOUR
21	AREADY	MEMEN
22	DEN	READY
23	GRANTIN	GRANTOUT
24	PWRFAIL	BUSY
25	GND	GND
26	+15V	ANAHI
27	ANACOM	ANALO
28	-15V	CRUIN
29	#WE-	+5STBY
30	+5V	+5V
31	MEMWIDTH	CRUCLK
32	GND	GND

SK2 AND SK3

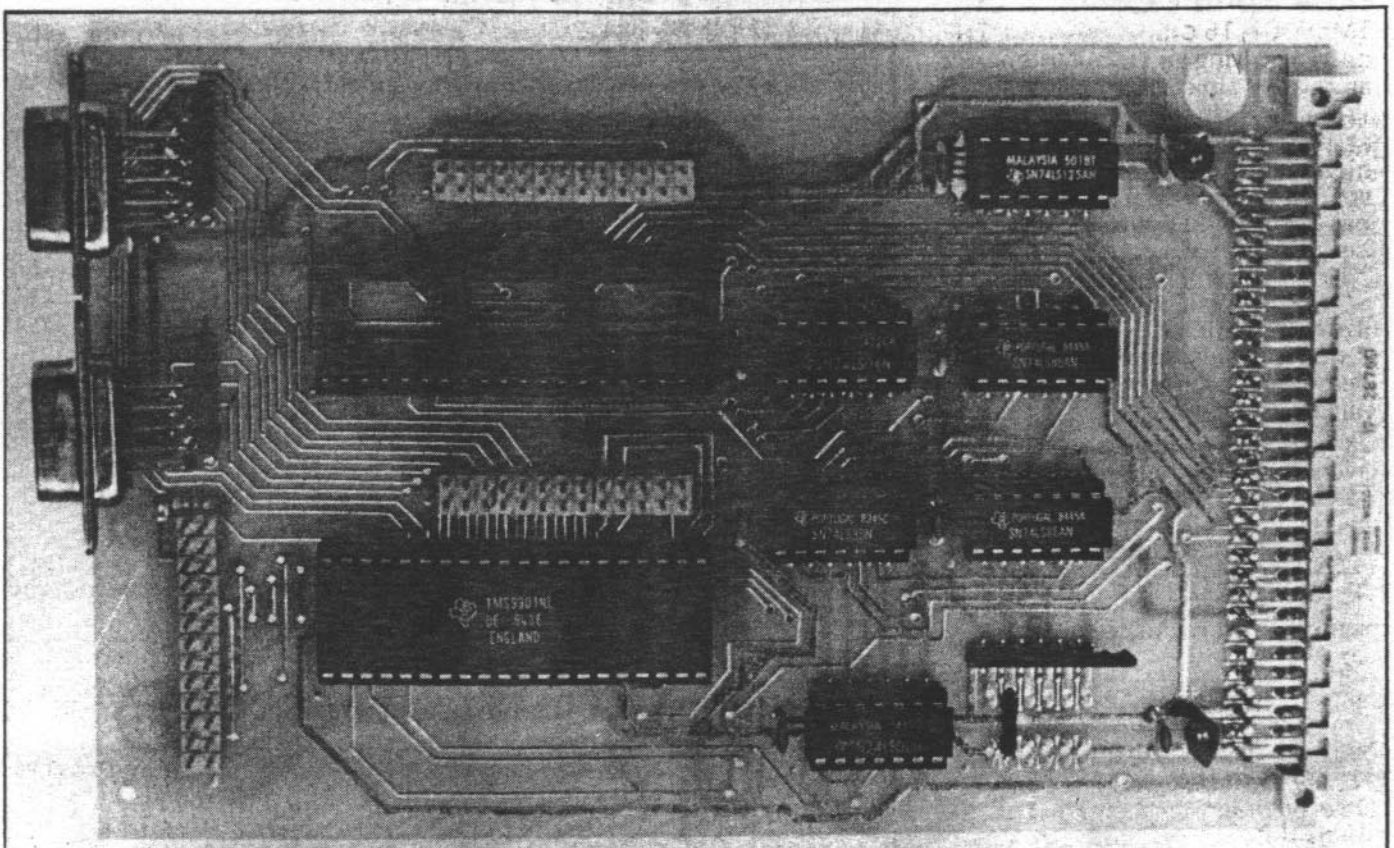
PIN	FUNCTION
1	UP
2	DOWN
3	LEFT
4	RIGHT
5	N/C
6	FIRE
7	+5V
8	GND
9	N/C

SK4

PIN	FUNCTION
1	STROBE
2	DATA 1
3	DATA 2
4	DATA 3
5	DATA 4
6	DATA 5
7	DATA 6
8	DATA 7
9	DATA 8
10	ACKNLG
11	BUSY
12	PE
13	SLCT
14-24	GND

SK5 AND SK6

PIN	FUNCTION	PIN	FUNCTION
1	INT7/P15	2	INT6
3	INT/8/P14	4	INT5
5	INT9/P 13	6	INT4
7	INT 10/P12	8	INT3
9	INT11/P11	10	INT2
11	INT12/P10	12	INT1
13	INT13/P9	14	P6
15	INT14/P8	16	P5
17	INT15/P7	18	P4
19	GND	20	P3
21	GND	22	P2
23	GND	24	P1
25	GND	26	P0



The cortex parallel I/O board configured for Centronics port and two joysticks only.

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