CORTEX PART 2

Build yourself a better brain: this month we explain the remaining Cortex circuitry and the construction of the main board.

Serial I/O on the Cortex is handled by a versatile UART, the 9902. The CPU communicates with the UART via its serial I/O bus, based on the Communication Register Unit or CRU, which requires only three wires; thus the device fits easily into an 18-pin package. The 9902 is fully programmable and the range of variations is so great that it's outside the scope of this article. In the Cortex the chip is configured to handle RS232 eight-bit codes with even parity and 1½ stop bits; the communication rate can be set from BASIC using the BAUD command and the device is activated using the UNIT statement. The parameter for UNIT is a 16-bit word, each bit corresponding to a channel that can be either on (1) or off (0).

Channel 0 is the keyboard/screen channel; channel 1 is the 9902 that is already wired into the PCB. Channels 2–15 are implemented in software and only require the addition of extra 9902s on the CRU bus. The Cortex powers up set to UNIT 1. Executing UNIT 2 disables the keyboard and passes control to the 9902. UNIT 3 enables both simultaneously.

TABLE 1

SIZE	DDEN	TRANSFER RATE (kHz)	DIVISION RATIO (IC87)	MONOSTABLE PERIOD (uS)	COMMENTS
0	0	125	12	3.0	5¼" single density
1	0	250	6	1.5	5¼" double density
0	1	250	6	1.5	8" single density
1	1	500	3	0.75	8" double density

BUYLINES

Powertran are supplying complete kits of parts and component packs for the Cortex. A complete 64K Cortex kit will cost £295 plus VAT, carriage free A ready-built 64K Cortex will cost £395 plus VAT, carriage free. Prices for add-ons (eg floppy discs, RS232C interface, memory expansion etc) and for component packs (eg PCB, semiconductors etc) can be found in Powertran's brochure. Powertran Cybernetics, Portway Industrial Estate, Andover, Hants SP10 2NM. Telephone 0264 64455.

HOW IT WORKS—I/O

The I/O map space is split into two regions; the bottom region is for on-board I/O devices and the top region causes an off-board access. (The CPU has an internal I/O area of 16 bits, some of which is reserved for specific hardware functions; the rest is free for the user.) The on-board I/O area of the Cortex is decoded by IC34 into eight 32-bit slots, of which only four are used. Two slots (CS A and CS C) are used for the Asynchronous Communications Controllers (ACCs), the third (CS B) for the parallel I/O for the keyboard data, flags and control lines (such as 'ROM', mentioned in the Memory section), and the fourth for the DMA controller IC8 (CS D).

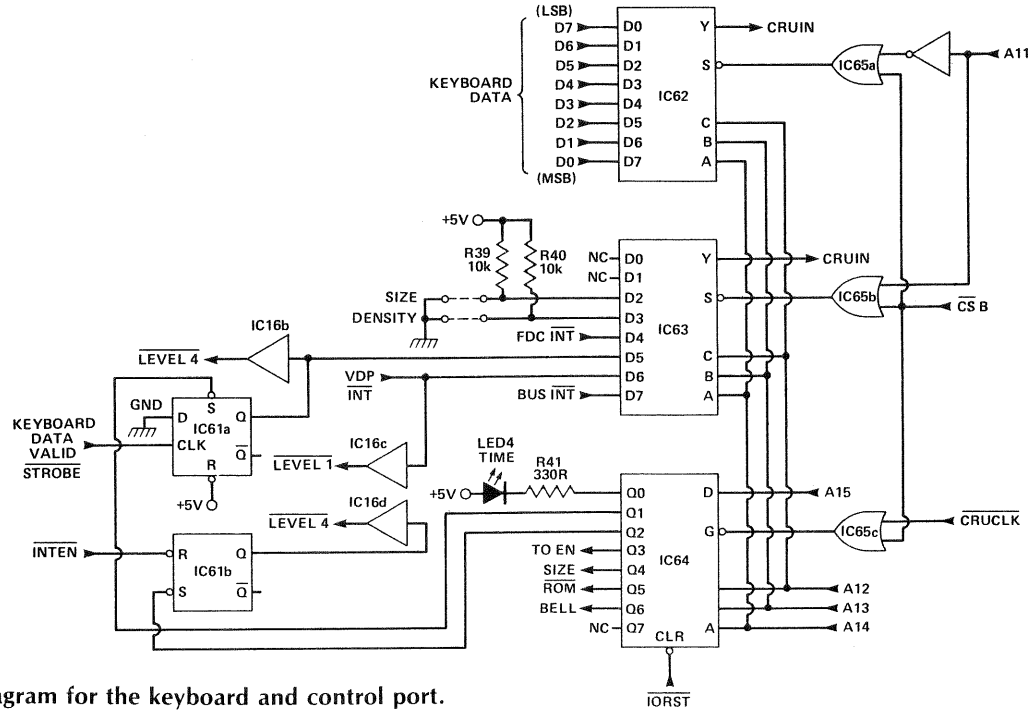


Fig. 1 Circuit diagram for the keyboard and control port.

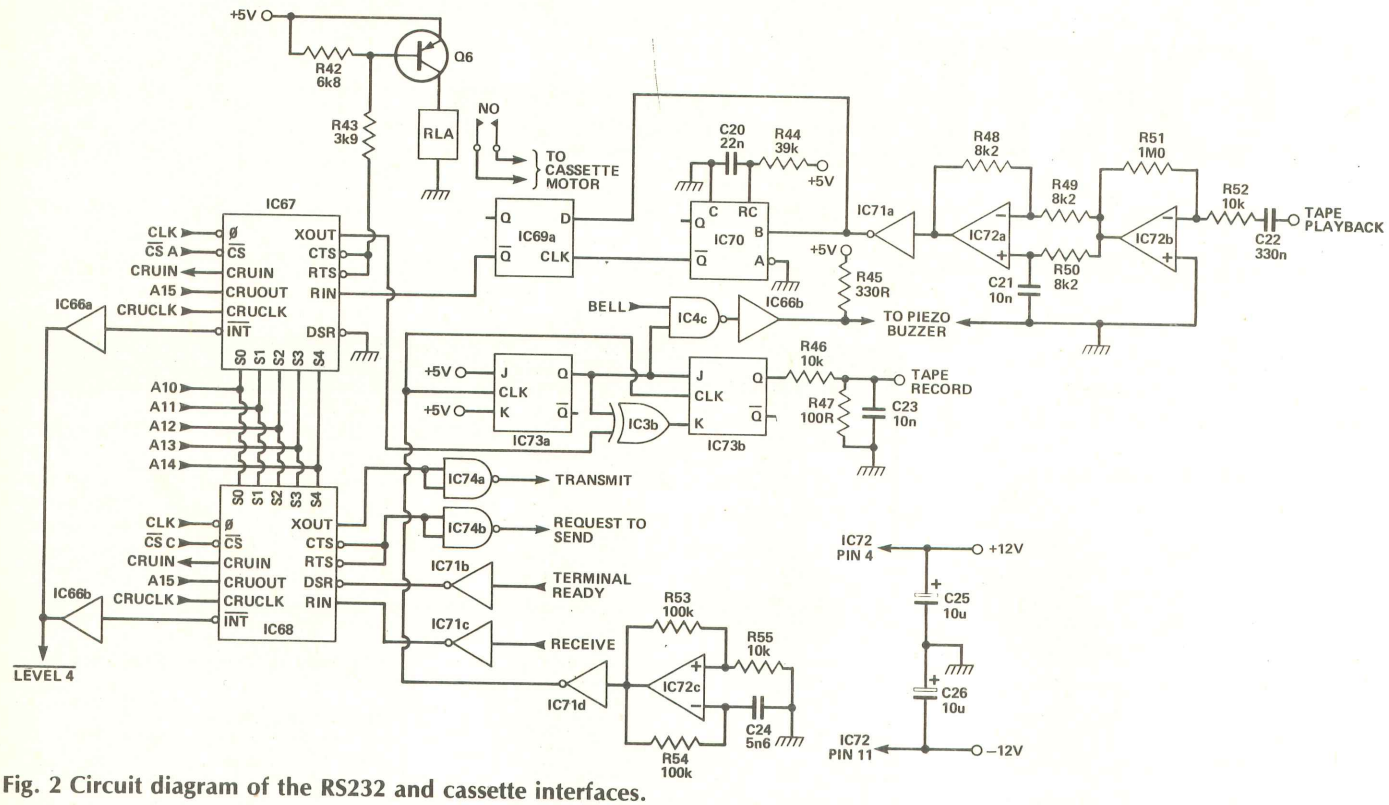


Fig. 2 Circuit diagram of the RS232 and cassette interfaces.

HOW IT WORKS — RS232 AND CASSETTE PORT

The RS232 port consists of IC68, a TMS9902 Asynchronous Communications Controller (ACC) and the TTL-to-RS232 signal level shifters (IC74a,b and IC71b,c). IC68 is a completely software-controlled device; its baud rate can be set at anything from 46 baud to over 100,000 baud. The number of bits to be transmitted or received can also be changed, as can the type, the parity and number of stop bits. The CPU drives the ACC through the serial I/O (CRU) bus. The ACC is decoded as a 32-bit block, each bit being selected by the five address lines A10–A14.

The cassette interface uses another ACC, IC67. First a 4.8kHz op-amp oscillator (IC72c) drives a level shifter (IC71d) before being divided by two in the first flip-flop (IC73a). This ensures that the waveform has a unity mark-space ratio. The serial output from IC67 then controls the action of the second flip-flop, IC73b, via the EXOR gate IC3b. When the output is high, IC73b acts as a shift register, passing through the 2.4kHz tone; however, when the ACC output goes low then synchronously at the next clock pulse, IC73b starts to divide by two, hence generating 1.2kHz. The key point here is the synchronous switch from one tone to the other. The signal is high-pass-filtered and attenuated by R46, R47 and C23 before passing to the tape recorder.

On playback the signal is first amplified by a factor of 100 and buffered in IC72b before going through an all-pass filter, IC72c. This is necessary because of the nature of tape recording. When square waves are recorded on tape they are accurately captured; however, on playback frequency equalisation is carried out in the tape recorder but the phase relationship is destroyed, resulting in a 'spiky' sine wave. This is corrected by the linear phase-shift-versus-frequency characteristic of the all-pass filter. Thus the original square wave shape is recovered at the output of IC72a. This is then level-shifted by IC71a and used to trigger a monostable (IC70a). At the end of the monostable period (312.5 uS) the state of the signal is sampled by the D-type flip-flip IC69a. As the half-periods of the two tones lie either side of the monostable period, each tone generates the opposite logic level at the sample point.

HOW IT WORKS — FLOPPY DISC CONTROLLER

The TMS9909 (IC76) is a highly complex micro-controller, designed to work in conjunction with the TMS9911 DMA controller to transfer data from floppy discs. The FDC can control up to four drives which can be a mixture of two sizes or types.

All signals that go to the drives are open-collector buffered by IC80,82,83 and terminated by a resistor pack on the last drive in the chain. The signals from the drives are terminated on the board by a resistor pack and then buffered by IC84.

The raw data pulses from the drive, after being buffered by IC84a, are stretched by a monostable (IC70b) by an amount dependent on the data transfer rate selected by the 'SIZE' I/O bit and the 'DDEN' (double density enable) signal (see Table 1). The output of the monostable is used to control IC77, a digital phase-locked loop. The output of IC77 is, in the unlocked state, half the input clock frequency. When the loop is locked to a signal then the PLL inserts or deletes clock pulses in the pulse stream, thus shifting the average frequency. The programmable divider IC87 and divider IC69b are controlled by the 'SIZE' and 'DDEN' signals to select the correct clock frequency. The raw data is synchronised by IC88 to the PLL clock and then fed to the FDC. The FDC separates the interleaved clock and data bits from the pulse stream and sends data bytes via single byte DMA transfers to main memory.

Mini-floppy (5¼") drives require a motor control signal to start and stop the disc rotating. Upon starting, the disc will not be ready for data transfers for one second while the disc gets up to speed. To reduce the time required to access the disc repeatedly IC79b keeps the motor running for five seconds after it is de-selected and IC79a provides the initial one second 'not ready' signal to the FDC. For standard (8") drives that don't generate a 'ready' signal there is a set of four jumpers.

The BASIC interpreter has a 'BOOT' command which causes the FDC to read the first track from disc 1 and execute it as a machine code program. This could, for example, then search for and load the UCSD interpreter. In order that the system can boot from any type of disc there are two jumpers called 'SIZE' and 'DENSITY' which are read by IC63. This enables the BASIC interpreter to set up the FDC correctly.

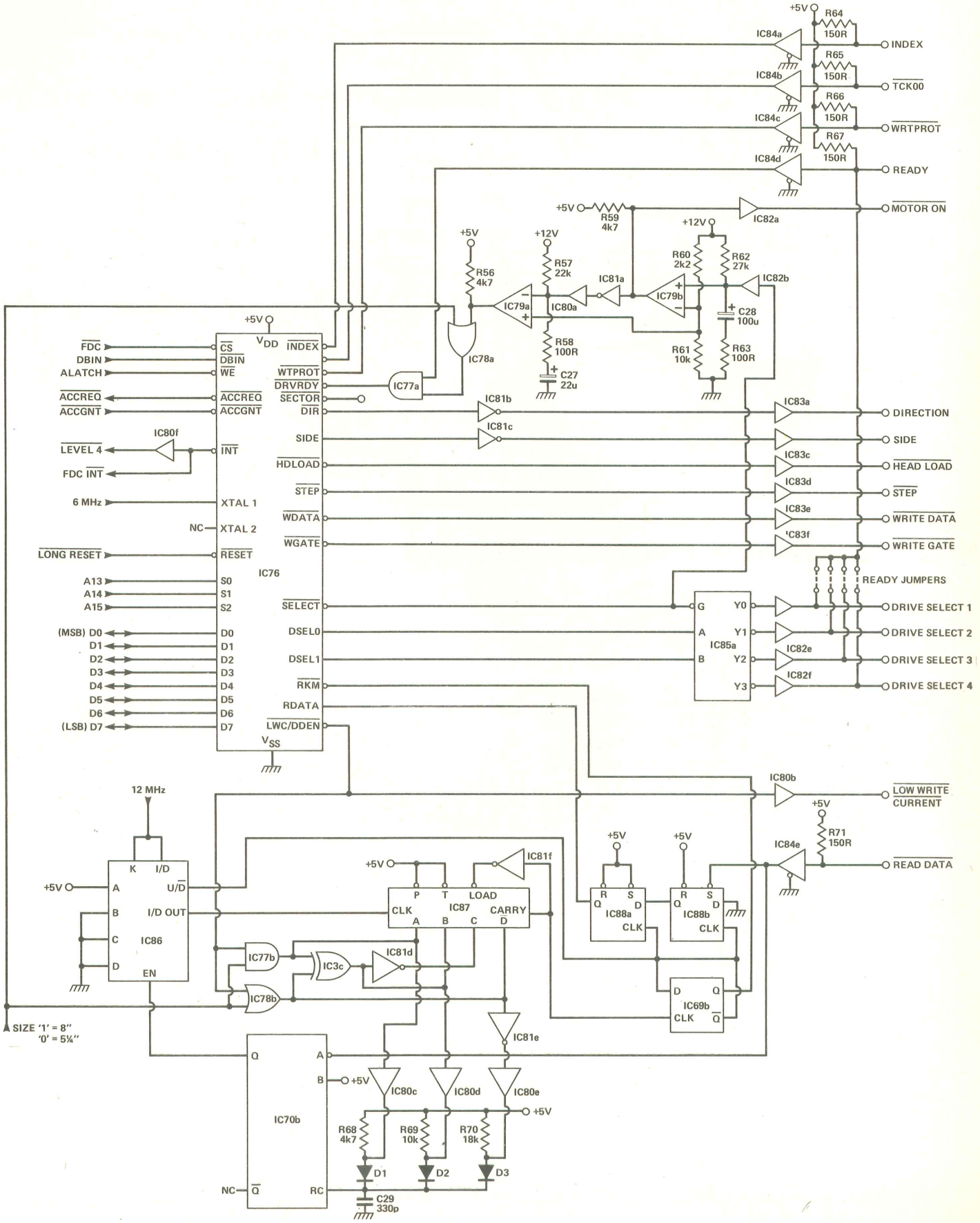


Fig. 3 Circuit diagram for the floppy disc controller section.

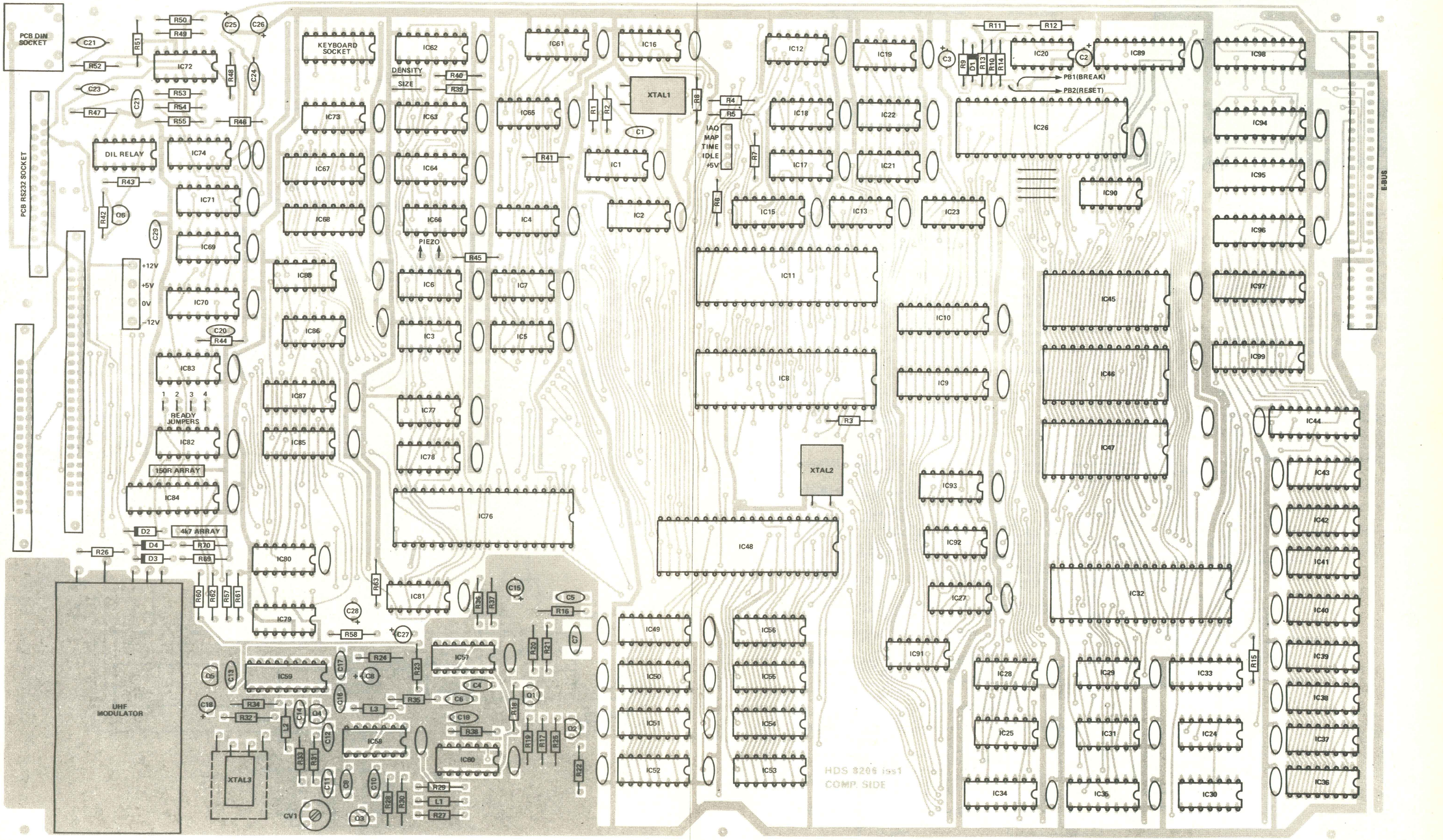
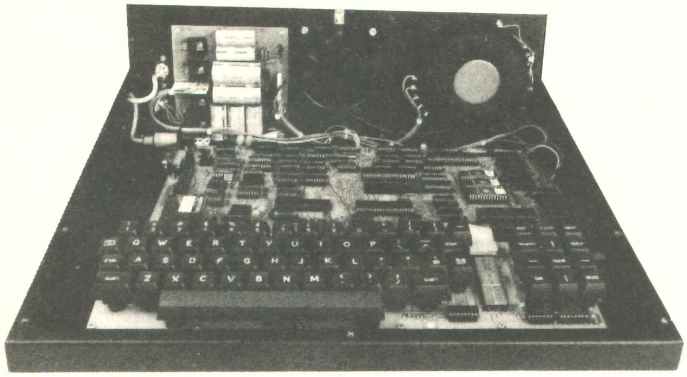


Fig. 4 Component overlay for the Cortex main board. Note that the numerous unmarked capacitors are for supply decoupling and are 47n ceramics. The grey tracks are those on the top (component) side of the board. Some changes in the IC numbering have occurred since last month due to a board redesign. To make last month's circuits agree with the above overlay, alter the labelling thus: IC6a to IC1c, IC6b to IC1d, IC6e to IC1e, IC12a to IC2b, IC1c to IC6c, IC1d to IC12a, IC1e to IC12b, IC1f to IC12c, IC14a to IC4b, IC2b to IC17b. IC14 and IC75 are not used in the new numbering. R26 is not needed in the PAL circuit, but the modulator needs a 10k pull-up to +5 V, so we've called this R26. IC60b clock goes to 0 V, IC60b SET goes to SYNC.



Construction

The main board and the keyboard both have plated-through PCBs, ie there are tracks on both sides and connections between the sides are made by the copper that has been plated onto the sides of each hole. There are therefore no track-link pins; it is, however, good practice to apply solder to EVERY hole to reinforce the connections which in some cases carry power. This happens automatically when boards are 'flow soldered' by passing over a wave of solder in a solder bath during factory assembly. With plated-through boards it is particularly important not to make errors of construction as removal of soldered-in parts is more difficult than on conventional boards and

Fig. 5 Circuit diagram for the E-BUS interface.

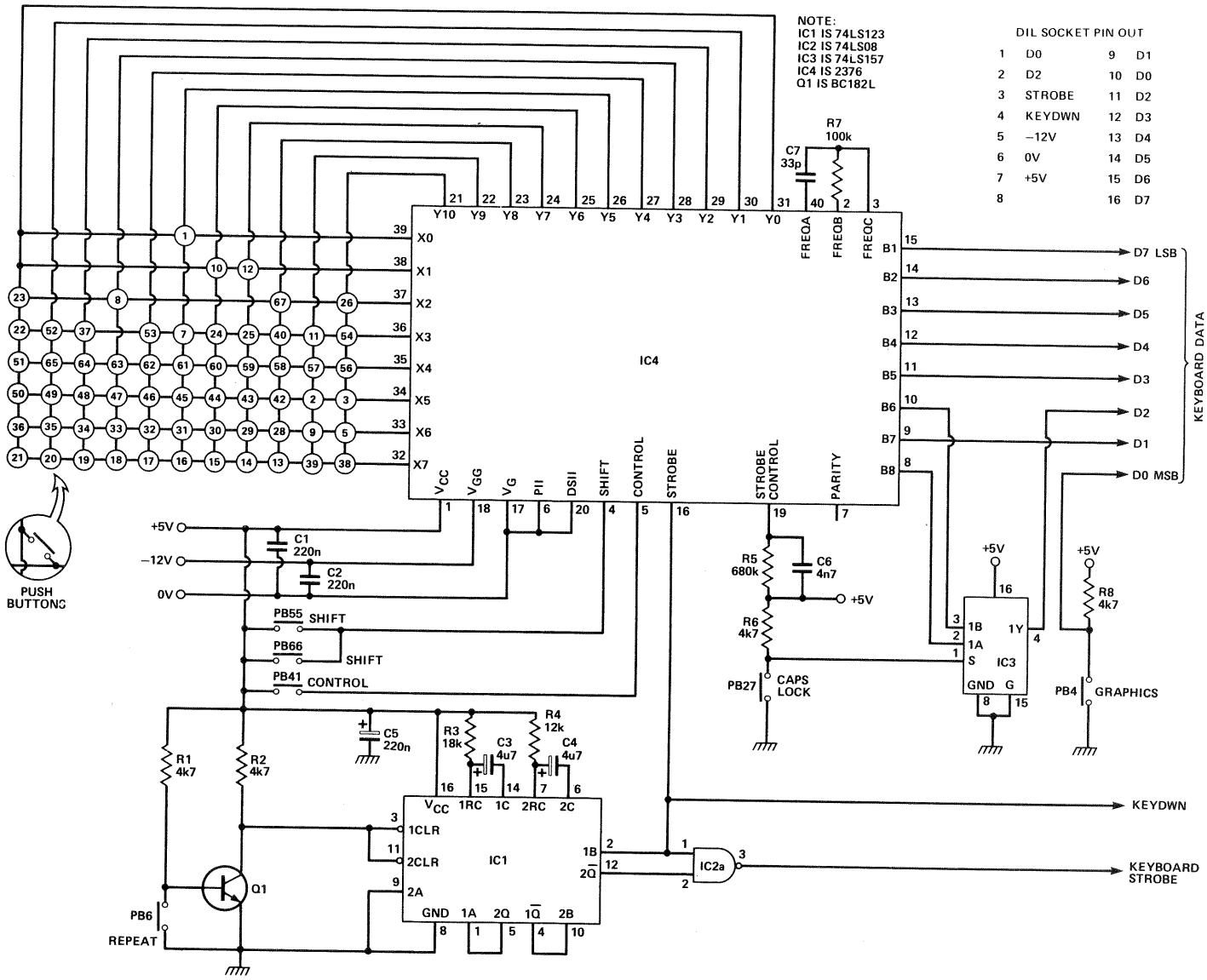


Fig. 6 Circuit diagram for the keyboard.

HOW IT WORKS — E-BUS

The E-BUS is a powerful and compact bus which allows many intelligent cards to share a common resource of memory and I/O cards. In order to share out the resources on the bus, each card has a priority according to its position. This is done by passing a signal down the bus which goes into each card as GRANTIN and comes out as GRANTOUT to form the GRANTIN of the next card. A second signal, BUSY, tells each card if the bus is in use or free. If the bus is free and a card requires the bus, it disables the lower priority cards with the GRANTOUT signal and if the GRANTIN signal and BUSY are OK it asserts BUSY and enables its data and address bus buffers.

Once the bus transfers are complete or if a higher priority card requires the bus, then the card will relinquish control. All these events are synchronised by a backplane clock, BUSCLK. Each data transfer that takes place must signal its completion using $\overline{\text{READY}}$.

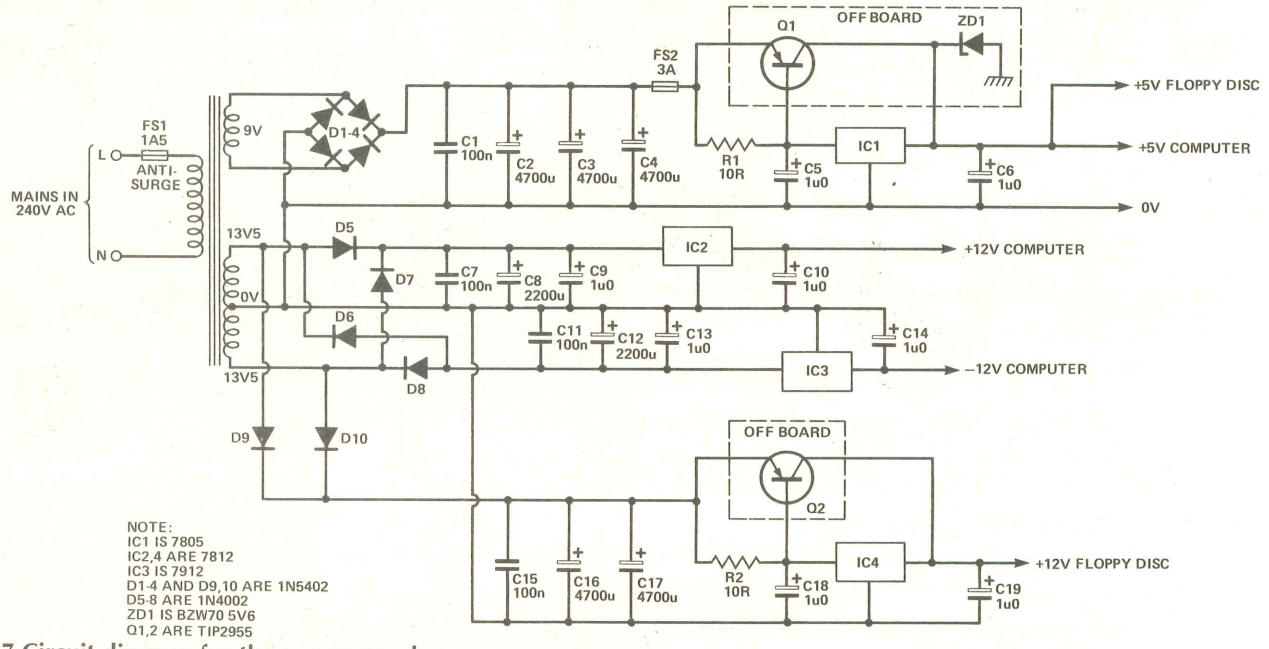
The 74LS2001 gate array (IC89) contains the bus arbitration and control logic to gain and release the bus with timeouts upon error conditions. If the card cannot gain control of the bus after 128 clock cycles, it aborts with a timeout interrupt. Also, if after 16 clock cycles the transfer has not been signalled as complete using the $\overline{\text{READY}}$ line, the controller completes and issues a timeout interrupt.

The E-BUS has provision for a multibit interrupt code signalled by the $\overline{\text{INTEN}}$ signal. This interface only provides a single interrupt level using the $\overline{\text{INTEN}}$ signal. The data, address and interrupt signal are multiplexed onto the same pins to conserve connections. The ALATCH signal is used to enable the address latches when the address is on the bus. Then either $\overline{\text{DEN}}$ or $\overline{\text{WE}}$ will be signalled, to show that either a data read or write is occurring and that data is now on the bus. The $\overline{\text{INTEN}}$ signal can be used to latch the interrupt code.

KEYBOARD

The keyboard is a separate unit providing a fully encoded output. Most of the work is carried out by the 2376 keyboard encoder (IC4). This IC contains a 50 kHz oscillator and two ring counters of eight and 11 stages, the outputs of which form an XY matrix across which the switches are connected. By this means each key is sequentially scanned. The closing of one of the switches for a sufficient length of time for switch bounce to be completed causes the scanning to stop; a 'valid' signal now appears on the strobe output. The encoder also contains a 2376-bit ROM (hence the IC name) arranged as three groups of 88 words of nine bits. The shift and control inputs select one of the three groups and the individual word is addressed by the ring counters.

IC3 is a data selector. D2 is either the output B6 or B8 depending on whether upper or lower case characters are selected by the CAPS LOCK switch. Repeated entry of a character is accomplished by multiple strobe signals from IC1, which is a dual monostable arranged as an oscillator and is enabled by a high level on the clear inputs.



NOTE:
IC1 IS 7805
IC2,4 ARE 7812
IC3 IS 7912
D1-4 AND D9,10 ARE 1N5402
D5-8 ARE 1N4002
ZD1 IS BZW70 5V6
Q1,2 ARE TIP2955

Fig. 7 Circuit diagram for the power supply.

the chances of this being required are much reduced by fitting ALL parts before soldering — if the last part left for fitting is not the one required for the last space you can be pretty sure that the required part is in the wrong holes! IC sockets should be regarded as essential; these are provided with the kits and should be fitted with the index mark corresponding with the index mark on the overlay.

The final part appears next month.

HOW IT WORKS — PSU

The computer main board and keyboard together require a 5 V at 3 A supply, together with low current ± 12 V rails. One amp plastic voltage regulators on small finned heatsinks are used for the 12 V supplies; for the 5 V supply a 1 A regulator is also used but the current-carrying capacity is boosted by bypassing it with a 15 A power transistor, the base current of which passes through the regulator. R1 prevents the off-load input current of the regulator from turning on the transistor when there is no load during testing. The resistor also increases the speed of operation of the transistor. The 1uf capacitors are for the stability of the regulator and the 100nF capacitors are used to remove fast transients orginating from the mains. The zener will clamp any spikes that reach the output.

To simplify the addition of floppy discs these are powered from the same board. The drivers require about 0A7 at 5 V which is also supplied by Q1; they also require + 12 V at 1A6 with higher surges at switch-on, and this is provided by a separate section using Q2 controlled by IC4.

PARTS LIST — MAIN BOARD

Resistors (all ¼W, 5% except where stated)

R1,2	470R
R3-5,11,32	4k7
R6-8,20,21, 28,37,41,45	330R
R9,12,13,15, 39,40,46,52, 55,61,69	10k
R10,14,47, 58,63	100R
R16-19	560R
R22	120k
R23,24,31, 36	1k0
R25,29,33	2k7
R27	390R
R30	1k5
R34	1k8
R35,60	2k2
R38,53,54	100k
R42	6k8
R43	3k9
R44	39k
R48-50	8k2
R51	1M0
R56,59,68	4k7 resistor array
R57	22k
R62	27k
R64-67,71	150R resistor array
R70	18k

Capacitors

C1	1n0 ceramic
C2	4u7 16 V PCB electrolytic
C3,25,26	10u 16 V PCB electrolytic
C4-6,9,10, 17	100n ceramic
C7	470n ceramic
C8	33u 16 V PCB electrolytic
C11,12,16	33p ceramic
C14	47p ceramic
C15,18,27	22u 16 V PCB electrolytic
C19	100p ceramic
C20	22n ceramic
C21,23	10n ceramic
C22	330n ceramic
C24	5n6 ceramic
C28	100u 16 V PCB electrolytic
C29	330p ceramic
CV1	6-30p trimmer

Semiconductors

IC1,6,12,27, 81	74LS04
IC2,17,18, 61,69,88,92	74LS74
IC3	74LS86
IC4,21,31,93	74LS00
IC5,22,30	74LS02
IC7,24	74LS10
IC8	TMS9911
IC9,10,84, 94-96,98,99	74LS244
IC11	TMS9995
IC13,77,90	74LS08
IC15,34,35	74LS138
IC16,66,80, 82,83	74LS07
IC19	74LS164
IC20,79	LM339
IC23	74LS20
IC25,65,78, 91	74LS32
IC26	74LS612
IC28,29	74LS27
IC32	TMS4500
IC33,85	74LS139
IC36-43	TMS4164
IC44,97	74LS245
IC45-47	TMS2564
IC48	TMS9929
IC49-56	TMS4116
IC57,58	4016B
IC59	LM1889
IC60	4013
IC62,63	74LS251
IC64	74LS259
IC67,68	TMS9902
IC70	74LS123
IC71	75189A
IC72	TL084
IC73	74LS73
IC74	75188
IC76	TMS9909
IC86	74LS297
IC87	74LS163
IC89	74LS2001
Q1,3,4	2N3904
Q2,5	2N3906
Q6	BC212
D1-4	1N4148
LED1-4	LEDs to choice

Miscellaneous

PCB (see Buylines); case (see Buylines); IC sockets; I/O connectors to suit; UHF modulator (UM1233 or UM1286).

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